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CMOS photodetector systems for low-level light applications

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Abstract In this work, we have designed, fabricated and measured the performance of three different active pixel sensor (APS) structures. These APS structures are studied in the context of applications that require low-level light detection systems. The three APS structures studied were—a conventional APS, an APS with a comparator, and an APS with an integrator. A special focus of our study was on both the signal and noise characteristics of each APS structure so the key performance metric of signal-to-noise ratio can be computed and compared. The pixel structures that are introduced in this work can cover a wide range of applications, such as high resolution digital photography using the APS with a comparator, to ultra-sensitive biomedical measurements using the APS with an integrator.

1 Introduction

The advances in deep submicron CMOS technologies and integrated microlens have made CMOS image sensors (especially the active pixel sensor—APS) a practical alternative to charge-coupled device (CCD) imaging technology. A key advantage of CMOS image sensors is that they are fabricated in standard CMOS technologies, which allows for full integration of the image sensor with the analog and digital processing and control circuits on the same chip. This "camera-on-chip" system leads to reduction in power consumption, cost and sensor size, and it allows for integration of new sensor functionalities [1].

The advantages of CMOS image sensors over CCDs [1–3] include lower power consumption, lower system cost, on-chip functionality leading to camera-on-chip solutions, smaller overall system size, random access of image data, selective readout, higher speed imaging, and finally the capability to avoid blooming and smearing. Some of the disadvantages of CMOS image sensors compared to CCDs are lower sensitivity, lower fill-factor, lower quantum efficiency, lower dynamic range (DR), all of which translate into the CMOS imager's lower overall image quality [1–3]. Typical APS sensors have a fill-factor (FF) of around 30% and the FF is typically limited by the interconnection metals and silicides that shadow the photosensitive area and recombination of the photo-generated carriers with majority carriers [2].

Among the many emerging CMOS imaging applications, biomedical applications that require very low-level light imaging systems are considered a major design challenge. Low-level light bioluminescence applications [4] require novel techniques to reduce the sensor noise and dark current and to increase the gain and sensitivity to low-light levels. Such techniques may involve designs such as the one described in [5], where sensitivity to low-light levels was increased by biasing the photodiode of each pixel to near zero volts and by separating the photodiode from the integration node. Most successful designs that offer higher dynamic range and lower noise comprise of a smart APS, where data processing is done on the pixel level [1]. Pixel level processing, which can be referred to as interpixel analog processing [6], can provide high SNR, low-power consumption, increased DR through adaptive

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image capturing and processing, and high speed due to parallelism and processing during the integration time [6]. Since there is a practical limit on the minimum pixel size (4–5 μm), then CMOS technology scaling can be used to increase the number of transistors to be integrated into each pixel. For example, when using a CMOS 0.18 μm technology with a 5 × 5 μm^2 pixel and a 30% FF, eight analog transistors or 32 digital transistors can be integrated within the pixel [6].

Since digital transistors take more advantage of CMOS scaling properties, digital pixel sensors (DPS) have become very attractive [1]. A digital pixel sensor integrates an analog-to-digital converter (ADC) in each pixel and the digital data is read out from each pixel, thus resulting in a massively parallel readout and conversion that can allow for very high speed operation [7–10]. The low FF of DPS sensors is no longer an issue for CMOS technologies of 0.18 μm and below [1, 6]. The high speed readout makes CMOS image sensors suitable for very high-resolution imagers (multi-megapixels), especially for video applications. For example, in [8], a 352 × 288 pixel CMOS image sensor was presented that is capable of operating at 10,000 frames/s (1 Gpixel/s) with a power consumption of 50 mW.

Smart pixels have been reported to reduce the fixed-pattern noise (FPN) by more than 10 times and to increase the dynamic range [11–13]. For example, in [14], the high DR of 132 dB was achieved in a CMOS APS structure. In another example [15], the low-power design (40 nW per pixel from a 3.3 V supply) with an in-pixel ADC and a free running continuous oscillator achieved a DR of 104 dB. Block-of-pixel readout was achieved in [16] using a DPS design that allowed for seamlessly scanning a 5 × 5 pixel kernel filter across a pixel array of 64 × 32 rather than a line-readout that would require reading five lines to obtain the 5 × 5 block. In [17], a 1-bit first order Sigma-Delta (ΣΔ) modulator used 17 transistors for each 2 × 2 block of pixels, 4.25 transistors per pixel, to directly convert photocharge to bits. The design is suitable for infrared (IR) applications which require large charge handling capabilities and fine quantization levels. A Nyquist rate multi-channel-bit-serial (MCBS) ADC using successive comparisons, 4.5 transistors per pixel, to convert the pixel voltage to bits, was presented in [18]. This design [18] is suitable for visible applications where low fixed-pattern noise and low data rates are required. A pulse-frequency modulation (PFM) scheme was used in [19] to achieve pixel level ADC with a 23% FF to allow for low-light adaptation by adjusting the saturation level. The average power consumption per pixel is 85 μW in a 0.25 μm CMOS technology. Using two integration times, a linear APS sensor achieved a DR of 92 dB as compared to a DR of 61 dB with only one integration time [3].

Despite the many improvements in CMOS sensors, some of which were highlighted above, there are currently no CMOS image sensors that can provide the image quality of CCDs in terms of noise, sensitivity and dynamic range [3]. This makes CMOS image sensors application specific, since it is possible to improve some of the characteristics of the sensor, but not all of them. Different kinds of image sensors satisfy different performance requirements such as for digital photography, industrial vision, or for medical or space applications.

In this article, three APS structures—the conventional APS sensor, the APS with an integrator, and the APS with a comparator, are discussed and compared to show their applicability to different applications. The article is organized as follows. Section 2 introduces the three different APS structures, and the measurements performed—the conventional APS (Sect. 2.1), the APS with comparator (Sect. 2.2), and the APS with integrator (Sect. 2.3). In Sect. 3, the performance of the three different APS structures is compared and their suitability for specific applications discussed. Finally, in Sect. 4, the conclusions are presented.

2 Pixel structures studied

In this work, we have designed and fabricated (using a foundry process) three different APS structures. The pixels are fabricated in a 0.18 μm, single poly, six-metal layer, salicide commercial CMOS technology. The different pixel structures are fabricated in the same technology and on the same die. In this way, a fair comparison of their performance can be made. The performance characteristics of the pixels are compared to verify their suitability for low-level light and other applications.

2.1 Three transistor APS

Three transistor APS is the simplest and most commonly used APS structure. Each pixel in this structure consists of a photodiode and three transistors. Figure 1a shows the APS circuit, with its designed layout shown later in Fig. 7a. The pixel operates in repeating integration and reset periods. During the integration time, transistor M1 is off and the photodiode junction capacitance discharges by the internally generated photocurrent and dark current. The voltage drop during the integration period is proportional to the light intensity. At the end of integration, this voltage drop is read through transistor M2 which acts as a buffer. Transistor M3 connects the pixel to the readout bus. At the beginning of reset period, transistor M1 is turned on for a few microseconds to charge the photodiode junction

capacitance and to make the pixel ready for the next reading. Figure 1b shows the measured output waveform of the APS along with the reset signal. The integration time in this measurement is 20 ms and the voltage drop is about 400 mV.

Low-level light applications require detectors with high signal-to-noise ratios (SNRs). The noise at lower levels of light can limit the detection capability of the optical sensor. There are different noise sources that affect the performance of an APS. During reset, the dominant noise source is the thermal noise. The noise power in the sense node voltage generated during reset is given by:

$$\overline{V_n^2} = \frac{kT}{2C}, \tag{1}$$

where k is the Boltzmann's constant, T is the temperature in Kelvin, and C is the sense node capacitance. The effect of 1/f noise during reset has been analyzed in [20], and it has been shown that the reset noise is dominated by thermal noise.

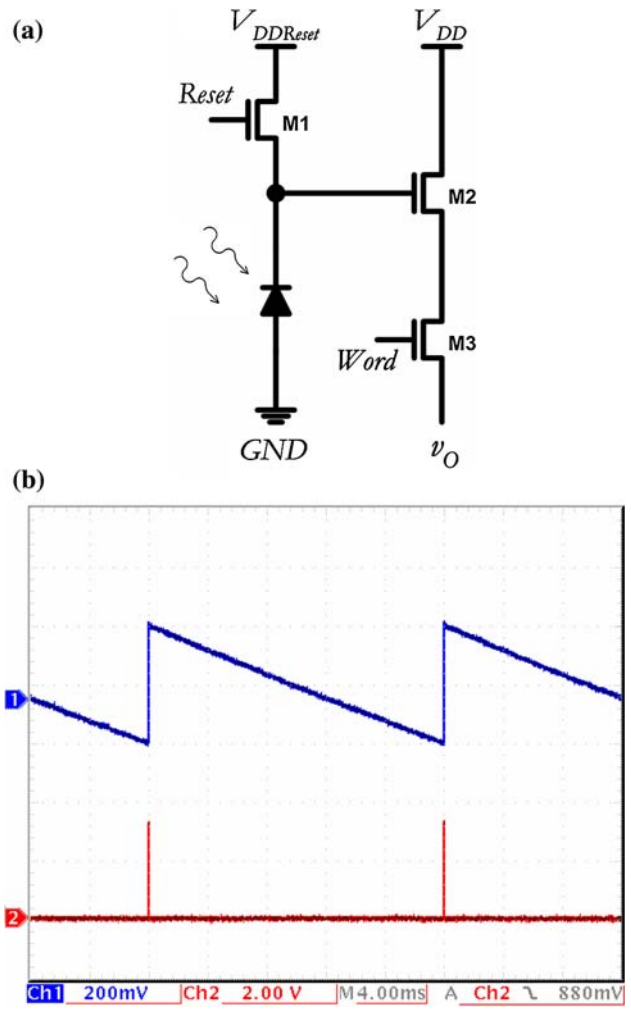

Fig. 1 (**a**) Structure of a three transistor active pixel sensor. (**b**) Output of the APS on channel 1 and reset signal on channel 2, captured on the oscilloscope screen

During integration, the shot noise is the dominating source of the noise. The noise power in the sense node voltage at the end of integration is approximately given by:

$$\overline{V_n^2} \simeq \frac{q(i_{PH} + i_{DK})}{C^2} t_{int}, \tag{2}$$

where q is the electronic charge, t_{int} is the integration time, i_{PH} is the photocurrent, and i_{DK} is the dark current. The signal at the end of integration can be approximated with $(i_{PH}/C)t_{int}$. Assuming that all other sources of noise are small compared to the shot noise and that the dark current is negligible, then the SNR of the output (in dB), before saturation, can be approximated by:

$$SNR \simeq 10 \log \frac{i_{PH} t_{int}}{q} \tag{3}$$

Figure 2 shows the measured signal-to-noise ratio (SNR) of our APS, at different light levels for different durations of integration time. Equation 3 indicates that SNR improves by increasing the integration time [21], given that the pixel capacity is not saturated at the end of integration. Figure 2 implies that the SNR curve will cross zero at lower levels of light for a longer integration time. However, the integration time is limited in length by the rate of temporal variation of the signal to be measured. Also, the dark current of the pixel may saturate the pixel capacity before the long integration time ends.

The number of transistors that could fit into a pixel was limited in past. This was due to the large size of transistors compared to the desired pixel pitch for medium- to high-resolution imagers. Deep submicron technologies have made it possible to put more transistors into the same die area. This has made the transition from passive pixel

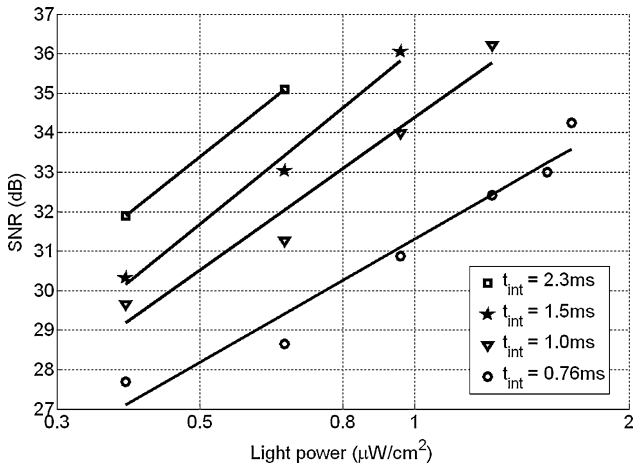

Fig. 2 Signal-to-noise ratio (SNR) of the APS measured at different light powers and for different integration times. Equation 3 suggests, and our measurements indicate, that in the region of operation of APS where the shot noise during integration is the dominant noise source, that the output SNR varies linearly with the logarithm of light power

sensors (one transistor per pixel) to active pixel sensors (three transistors) and beyond, now possible. It is now feasible to do parts of the data processing within the pixel and develop smart pixels. Smart pixel systems are integrated and can perform sophisticated tasks faster than conventional imaging systems. In the following subsections we analyze two APS pixels with in-pixel circuitry that are the core of many smart pixels.

2.2 APS with comparator

The general structure of our APS pixel with an internal comparator is shown in Fig. 3a. The pixel consists of eight transistors including the reset transistor, with the layout shown later in Fig. 7b. The pixel has a reference level input and its output has a digital "High" or "Low" value, depending on the value of the sense node voltage across the photodiode relative to the value of the reference voltage of the comparator v_{ref}. The photodiode and reset transistor combination of the pixel works in the same manner as the conventional APS. Figure 3b shows different signals from the pixel and how they correspond to each other. Waveforms 1 and 2 in Fig. 3b are the measured reset signal and output of the pixel. Waveforms 3 is an illustration of the internal sense node voltage, and waveform 4 is the reference level. After reset, the sense node voltage is above the reference level and the output is low. The sense node voltage will decrease during integration, and if the light level is high enough, it will cross the reference level. Therefore, the duration of the output pulse at low will be inversely proportional to the light level and this is the output signal of the pixel.

The time at which the output of the pixel goes from "High" to "Low" is fixed by the externally applied reset. The time at which the pulse comes back to "High" however, is affected by the noise that is present in the sense node voltage. The noise sources that contribute to the total noise of the sense node voltage are the same as the three-transistor APS described above in Sect. 2.1. In this APS with a comparator, an easy way to quantify the noise is from the jitter in the rising edge of the output pulse of the comparator. Figure 4a shows the jitter of the output, captured on the oscilloscope screen. Figure 4b shows the root-mean-square (RMS) value of the jitter of the output, compared to the output pulse width. Figure 4b shows that the SNR of the output is not the limiting factor in detection of the low-light-levels using this structure. However, sensing lower light levels requires higher integration times to let the sense node voltage drop enough to cross the reference level. This is similar to the three transistor APS, with the difference being that now the reference level can also be adjusted to optimize the detection of the light intensity range of interest.

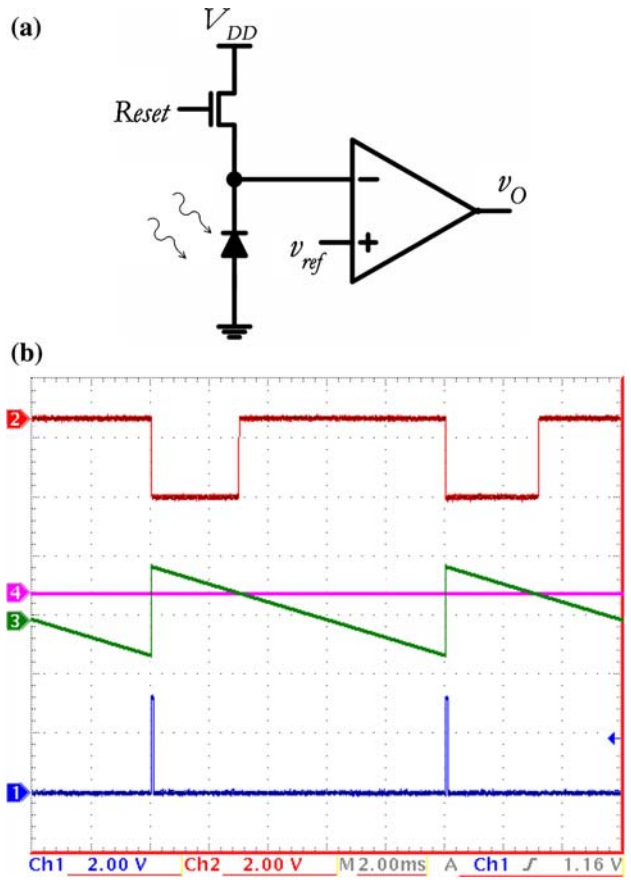

Fig. 3 APS with comparator. (**a**) General schematic of the pixel and (**b**) Its measured and illustrated waveforms. Channel 1 shows the reset signal applied to the pixel, for a 10 ms readout time. Channel 2 shows the measured output of the pixel. Channel 3 shows the internal sense node voltage and compares it to the reference level of channel 4

The main advantage of this structure is the immediate analog-to-digital conversion of the signal, inside the pixel, thus eliminating the readout noise of the consequent stages of the imager. It will also provide a parallel and fast A/D conversion of the signal, making it possible to achieve faster scanning times.

2.3 APS with integrator

In most of the APS structures, including the two that are described above, the photocurrent is integrated by the junction capacitance of the photodiode. A diode however, is not a perfect capacitor, as the junction capacitance changes with the applied bias [21]. As a result, output of the APS becomes nonlinear [21, 22] and this has an impact on both the signal and SNR characteristics [23]. It should be mentioned that the sense node voltage capacitance of an APS has a parallel component equal to the gate-source

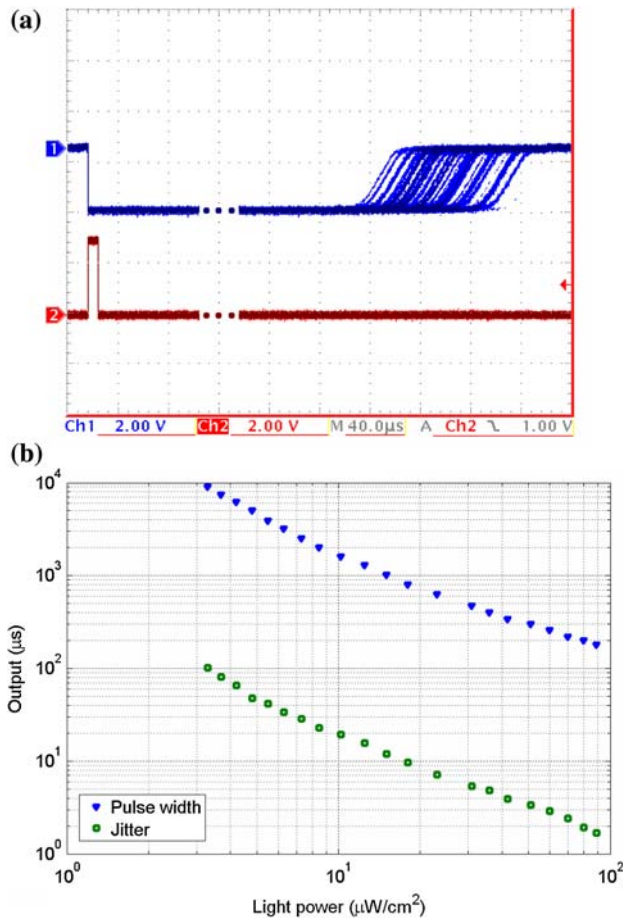

Fig. 4 (**a**) Measured output of the APS with comparator, zoomed in to show the jitter in its output. This jitter is the noise of the output as the pulse width is the output of the pixel. (**b**) Measured signal (pulse width) and noise (jitter) of the output of the pixel, as a function of light power

capacitance of the buffer transistor (M2 in Fig. 1a). One can reduce the effect of nonlinear capacitance of the photodiode, by making the gate-source capacitance of M2 high, such that it dominates the sense node capacitance. This solution will keep the capacitance at the sense node relatively constant. However, it will result in an increase in the size of the buffer transistor, thus reducing the fill-factor of the pixel. It will also reduce the charge-to-voltage conversion gain of the pixel, thus degrading its sensitivity. An integrator, using an operational amplifier, can solve this problem by keeping the sense node voltage constant and integrating the photocurrent in its fixed capacitor. We have designed a pixel with a current integrator that integrates the photocurrent into an on-chip metal-oxide-metal capacitor. The schematic of the APS with integrator is shown in Fig. 5a, with its layout shown in Fig. 7c.

The measured output of the APS with integrator is shown in Fig. 5b. After the reset period, the capacitance of the integrator discharges. During integration, the operational amplifier of the integrator keeps the bias over the photodiode fixed. This causes the photocurrent generated in the photodiode to be integrated in the capacitor rather than the photodiode. The output of the integrator will then increase in proportion to the generated photocurrent during the integration time.

Figure 6 shows how the output of the APS with integrator varies with the incident light power. The measurements are done for light at different wavelengths and they show good linearity of the output with respect to the power of incident light, unless the pixel is saturated.

Analysis of the shot noise during integration, for the APS with integrator, is similar to the three transistor APS with the only difference being in the value of the capacitance. However, the effect of 1/f noise will be more important now, as different elements of the integrator also contribute to the 1/f noise. It is important to remember that frequency domain analysis is not applicable for the analysis of 1/f noise in this circuit, as APS is a switched circuit, and the 1/f noise will appear as a cyclo-stationary process in its

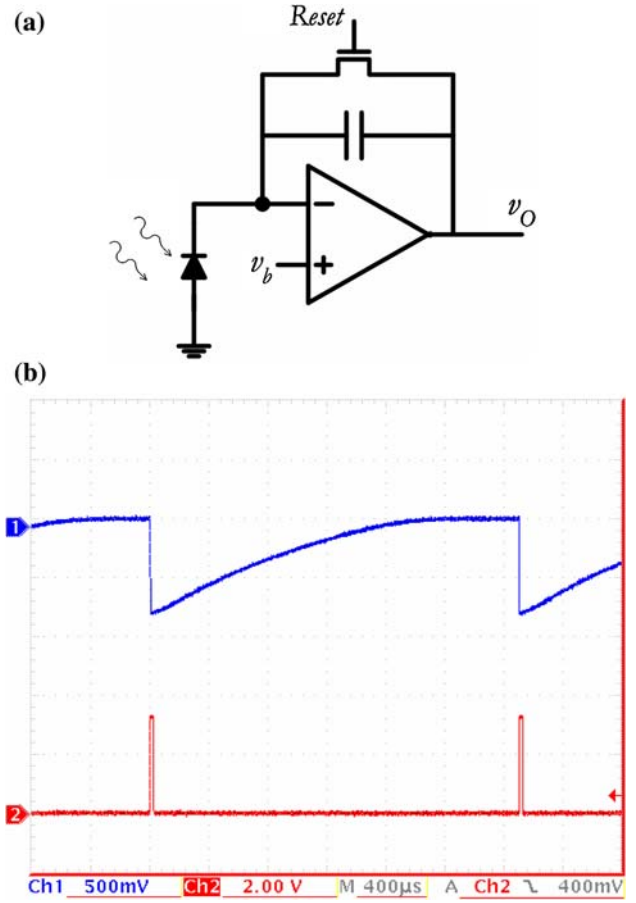

Fig. 5 APS with integrator. (**a**) General schematic of the pixel and (**b**) Its measured waveforms. Channel 1 shows the measured output of the pixel, while channel 2 shows the reset signal applied to the pixel, for a 2.5 ms readout time

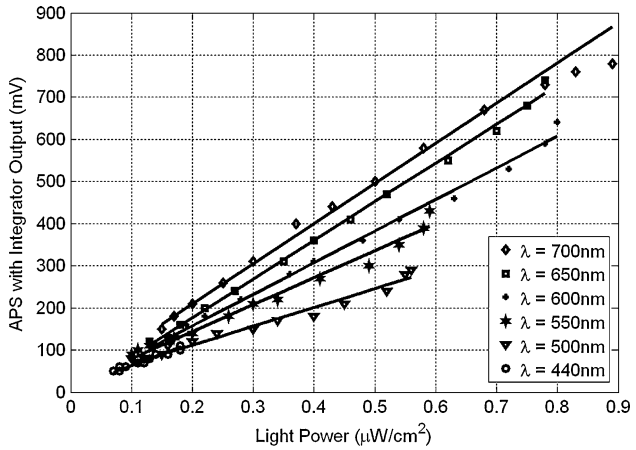

Fig. 6 Output of the APS with integrator, sampled at different levels of incident light power. Measurements are done at different wavelengths. It can be observed that a good linearity exists in the output, unless the output saturates, as shown in the curve for the 700 nm light

output [20]. A time domain analysis of the noise, using the auto-covariance function of the equivalent total trap number in the trap model of the 1/f noise δ, can be performed to get the power of noise [21], and the result is:

$$\overline{V_n^2} = \left(\frac{q}{CAt_r}\right)\int_0^{t_r}\int_0^{t_r}\delta(\tau_1, |\tau_2 - \tau_1|)d\tau_2 d\tau_1 \qquad (4)$$

where A is the channel area of the reset transistor and t_r is the reset time. The output noise level of the APS with integrator, in general, is higher than the equivalent three transistor APS pixel.

One advantage of the proposed APS with integrator design is that the size of the photodiode and the capacitance of the integrator can be chosen independently. Thus the capacity of the pixel can be adjusted while keeping the photosensitive area of the pixel fixed. The main advantage of this structure, however, is its performance in dark. The amplifier of the structure keeps the bias applied to the photodiode fixed. The bias level is controlled by the input v_b which is very close to zero. At these small bias voltages, the dark current generated in the photodiode is small compared to the dark current of the conventional APS generated at a bias close to V_{DD} [24]. As a result, the output voltage read from the pixel at dark will be small, compared to the three transistor APS.

3 Comparison and discussion

Three different APS structures are introduced in this work. Each of the structures has characteristics that make it suitable for certain types of applications. Table 1 compares these structures and some of their key performance measures. The three transistor APS has the simplest structure and highest fill-factor. It is suitable for applications that require ultra-high resolution imaging. It has also the least noisy output, because it has the least number of transistors in its data path to the output.

The APS with the comparator structure has an acceptable fill-factor of 36% due to our compact design, and this is shown in Fig. 7b. It has a digital output, which makes it applicable to ultra-fast digital imagers. It is possible to adjust the reference level and integration time, and thus to achieve good sensitivity at the desired light levels. It also has the widest dynamic range, as the sense node voltage is

Table 1 Comparison of the APS structures studied

	APS	APS with comparator	APS with integrator
Photodiode size	20 × 20 μm²	10 × 10 μm²	10 × 10 μm²
Number of transistors	3	8	6
Fill-factor	63%	36%	15%
Output swing	1 V	2.2 V	0.8 V
Dark output rate	50 mV/s	210 mV/s	16 mV/s

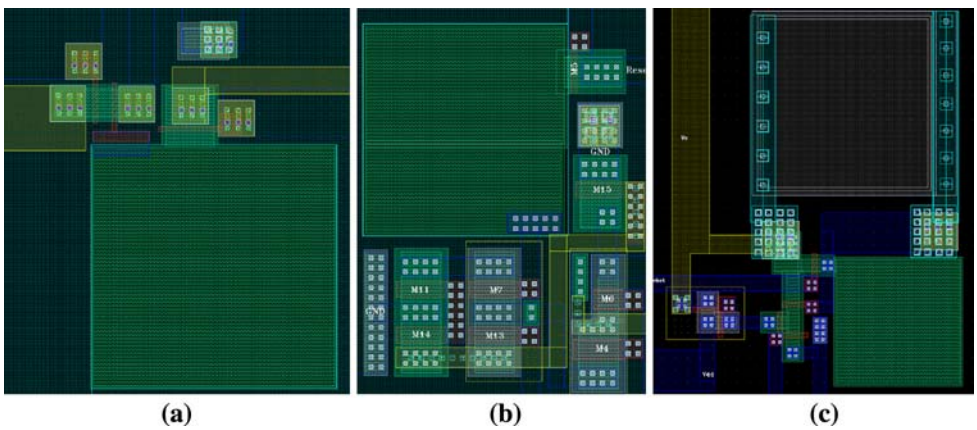

Fig. 7 Layouts of different APS structures. (**a**) Three transistor APS has the simplest layout and highest fill-factor. (**b**) The APS with comparator has eight transistors. However, our compact design has kept the fill-factor at a high level. (**c**) The APS with integrator. This design considers a capacitor in each pixel that reduces the fill-factor of the pixel. However, the fill-factor is still at a reasonable level

read and converted to digital level immediately, and the overhead voltage drops of amplifier and buffer stages do not affect the output.

The APS with integrator structure has a low fill-factor. It has a low dynamic range, is slow, thus it is not suitable for applications that require high scanning rates. However, its output is the most linear with respect to incident light power, and it has an internal dark current cancellation mechanism. These two features make this APS structure a good candidate for low-level light imaging using longer integration times.

4 Conclusions

In this research, we have carefully compared the key performance characteristics of three different active pixel sensor structures—size of photodiode, number of transistors in pixel, fill-factor, output swing and dark output rate. The pixel structure with control transistors inside the imager pixel provides advantages such as easy integration in a two-dimensional array with readout capabilities compared to using only a photodiode. The simple three transistor APS is effective for high resolution and low noise applications. The APS with a comparator pixel is good for fast digital imaging and provides high dynamic range. Finally, the APS with a comparator has linear response and has the lowest dark output rate.

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References

1. A. El Gamal, H. Eltoukhy, IEEE Circuit. Devic. **21**(3), 6–20 (2005)
2. E.R. Fossum, IEEE T. Electron. Dev. **44**(10), 1689–1698 (1997)
3. M. Bigas, E. Cabruja, J. Forest, J. Salvi, Microelectr. J. **37**, 433–451 (2006)
4. H. Eltoukhy, K. Salama, A. El Gamal, M. Ronaghi, R. Davis, Proc. Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2004, pp. 222–223
5. J. Honghao, P.A. Abshire, IEEE International Symposium on Circuits and Systems (ISCAS 2006) pp. 1651–1654
6. A. El Gamal, D. Yang, B. Fowler, Proc. SPIE. **3650**, 2–13 (1999)
7. B. Fowler, A. El Gamal, D.X.D. Yang, Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, (1994) pp. 226–227
8. S. Kleinfelder, S.H. Lim, X.Q. Liu, A. El Gamal, Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, (2001) pp. 88–89
9. D. Yang, A. El Gamal, B. Fowler, H. Tian, IEEE J. Solid-St. Circ. **34**, 1821–1834 (1999)
10. W. Bidermann, A. El Gamal, S. Ewedemi, J. Reyneri, H. Tian, D. Wile, D. Yang, Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, (2003) pp. 212–213.
11. N. Faramarzpour, M.J. Deen, S. Shirani, Q. Fang, L.W.C. Liu, F. Campos, J.W. Swart, IEEE T. Electron. Dev. **54**, 9 (2007) December
12. L. Liang-Wei, C.-H. Lai, Y.-C. King, IEEE Sensors J. **4**(1), 122–126 (2004)
13. J.L. Trepanier, M. Sawan, Y. Audet, J. Coulombe, IEEE International Midwest Symposium on Circuits and Systems Vol. **2**, 437–440 (2002)
14. D. Stoppa, A. Simoni, L. Gonzo, M. Gottardi, G.-F. Dalla Betta, IEEE J Solid-St Circ **37**(12), 1846–1852 (2002)
15. L.G. McIlrath, IEEE J. Solid-St. Circ. **36**, 846–853 (2001)
16. B. Tongprasit, K. Ito, T. Shibata, IEEE International Symposium on Circuits and Systems Vol. **3**, (2005 ISCAS), pp. 2389–2392
17. B. Fowler, A. El-Gamal, Proc. Infrared Readout Elect. IV, SPIE **3360**, 2–12 (1998)
18. D. Yang, B. Fowler, A. El Gamal, IEEE J Solid-St. Circ. **34**, 348–356 (1999)
19. A. Bermak, A. Bouzerdoum, K. Eshraghian, Microelectr. J. **33**(12), 1091–1096 (2002)
20. H. Tian, A. El Gamal, IEEE T. Circuits Syst. **48**(1), 151–157 (2001)
21. N. Faramarzpour, M.J. Deen, S. Shirani, J. Vac. Sci. Technol. A (Special Issue Canadian Semiconductor Technology Conference) **A24**(3), 879–882 (2006)
22. N. Faramarzpour, M.J. Deen, S. Shirani, IEEE T. Electron. Dev. **53**(9), 2384–2391 (2006) September
23. Y. Ardeshirpour, M.J. Deen, S. Shirani, J. Vac. Sci. Technol. A (Special Issue Canadian Semiconductor Technology Conference) **A24** (3) (May/June 2006) pp. 860–865
24. Y.C. Shih, C.Y. Wu, IEEE International Symposium on Circuits and Systems Vol. **1**, (ISCAS 2003), pp. 809–812