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Analysis of Dynamic Energy Consumption Sources and Energy Conservation Measures for Bus

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Abstract: This paper focuses on analyzing the influencing factors of bus dynamic energy consumption, providing a bus model related to dynamic energy consumption, as well as the relationship between coupling parameter values and process size changes. By analyzing the calculation formula of bus dynamic energy consumption, measures to reduce bus dynamic energy consumption are pointed out, which is helpful for studying on-chip bus energy conservation issues in deep submicron and nano processes.

Keywords: Dynamic energy consumption, Bus energy-saving, Bus model.

1. Introduction

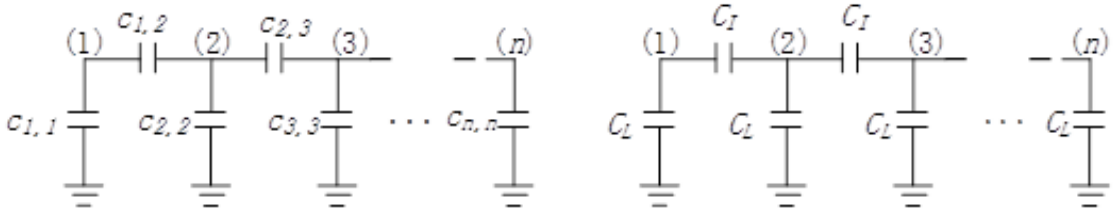
The on-chip bus is responsible for the connection and communication of other components on the chip, and is a medium for the interaction of other components. It is generally composed of parallel distributed, aligned, and identical metal wires located on the same metal layer. The driver and receiver are arranged at both ends of the bit line, and in some cases, a relay is also connected in the middle. Transferring data and instructions over longer and wider buses requires a significant amount of energy consumption and time [1,2]. In some widely used circuit classifications [3], interconnect power consumption even exceeds half of the total power consumption. A low-power circuit design that ensures high-speed performance is not only necessary for portable applications powered by batteries, but also for reducing the power consumption of dedicated VLSI processors, as any additional current density in the interconnect may cause temporary or long-term failures due to voltage drops and electromigration.

In deep submicron (DSM) and nanotechnology, interconnection problems become severe and complex, one of the reasons being the increased coupling capacitance between lines [2]. This is because smaller spacing between bit lines and higher aspect ratios (height/width) are necessary to maintain a reasonable size of linear resistance. Another complexity is the distribution characteristics of slender wires. These two issues are believed to become more prominent in future technology.

2. Bus Energy Consumption Model and Analysis of Influencing Factors

For a DSM bus with n bit lines considering coupling capacitance, the coupling capacitance and boundary capacitance between non adjacent bit lines are ignored. The approximate bus model related to energy consumption is shown in Figure 1 (a), and the total capacitance matrix can be represented by a tridiagonal matrix as formula (1).

$$C'_T = \begin{bmatrix} c_{1,1}+c_{1,2} & -c_{1,2} & 0 & \text{B} & 0 & 0 \\ -c_{1,2} & c_{1,2}+c_{2,2}+c_{2,3} & -c_{2,3} & \text{C} & 0 & 0 \\ 0 & -c_{2,3} & c_{2,3}+c_{3,3}+c_{3,4} & \text{E} & \text{C} & \text{C} \\ \text{C} & \text{C} & \text{C} & \text{B} & c_{n-2,n-1}+c_{n-1,n-1}+c_{n-1,n} & -c_{n-1,n} \\ 0 & 0 & \text{B} & \text{B} & -c_{n-1,n} & c_{n-1,n}+c_{n,n} \end{bmatrix} \quad (1)$$



(a) DSN approximate bus model related to energy consumption

(b) Simplified DSNI approximate bus model related to energy consumption

Figure 1. An approximate DSM bus model

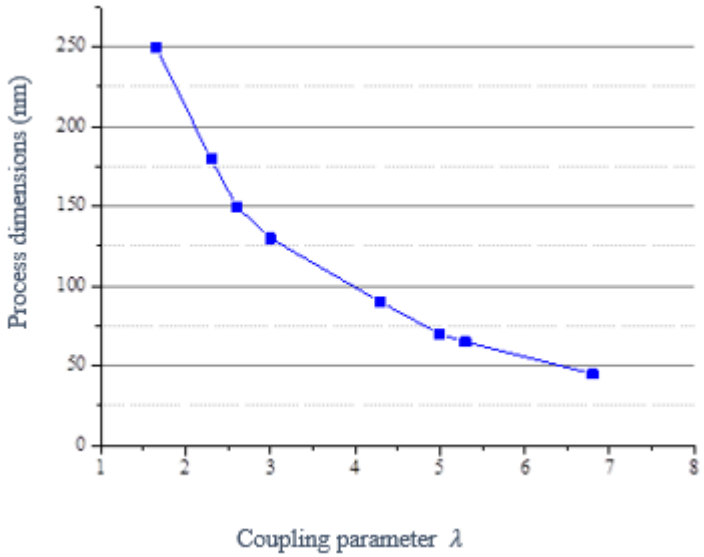


Figure 2. Relationship between coupling parameter values and process dimensions

If we make the capacitance of all bit lines to ground equal, that is $c_{1,1}=c_{2,2}=c_{3,3}=\mathrm{B}=c_{n,n}=C_L$, the coupling capacitance between lines is equal, that is $c_{1,2}=c_{2,3}=\mathrm{B}=c_{n-1,n}=C_I$, the model can be further simplified as shown in Figure 1 (b). At this point, the total capacitance can be expressed as formula 2, coupling parameter $\lambda=C_I/C_L$. Combined with references [4,5], we can obtain the relationship between the values λ and the changes in process dimensions under different process sizes as shown in Figure 2.

$$C_T=\begin{bmatrix} 1+\lambda & -\lambda & 0 & \mathrm{B} & 0 \\ -\lambda & 1+2\lambda & -\lambda & \mathrm{C} & 0 \\ 0 & -\lambda & \mathrm{E} & \mathrm{C} & \mathrm{C} \\ \mathrm{C} & \mathrm{C} & \mathrm{C} & 1+2\lambda & -\lambda \\ 0 & 0 & \mathrm{B} & -\lambda & 1+\lambda \end{bmatrix} C_L \quad (2)$$

Under the approximate bus model in Figure 1 (b) [6], the bus energy consumption formula can be expressed as formula (3), where V^i indicates the initial voltage before transmitting data values, which can be expressed as $V^i=[V_1^i,V_2^i,\mathrm{B},V_n^i]^T$, V^f indicates the termination voltage after transmitting data values, which can be expressed as $V^f=[V_1^f,V_2^f,\mathrm{B},V_n^f]$.

$$E=(V^f)^T\cdot C_T\cdot(V^f-V^i) \quad (3)$$

For the i-th bit line $V_i^f=V_{DD}\cdot S_i$, V_{DD} represents the power supply voltage, and Si represents a jump, which is determined to be 0 or 1 based on the transmitted value. By combining formulas (2) and (3), we can obtain formula (4) to calculate bus energy consumption. Where SW_i indicates the number of bit transformations (vertical distance or Hamming distance) on the i-th bit line, caused by its own capacitance, will occur when the consecutive data transmitted on the bit line, that is, the current value and the previous value, change from 0 to 1 or from 1 to 0. $SW_{j,j+1}$ indicates the number of coupling transformations (horizontal distance) on adjacent bit lines j and j+1, caused by coupling capacitance, occurs when adjacent bit lines change their values simultaneously, i.e. from 00 to 11, from 11 to 00, from 10 to 01, from 01 to 10. When=0, it represents a bus model that does not consider coupling capacitance. At first, we will examine bus energy-saving methods that do not consider the influence of coupling capacitance, and then, we will study bus energy-saving methods that consider the influence of coupling capacitance.

$$E=V_{DD}^2\cdot(\sum_{i=1}^{n}SW_i+\lambda\cdot\sum_{j=1}^{n-1}SW_{j,j+1})\cdot C_L \quad (4)$$

From formula (4), it can be seen that there are various factors that affect bus energy consumption: power supply voltage, number of bus bit lines, self-capacitance and coupling capacitance, as well as the number of vertical and horizontal transformations brought about by them. From the perspective of data transmission, factors that affect bus energy consumption also include the amount of data transmission on the bus.

3. Measures to Reduce Dynamic Energy Consumption of Bus

To achieve the goal of bus energy conservation, according to formula 4, we can optimize or reduce one or more factors based on the above factors, and ultimately achieve dynamic energy consumption optimization of the bus. The following are discussed separately:

(1) Reduce power supply voltage

Lowering the power supply voltage can reduce bus energy consumption, but reducing the power supply voltage will increase data access latency [7]. Therefore, it is possible to reduce the power supply voltage appropriately when performance allows to achieve energy-saving goals. Additionally, reducing voltage swing [8] is also beneficial for bus energy conservation.

(2) Reduce the capacitance of the capacitor itself and the

coupling capacitance

Capacitors, especially coupling capacitors, are related to the material, arrangement, topological distribution, size, etc. of the wires and are generally relatively fixed. In the existing methods, the capacitance value is reduced by adding shielding wires, increasing the spacing between bit lines, and reducing the phase reversal transformation between adjacent bit lines.

(3) Reduce data communication volume

Reducing data communication on the on-chip bus is also a way to achieve bus energy efficiency, such as increasing the hit rate of the on-chip first level cache and reducing the number of requests accessing the second level cache, which can effectively reduce communication on the bus and objectively reduce bus energy consumption.

(4) Reduce the number of bit transformations

The commonly used energy-saving method for existing buses is to reduce the number of transformations, including vertical and horizontal transformations. This method is represented by encoding measures, and bus energy optimization methods based on encoding can usually be divided into three types: algebraic encoding, permutation encoding, and probability encoding. Algebraic encoding refers to the transformation of the original value encoding into other forms of encoding through algebraic transformations, such as bus flipping codes [9]; Permutation encoding refers to only performing permutation transformations on the original value encoding, such as pattern transformation encoding [6]; Frequency coding refers to obtaining the frequency of continuous occurrence of data through statistical analysis of programs, and then encoding data pairs with high probability of occurrence, such as frequent value coding [10]. The above three types of encoding aim to minimize the number of transformations in the encoding value during transmission, and the efficiency of encoding is measured by the total number of transformations. In addition, reducing the number of bit lines involved in data transmission and using as few bit lines as possible to transmit data values can also effectively reduce the number of transformations. Reducing the amount of transmitted communication ultimately results in a reduction in bit transformation, which belongs to the indirect reduction of the number of transformations and can also be classified in this category.

4. Summary

In the paper, it is based on an approximate bus model related to energy consumption, constructs a bus energy consumption model, and provides the relationship between coupling parameter values and process size changes. From the perspective of factors affecting the dynamic energy consumption of the bus, it analyzes the entry points that can be paid attention to in achieving bus energy conservation. Based on these entry points, we can have a more comprehensive understanding of bus energy-saving technology, utilize its advantages, improve existing shortcomings, and provide a basis and reference for designing efficient bus energy-saving methods.

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