

Design and Implementation of DDS Signal Generator Based on FPGA

Shun Li*

School of Physics and Electronic Engineering, Northwest Normal University, Lanzhou 730070, China

*Corresponding author: learn_nwnu@126.com

Abstract: With the rapid development of semiconductor technology, the digital circuit of the control chip gradually replaces the analog circuit of the traditional signal generator, which improves the performance of the signal generator and reduces the cost of research, development and production. This paper proposes a design scheme that takes FPGA chip as the control center. The signal generator system mainly includes DAC module, FPGA module and key module. The system uses Verilog language to develop the sine wave digital signal generation and key switching frequency control logic circuit on FPGA. The frequency control word circuit in the FPGA module provides multiple frequency sine wave selection, and the look-up table circuit realizes the reading of different phases by controlling the read address of the ROM. The 14-bit high-speed DAC module converts the digital signals sent by FPGA into analog signals. The DAC module integrates low-pass filter processing to increase the smoothness of the signal. After testing, the system meets the design requirements.

Keywords: FPGA; DDS; DAC; Verilog.

1. Introduction

DDS signal generator is widely used in communication, radar, medical equipment, scientific research and other fields, for testing and measuring, signal generation and other applications[1]. Traditional signal generators have problems such as low integration, large size, high production cost, poor scalability, etc. This paper designs a DDS signal generator based on FPGA chip. FPGA detects the frequency of waveform generated by key switching, and can realize the conversion of waveform digital signal to analog signal by configuring the clock and letter number of AD9767 chip[2]. The operational amplifier circuit integrated with the DAC module can adjust the amplitude of the signal within the specified range.

2. Working Principle of DDS Signal Generator

DDS is the abbreviation of digital frequency synthesis. It is a new frequency synthesis technology that realizes signal phase synthesis and control based on the sampled data of the

waveform generated by the system[3]. The following figure is the structural schematic diagram of DDS, which is mainly composed of phase accumulator, phase modulator, waveform look-up table and digital to analog converter[4]. The frequency control word controls the frequency of the synthetic signal. If the system clock is Clk, the frequency control word Fword is M, the phase accumulator bit is N, and the output frequency is $F_{out} = M \times Clk / 2^N$, the phase accumulator completes the accumulation of the frequency control word at the rising edge of each clock and outputs the phase data, realizing the purpose of the frequency control word to control the signal frequency by controlling the phase[5]. The data output by the phase accumulator is the phase of the synthetic signal, and the phase can be used as the address data of the waveform ROM. The ROM stores the quantized value of the waveform sampling data, and uses the result of adding the phase data and the frequency word as the ROM reading address to realize the phase control of the synthesized waveform. The output data of the waveform ROM is transmitted to the digital to analog converter and converted into waveform analog signal output. The schematic diagram of DDS structure is shown in the following figure.

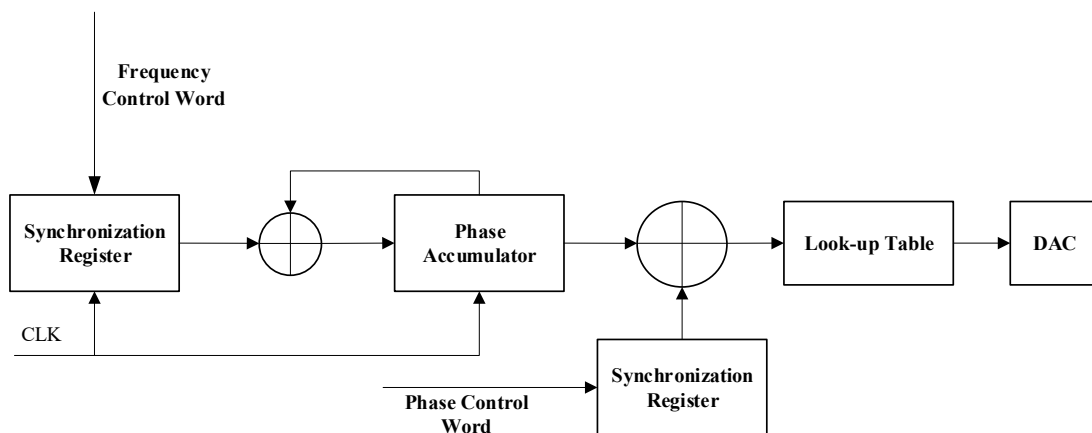


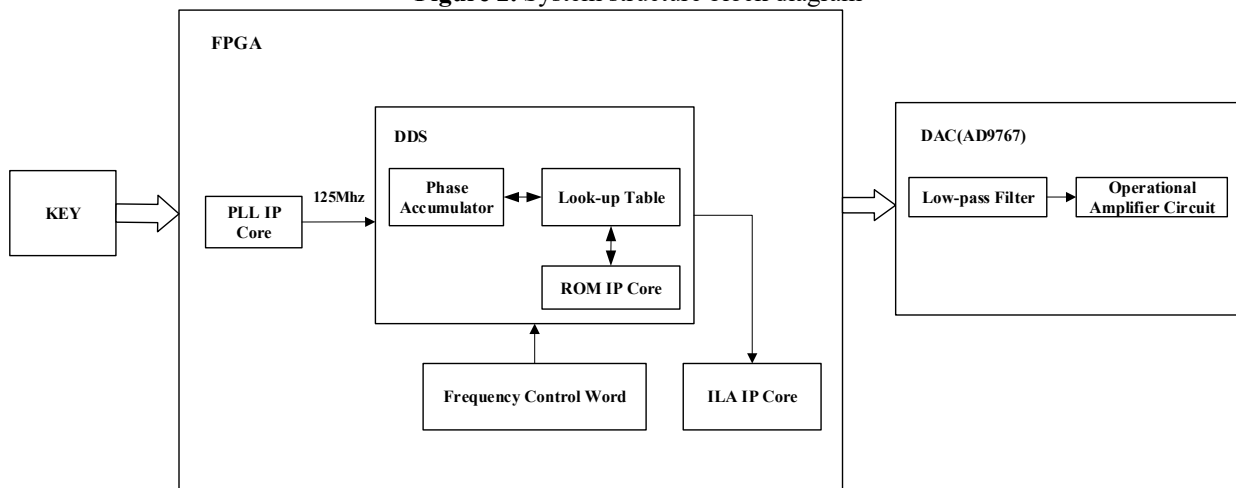
Figure 1. DDS structure schematic diagram

3. Overall Design Scheme

The following figure is the block diagram of DDS signal generator system structure. The system mainly includes key control module, FPGA chip and DAC module. As the system control core, FPGA chip is responsible for the synthesis of multiple frequency sine wave signals and key control. When FPGA detects that the key is pressed, the frequency control word selected by the key is transmitted to the DDS module, and the phase accumulator is responsible for synthesizing the waveform phase of the current frequency. The look-up table

module directly intercepts the upper 12 bits of the 32-bit accumulator result as the read address of the ROM[6], reducing the resource consumption of the ROM. The sinusoidal quantized value of the readout ROM IP from the look-up table is converted into a 14 bit analog signal by the AD9767 chip on the DAC module. The analog signal passes through a low-pass filter and a two-stage operational amplifier circuit to finally obtain a signal with a voltage range of -4V to+4V.

Figure 2. System structure block diagram



4. Hardware Design

4.1. FPGA Development Board

The AX7103 development board of ALINX company is selected as the FPGA development board. This series of development boards adopts the structure of core board and expansion board. The core board is mainly composed of FPGA and two DDR3 and QSPI FLASH, which realizes the function of high-speed data processing and storage of

FPGA[7]. The FPGA chip selects Xilinx's XC7A100T-2FGG484I. Xilinx Artix-7 series chips optimize low power applications that require serial transceivers, high DSP and logical throughput, and provide the lowest total material cost for high-throughput, cost sensitive applications[8]. The expansion board also provides rich hardware resources. The 40 pin expansion port is responsible for the connection with the DAC module, and the keys are responsible for the step control of the frequency. The structure block diagram of the AX7103 development board is shown in the figure below.

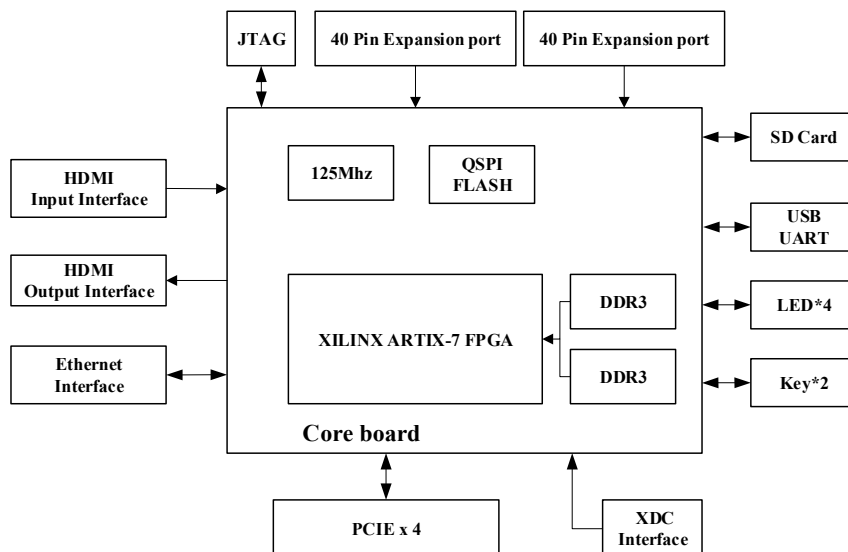


Figure 3. Structure block diagram of AX7103 development board

4.2. DAC Module

The DAC module selects the AN9767 of ALINX company, which supports independent dual channel, 14 bit, 125MSPS digital to analog conversion. ADI's AD9767 chip is a dual port, high-speed, dual channel, 10/12/14 bit CMOS DAC. Each part integrates two high quality TxDAC cores, a voltage reference, and digital interface circuitry into a small 48-lead LQFP, supports an update rate of up to 125 MSPS[9]. The AD9767 chip converts the digital signal into the analog signal, and the low-pass filter filters out the noise beyond the fundamental frequency to obtain a smooth waveform. The operational amplifier circuit on the module can adjust the waveform amplitude, and the final waveform signal is output through the BNC analog output interface. Since the dual channel DA digital input interface is independent, the 125 MHz clock from PLLIP core frequency division can be connected with the clock pin of any channel of AN9767 module and DAC write signal to realize the conversion from digital signal to analog signal. The following figure is the data sequence diagram of AD9767 in dual port mode.

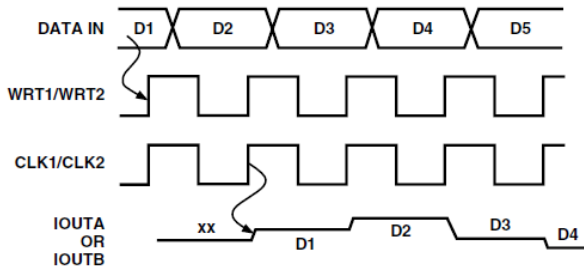


Figure 4. Data sequence diagram of dual port mode

5. Software Design

5.1. FPGA Logic Design

The top module of DDS signal generator project instantiates a PLL IP core (phase locked loop), an ILA IP core (logic analyzer), and a DDS module. The FPGA clock is 200MHz, and the digital to analog conversion rate of the AN9767 module is 125 MSPS, so the program needs to instantiate the PLL IP core to generate a 125MHz drive clock. The instantiated ILA IP core is responsible for capturing key pin signals and 40 pin expansion port signals connected to the DAC module[10]. DDS module is mainly composed of frequency control module, phase accumulator module and lookup table module.

The frequency control module consists of a button control module, a button stabilization module, and a frequency control word module. The button stabilization module adopts the idea of delayed stabilization. When the system detects that a button is pressed, the counter circuit adds 1 to the count value. The program has set corresponding frequency control words for each count value, so when the button is pressed, the frequency control word changes, and the waveform frequency also changes, achieving button control frequency. The DDS module instantiates a single port ROM IP core, and the following diagram shows the structure of the single port ROM IP core. The waveform generator software generates .coe file for sine waves, stores the waveform data file in the instantiated ROM IP core, and waits for the look-up table module to read the sine wave data in the stored waveform memory[11].

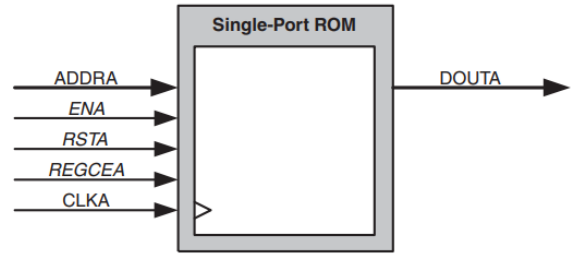


Figure 5. Single-port ROM

The phase accumulator here is a 32-bit adder that adds the frequency control word to the phase data output from the accumulation register to synthesize the phase of the signal. The phase value synthesized by the phase accumulator module is transmitted to the lookup table module, which connects the phase value to the address of the ROM IP core and reads the sine waveform data stored in the ROM.

5.2. Simulation

To reduce the development time of the program, it is necessary to verify the simulation results of Verilog. After the simulation verification is passed, the wiring of the program and the generation of bitstream files are performed, downloading the generated bitstream files to the FPGA development board for board testing[12]. During the research process, Vivado software was used to simulate and verify the software part of this system. The reference clock of the system is 5ns, and the system generates a sine wave with a frequency of 100kHz as shown in the following figure.

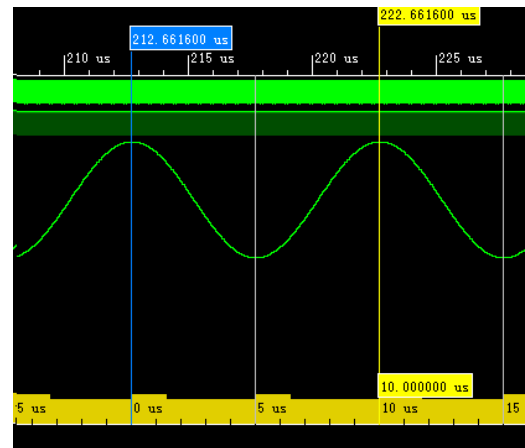


Figure 6. Sine wave with a frequency of 100 kHz

The sine wave period in the above figure is 10μs. The sine wave function simulation with an initial frequency of 100kHz that meets the software design has been passed. The DDS signal generator system has the function of switching the sine wave frequency with a button, and the frequency step of pressing the button is 100kHz. When writing the testbench (incentive file), Verilog was used to simulate the situation of pressing keys. When the simulation button is pressed, the frequency increases by 100 kHz, and the output sine wave frequency changes from 100kHz to 200kHz. The simulation results are shown in the following figure, with a sine wave period of 5μs. Meet simulation requirements.

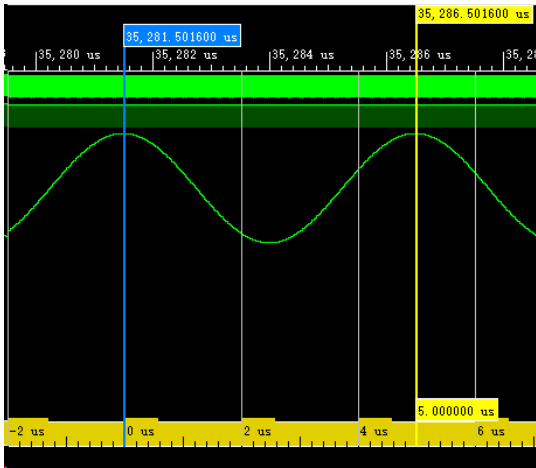


Figure 7. Sine wave with a frequency of 200kHz

6. System Test

The ILA IP core is instantiated in the system code to

capture the signal of the specified pin. Due to the limited amount of data read by the ILA IP core at one time, this test only captures the key input signal and waveform data signal. In the trigger setting part, the falling edge of the key is selected as the trigger condition. In the initial state, the system outputs a sine wave with a frequency of 100 kHz. When the system detects that the key of the development board is pressed, the sine wave frequency steps from 100 kHz to 200 kHz. Every time the key is pressed, the frequency of the output waveform of the development board increases by 100 kHz, and the maximum frequency that can be achieved is 500 kHz. Vivado software can adjust the format of digital signal captured by logic analyzer to analog signal format, which is convenient for observing sine wave analog waveform and debugging. The following figure shows the waveform signal diagram captured by the logic analyzer, which is the sine wave with the frequency of 100 kHz under the initial state and the sine wave with the frequency of 200 kHz after pressing the key.

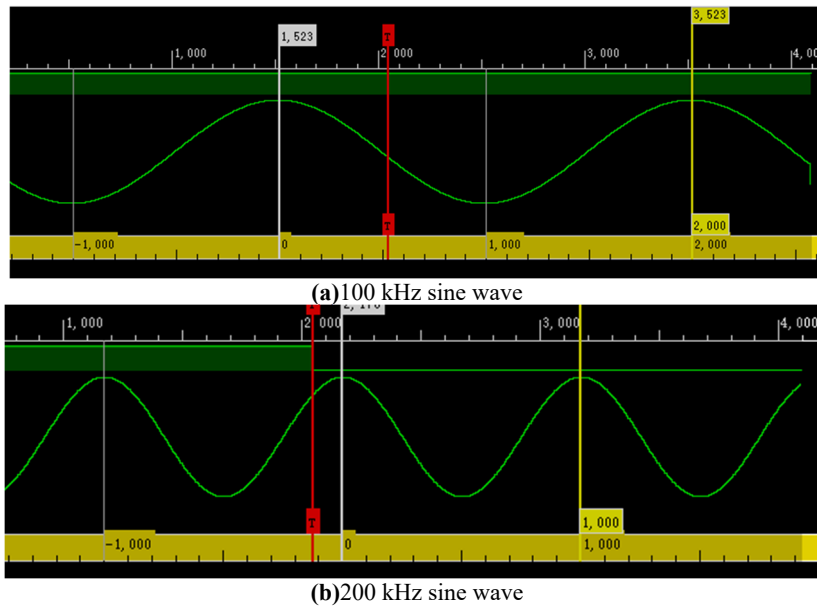


Figure 8. Sine wave signal diagram of 100kHz and 200kHz captured by logic analyzer

According to the further verification of the signal results captured by the logic analyzer, the waveform cycle length in the initial state is 2000 clock cycles. Because the clock frequency of the development board is 200 MHz and the clock cycle is 5ns, the sine waveform cycle is 10 μ s. The period of the initial sine wave corresponding to the frequency of 100kHz. The figure shows that the FPGA detects that the frequency steps to 200kHz after pressing the key, and the cycle length of the new sine wave waveform synthesized by the system is 1000 clock cycles, which is 5 μ s. The corresponding frequency is 200kHz, which meets the design requirements of frequency step 100 kHz.

After the verification and analysis of FPGA development board online logic analyzer is completed, the signal generator experimental environment is built. Connect the DAC module to the FPGA development board, and the signal output end of the DAC module is connected to the oscilloscope through the BNC signal test line[13]. After the hardware connection check is correct, power on and download the bit stream file generated by Vivado to the FPGA chip through the JTAG interface. In the initial state of the system, the oscilloscope displays a 100 kHz sine waveform. The system detects that

the key is pressed and the frequency step is 100kHz. Press the key for 4 times in this experiment, and the sine wave frequency ranges from 100 kHz to 500 kHz. The following figure shows the sine wave with frequencies of 100 kHz and 500 kHz on the oscilloscope.

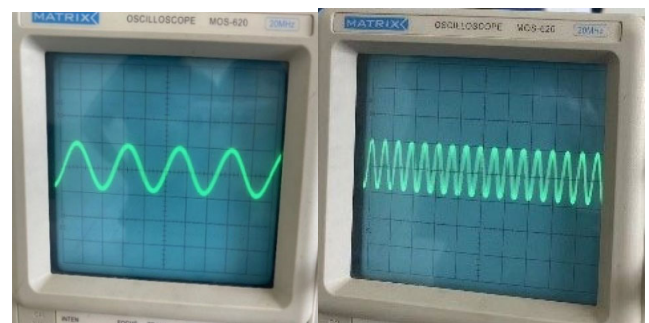


Figure 9. Sine wave waveform signal with frequency of 100kHz and 500kHz collected by oscilloscope

7. Conclusion

This paper designs a DDS signal generator based on FPGA, which is used to generate sine wave signals with multiple frequencies and adjustable amplitude[14]. It has the advantages of simple structure, easy debugging, stability, reliability, small size, etc. The test results show that the system can output sine wave signal with a frequency of 100kHz-500 kHz stably, and the amplitude of the signal can be adjusted from -4 v to+4 v. The expansion version of FPGA development board reserves data transmission interfaces such as gigabit network, UART and PCIE, which can meet the data transmission of the system in most scenarios. In the next step, we will continue to increase the types of synthetic signals of DDS signal generator, increase the adjustable range of synthetic waveform, and plan to add high-speed data interfaces such as gigabit network to meet the high-speed data interaction with PC[15].

References

- [1] Hao D. Research on DDS-based Portable Signal Generation Testing Device[C]//Journal of Physics: Conference Series. IOP Publishing, 2021, 1971(1): 012001.
- [2] Lei H, Gao G, Huang Y. Design and Simulation of Multi-modal Signal Generator[C]//2020 7th International Conference on Information Science and Control Engineering (ICISCE). IEEE, 2020: 2366-2369.
- [3] Tierney. A Digital frequency synthesizer [J]. IEEE Trans AEV, 1971, 19(1) :48-57
- [4] Vankka J. Digital frequency synthesizer/modulator for continuous-phase modulations with slow frequency hopping[J]. IEEE transactions on vehicular technology, 1997, 46(4): 933-940.
- [5] Bommi R M, Raja S S. High Performance Reversible Direct Data Synthesizer for Radio Frequency Applications[J]. Mobile Networks and Applications, 2019, 24(1): 224-233.
- [6] Dangui Y, Ruijun T, Min X, et al. An optimal method for costas loop design based on FPGA[C]//2013 Fourth International Conference on Digital Manufacturing & Automation. IEEE, 2013: 175-179.
- [7] Kuang L, Zeng J, Georgiou P. High-throughput digital readout system for real-time ion imaging using CMOS ISFET arrays[C]//2020 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2020: 1-5.
- [8] Xilinx, Inc. 7 Series FPGAs Data Sheet: Overview[J/OL]. 2020.09. www.xilinx.com
- [9] Analog Device Inc.Data Sheet: AD9763/AD9765/AD9767 10-/12-/14-Bit, 125 MSPS Dual TxDAC+ Digital-to-Analog Converters, 2009.
- [10] Zhang L, Zhang Y, Shang Z, et al. A generation and distribution system of clock signal source for signal acquisition system[J]. Engineering Reports, 2022, 4(6): e12494.
- [11] Liu Z. Design of typical waveform generator based on DDS/SOPC[C]//Proceedings 2013 International Conference on Mechatronic Sciences, Electric Engineering and Computer (MEC). IEEE, 2013: 642-645.
- [12] Muralikrishna B, Madhumati G L, Khan H, et al. Reconfigurable System-on-Chip design using FPGA[C]//2014 2nd International Conference on Devices, Circuits and Systems (ICDCS). IEEE, 2014: 1-6.
- [13] Woo M K. Frequency synthesizer requirements for future cellular radio systems (06-026)[J]. 2006.
- [14] Zhao Z, Wang L, Chen J, et al. The design and implementation of signal generator based on DDS[C]//2017 IEEE 9th International Conference on Communication Software and Networks (ICCSN). IEEE, 2017: 920-923.
- [15] Tummala R R, Laskar J. Gigabit wireless: System-on-a-package technology[J]. Proceedings of the IEEE, 2004, 92(2): 376-387.