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Research on Low Power BIST Based on LFSR Reseeding

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Abstract: With the increasing scale and complexity of the internal circuit, the function of the chip is more powerful, but it will bring serious problems to the test of the chip. The internal power consumption of the chip in the test mode is much higher than that in the normal working mode, especially in the process of built-in self-test, the excessive power consumption will damage the circuit under test and lead to the failure of the chip. The low power test vector generation technology reduces the test power by preprocessing the test vector set. However, the modification of the test vector set results in the low failure coverage in the test process. LFSR replaying technology is a common method of generating test vectors in built-in self-test. It can improve the coverage of test faults by loading test vector seeds into linear feedback shift register. However, while improving the fault coverage, the technology will generate high test power consumption in the circuit under test. In design for testability (DFT), it is a hot topic to generate low-power test vectors by combining LFSR reseeding technology with low-power test vector generation technology. Aiming at the problem of high power consumption caused by test vectors in built-in self-test, this paper proposes a low power test vector generation method based on LFSR reseeding. On the basis of studying the influence of test vector on dynamic test power consumption, the linear correlation between test vector seed and test vector is analyzed deeply. A model of dynamic test power consumption optimization based on Hamming distance sorting test vector seed is proposed to realize the design of low-power test vector seed generation algorithm. Combined with LFSR reseeding technology, a low-power test vector generator based on test vector seed sorting is designed. The simulation design of test vector generator is based on ISCAS85 and ISCAS89. The experimental results show that the total number of test vector seed storage bits is reduced by 64.39%, the average fault coverage is 97.42%, the average area overhead is 4.32%, and the dynamic test power consumption is reduced by 44.21%. Compared with other schemes, the proposed low-power test vector generation technology based on LFSR reseeding has some comprehensive advantages in reducing the number of seed storage bits, improving fault coverage, reducing circuit area overhead and reducing power consumption.

Keywords: Test vector seed reordering, LFSR reseeding technology, Test vector generation, Low power consumption, BIST, Test response analysis.

1. Introduction

The development of chip is inseparable from the progress of integrated circuit technology. Now the integrated circuit has entered the stage of very large scale integrated circuit (VISL). From the 180nm process of the Pentium 4 processor to the 7 nm chip process that Intel is breaking through, the exponential growth of semiconductor processes confirms Gordon Moore's prediction of Moore's law. The research and development of high performance chip provides powerful power and technological guarantee for the development of social science and technology. The chip has also begun to enter the era of system-on-chip. System-on-chip (SoC) refers to the integration of microcontroller, analog circuit, digital circuit, memory circuit and peripheral interface circuit in the system on chip. By means of integrating and reusing IP kernel, the design cycle of chip products is shortened, so that the chip can enter the consumer electronics market faster.

The increase of circuit size brings the increase of test vectors, and when the test vectors with low correlation are loaded into the circuit under test, the power consumption will increase. At the same time, In order to avoid the excessive dependence of Automatic Test Equipment (ATE) for chip testing, the technology of Built In Self Test (BIST) is gradually developed. Built in Self Test (BIST) is a kind of test vector that can be generated. Input to the Circuit Under Test (CUT), collect the input response, and verify the correct hardware circuit structure of the output result. BIST also has many advantages: reduced testing costs, improved error coverage, reduced testing time, the ability to test independently, etc. BIST is an effective method to solve the System On Chip (SOC) test problem, which has become a new research hotspot in the field of circuit test technology.

2. Methodology

2.1. Overall framework of built-in self test

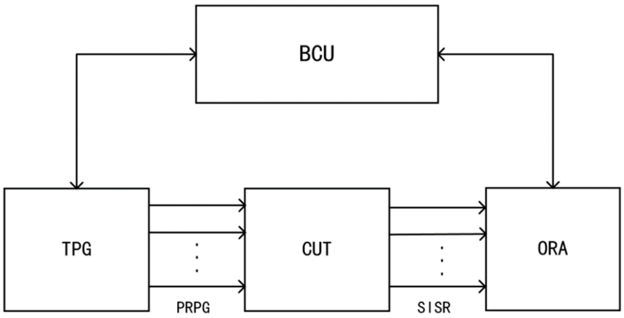


Figure 1. Diagram of the BIST structure

As shown in Figure 1, there are three main modules around the circuit under test (CUT) :

1.Test Vector Generator (TPG): Test generation and application module. During the built-in self-test, the test vector generator connected to the circuit under test outputs test vectors to provide test vectors for the circuit under test. The generation of the test vector is the process of detecting the fault with the test vector inside the circuit according to the given fault of the circuit under test. There are two issues to ensure: one is to ensure that the fault can be reproduced inside the circuit under test, and the other is to propagate the fault to the output of the circuit under test, that is, to make the source of the fault in the circuit can be effectively presented. In the process of chip testability design, the test vector generator is the main hardware circuit module, the main research content of this paper is this module.

2. Output Response Analyzer (ORA): A test response capture/qualification module that captures, compresses and analyzes test responses to determine the correctness of the circuit under test.

3. Built-in self-test control unit (BCU): It is the central processing unit of all BIST operations, controls self-test scheduling and determines the working mode of the above two modules, controls TPG to generate test data and input it to the circuit under test, and then sends the response to TAE et al. By accessing the BIST controller, the test results can be read out to complete the test of the circuit under test.

Built-in self-test total state transition: In the process of chip built-in self-test, it includes S0, S1, S2, S3, S4, S5, a total of 6 states. S0: initial test state; S1: seed generation state; S2: vector expansion state; S3: scan loading state; S4: circuit test state; S5: response analysis state. When the seeding of a test vector is completed, it returns to the S0 state.

2.2. Test vector generation

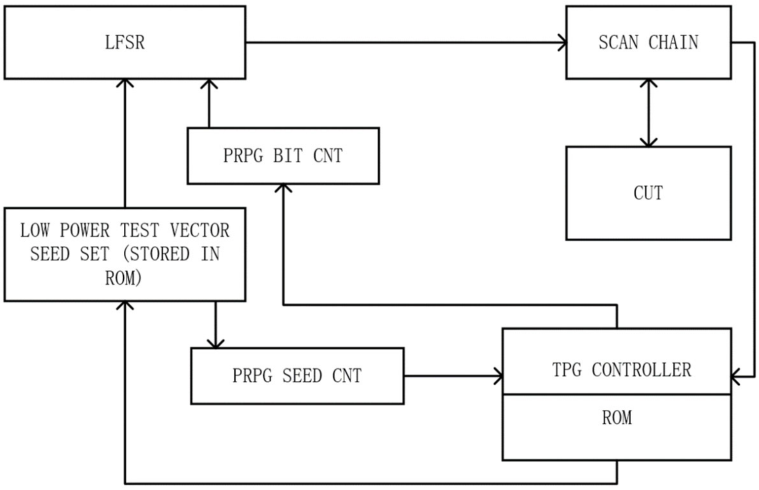


Figure 2. Test Vector Generator (TPG) structure diagram

1. Structure of Test Vector Generator (TPG):

Workflow: There is no need to change the test vector seed during the chip testing process, only the test data needs to be stored in Read Only Memory (ROM), which has the advantages of stable data storage and no loss of power-down information. Here, the IP Core inside Quartus is used to generate a ROM memory whose depth is the total number of test vector seeds and the bit width is the test seed bit width. After the ROM is generated, the MIF file is initially generated, and the encoded test vector seeds are written in the MIF file in sequence. When the chip performs the built-in self-test, the read pointer of the ROM test vector seed is in the form of binary code, and the number of calls of the read pointer is counted by a counter. When the count of the test vector seed counter is the number of test vector seeds, Then it is judged that the test vector seeds in the ROM have all been read once. With the clock cycle of the chip test, under the action of the control signal of the ROM controller, it is called in the specified order and input to the LFSR. Move each bit of the test vector unrolled in the LFSR into the scan chain until the test vector bit counter counts to the number of test vector bits, load the complete test vector into the circuit under test, and then test it. When the vector generation controller detects the feedback signal in the scan chain, that is, there is no test vector in the scan chain, the working signal is enabled for the LFSR, and each bit of the next test seed is loaded into the scan in turn. When the test vector seed counter reaches the maximum value of the test seed set, it means that all the test vector seeds in the ROM have been sown once, and wait for the second external work enable signal.

2. Select the generation method of the BIST test vector:

Traditional test vector generation techniques mainly include exhaustive testing, deterministic testing and pseudo-random testing. The test vectors generated by the exhaustive test and the deterministic test can be stored in the ROM directly as the test vector generation module of the BIST. At present, the deterministic test generally uses the automatic test vector generation tool ATPG to generate the deterministic test vector set. Pseudo-random test sequences can be generated using LFSR, which uses very little hardware and is highly cost-effective. However, due to the existence of anti-random circuit faults during actual testing, it is difficult for pseudo-random test vectors to detect anti-random faults. Therefore, only relying on pseudo-random testing cannot complete the fault detection of the test circuit. Deterministic vectors need to be generated during built-in self-test to achieve high test fault coverage.

The vector generation method used in this paper is the deterministic test vector generation method, and the test vector set used is the deterministic test vector set generated by ATPG.

3. Realize the generation of low-power test vector seeds:

The power consumption of CMOS circuits comes from three aspects: leakage current power consumption, DC short-circuit current power consumption, and dynamic switching power consumption. Leakage current power consumption is largely determined by the manufacturing process in which the chip is produced. The DC short-circuit power consumption can be solved from the device characteristics. Dynamic switching power consumption is the main component of chip power consumption, and the dynamic power consumption of circuit nodes mainly depends on the switching activity factor WSA. WSA is mainly affected by the number of transitions of the circuit nodes. Reducing the number of high-low transitions of the internal nodes of the circuit under test can effectively reduce the test power consumption. The internal data of the chip is related when it is working normally, so the power consumption of the chip is not very high when it is working normally. However, the test vectors used for the built-in self-test of the chip are generated by ATPG and have extremely low correlation, which will lead to frequent switching of the internal nodes of the circuit during the test, and exceed the normal working mode. Therefore, the test vectors are sorted according to the Hamming distance, and the loading order between the vectors is changed to minimize the number of internal flips of the circuit under test, thereby optimizing the test power consumption.

Main idea:

Combines LFSR reseeding technique and low power test pattern generation technique. First, use LFSR to encode the original test vector into a vector seed set, and then use the low-power test vector generation technology to encode the vector seed set into a low-power test vector seed set, and finally store the low-power test vector seed set in ROM. (Sort the vector seeds based on the Hamming distance, the algorithm is shown in Figure 3 below). During testing, the test vector seeds are expanded into low-power test vectors and loaded into the circuit under test, and the test fault coverage is improved by repeated seeding of the test vector seeds, which not only ensures high fault coverage of chip detection, but also reduces the dynamic power consumption in the test.

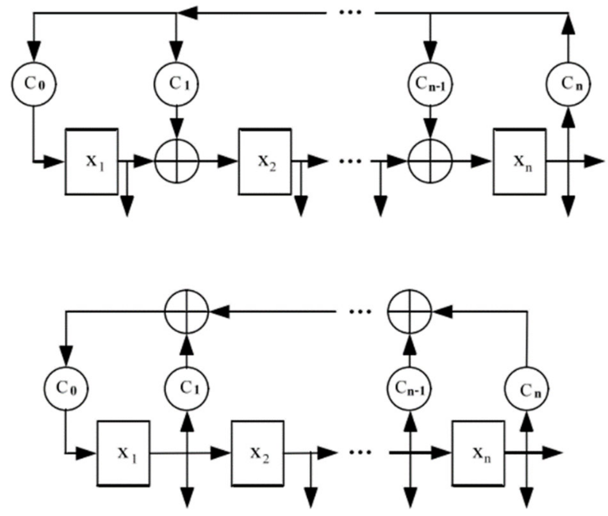


Figure. 3

Advantages of Low Power LFSR Reseeding Technology: All test vector sets can be encoded to meet the requirements of low-power test vector seed sorting; The low-power test vector generator based on the LFSR test vector reseeding technology only needs to decode the controller logic to control the XOR network to select the LFSR structure, the required hardware structure is simple, and the control logic is easy to implement; During the test process, the low-power test vector is repeatedly seeded to the circuit under test through LFSR, which reduces the test power consumption while improving the fault coverage rate, and balances the test power consumption and the test fault coverage rate.

2.3. Test Response Analysis

Test response analysis generally includes ROM storage-based deterministic testing and response compression methods. Since each expected test response result needs to be stored in the ROM memory, the silicon chip overhead is increased to a large extent. In order to reduce the test cost and time, test compression is introduced.

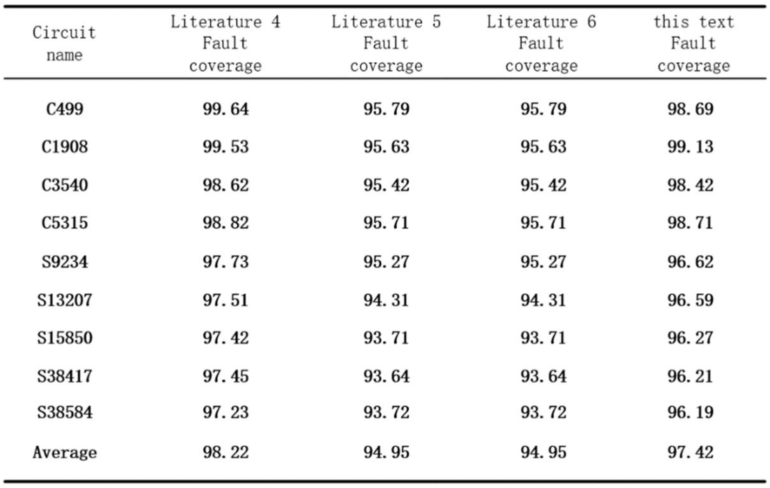
Feature analysis is a compression technique based on LFSR. The characteristic analysis method to realize the test response compression has the advantages of small aliasing probability and independent from the output response, simple structure design, low hardware cost, and can carry out multi-output analysis at the same time, which has great advantages over other methods.

The compression-based testing process first obtains the correct compression response through a fault-free good board simulation, called the Golden Signature. During the test, the test response of the circuit under test is compressed by the same mechanism, and the obtained features are compared with the good board features. If the obtained features are the same as the good board features, the CUT is considered to be a fault-free circuit, otherwise it is a faulty circuit.

3. Results and Discussion

3.1. Data Analysis of Test Vector Generation Module

According to the test vector seed generation algorithm based on Hamming distance reordering proposed in the second chapter of this paper, some circuits of ISCAS85 and ISCAS89 in the international benchmark circuit set are used for experiments. The experimental circuit generates the original test vector set through ATPG, encodes it into test vector seeds through LFSR, and stores the test vector seeds reordered based on Hamming distance into ROM for storage. The LFSR reseeding technique can improve the fault coverage of the test by repeatedly seeding the test vector seeds. Through experiments on some circuits of ISCAS85 and ISCAS89, the fault coverage rate of deterministic faults generated by low-power test vectors is calculated and compared with other methods, as shown in Figure 4.



Circuit name	Literature 4 Fault coverage	Literature 5 Fault coverage	Literature 6 Fault coverage	this text Fault coverage
C499	99.64	95.79	95.79	98.69
C1908	99.53	95.63	95.63	99.13
C3540	98.62	95.42	95.42	98.42
C5315	98.82	95.71	95.71	98.71
S9234	97.73	95.27	95.27	96.62
S13207	97.51	94.31	94.31	96.59
S15850	97.42	93.71	93.71	96.27
S38417	97.45	93.64	93.64	96.21
S38584	97.23	93.72	93.72	96.19
Average	98.22	94.95	94.95	97.42

Figure 4. Fault coverage comparison table

After the test vector is generated for the C499 circuit, the power consumption analysis is carried out, and the power consumption analysis report is shown in Figure 5. According to the power analysis report, the leakage power consumption of C499 designed for testability is 4.8733 μW, the short-circuit power consumption is 104.1798 μW, the internal power consumption is 104.1798 μW, the switching power consumption is 411.3177 μW, and the total dynamic power consumption is 520.3648 μW. Among them, the leakage power Leakage Power is the circuit power consumption when the circuit is not working, so it is generally not affected by the working state and frequency. It can also be seen from the report that switching power consumption is the main power consumption in dynamic power consumption, and needs to be paid attention to during the chip testing process.

```
****************************************
Report : power
        -analysis_effort low
Design : c499
Version: K-2015.06
Date   : Sun Dec 16 15:40:26 2022
****************************************
Library(s) Used:

    fast (File: /opt/Foundary_Library/TSMC90/aci/sc-x/synopsys/fast.db)
    gtech (File: /opt/Synopsys/Synplify2015/libraries/syn/gtech.db)
Operating Conditions: fast   Library: fast
Wire Load Model Mode: top
Global Operating Voltage = 1.1
Power-specific unit information :
Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW
  Cell Leakage Power   =   4.8733 uW

  Cell Internal Power  = 104.1798 uW  (100%)

  Net Switching Power  = 411.3117 uW  (100%)

Total Dynamic Power    = 520.3648 uW  (100%)
```

Figure 5. Power Analysis Report

3.2. Experimental simulation analysis of test response comparison module

The C499 circuit can be regarded as an 8-bit traveling wave carry adder, and its BIST logic synthesis waveform simulation is shown in Figure 6. After 8 clock cycles, test the output of the adder once, and analyze the test result according to the value of pass. If there is no fault in this circuit, the result will output 1, and if there is a fault, it will output 0. When the value of the finish signal is 1, it represents the end of the test. If there is a failure, the value of finish remains unchanged at 0. Analysis of Figure 5-13 shows that the logic simulation generated by the adder correctly proves the generated test code, and the logic simulation results of the feature analysis are reasonable. The waveform simulation characteristics obtained by the test are compact and orderly, which proves that the BIST control rationality.

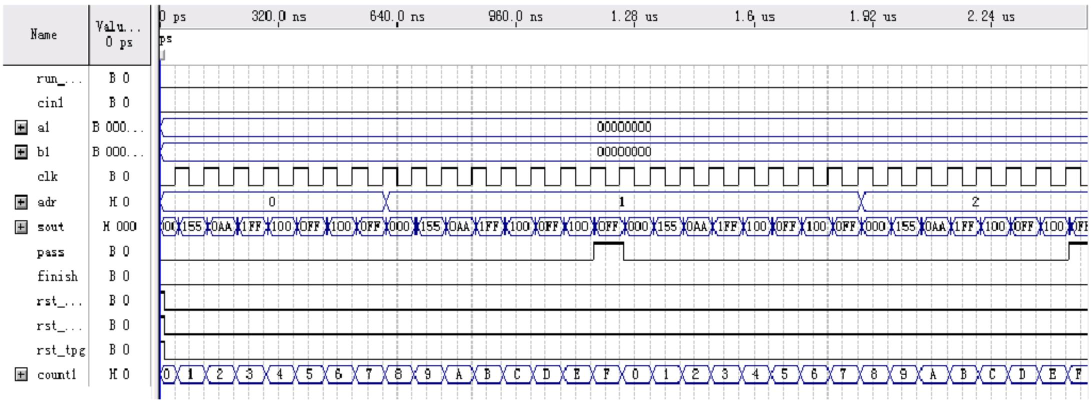


Figure 6. Logic synthesis waveform simulation

4. Conclusion

This paper analyzes the development trend of BIST test technology, and introduces the research status of LFSR reseeding technology and low-power test vector generation technology. Reducing the power consumption of chip testing by generating low-power test vectors is an important goal of chip testability design and the main research direction in the field of chip testing. This paper mainly introduces the low-power test vector generation technology, the principle of LFSR reseeding technology and the structure principle of built-in self-test. The main work of the article is as follows:

By studying the influence of the loading of the test vector inside the circuit under test on the dynamic test power consumption, the relationship between the test vector and the test vector seed in the LFSR reseeding technology is analyzed, and it is concluded that the test vector seed and the test vector have a linear correlation characteristic. A model for optimizing dynamic test power consumption based on Hamming distance sorting test vector seeds is proposed to realize the design of a low-power test vector seed generation algorithm.

The middle part of ISCAS85 and ISCAS89 circuits are selected for low-power test vector generator simulation design experiment. The method proposed in this paper reduces the total number of test vector seed storage bits by 64.39% on average, the test vector generation fault coverage rate is 97.42%, the circuit area overhead is 4.32%, and the dynamic test power consumption is reduced by 44.21% on average, achieving a low-power test vector generated request. Compared with other LFSR reseeding methods, the method proposed in this paper has certain advantages in reducing the number of test vector seed storage bits, reducing the circuit area overhead of the test vector generator, and reducing the dynamic test power consumption.

The C499 circuit is selected to build a BIST circuit, and the results are tested and compared through feature analysis, and the comparison information between the test response and the correct response is obtained, thereby proving the effectiveness of the BIST.

Acknowledgment

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