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Design of MoO_3 Porous Back Contact for High Efficiency CZTSSe Thin-film Solar Cells

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Abstract: The introduction of in-situ anodized MoO_3 porous arrays with tailored structural parameters as the rear interface contact has a positive impact on enhancing the solar cell performance. The optimized device efficiency increased from 6.31% to 9.00% (in reference to molybdenum-based cells), resulting in a 32% increase in J_{SC} and a 64% increase in FF. The results indicate that at a 10V oxidation voltage, the MoO_3 pore size is relatively larger, facilitating the formation of a well-interpenetrating structure and contact interface with CZTSSe. In turn, assists in carrier interface separation and transfer, effectively suppressing the recombination of separated carriers. It extends carrier lifetime, reduces band tailing effects, and lowers urbach energy, thus improving the overall performance of CZTSSe devices.

Keywords: $Cu_2ZnSn(S, Se)_4$; Porous MoO_3arrays; Anodization; Back Contact; Device.

1. Introduction

KesteriteCuZnSn(S,Se)$_4$ (CZTSSe) based thin-film solar cells exhibit a Shickley-Quiesser limit efficiency exceeding 30% [1] due to their easily tunable bandgap (1.0-1.5 eV), high absorption coefficient (>10^4 cm^{-1}), abundant and non-toxic chemical composition[2-6], making them one of the most promising photovoltaic materials. However, the current record efficiency achieved for CZTSSe solar cell devices is only 14.9% [7], significantly lower than its theoretical conversion efficiency of 32.4% [8] and the highest recorded PCE of 23.4% for CIGSe thin-film solar cells [9]. There is ample potential for enhancing the device's performance, with significant scope for improvement. Extensive research has revealed that a significant open-circuit voltage (V_{OC}) deficit is a critical factor limiting the performance of CZTSSe solar cells. In addition to various defects within the CZTSSe absorption layer and suboptimal interfaces, the primary reasons for the high V_{OC} deficit include the front interface between CZTSSe and the buffer layer and the rear interface between CZTSSe and Mo [10-13]. To address these interface issues, various strategies have been proposed to fabricate efficient CZTSSe cells.

In the context of selenium selenization, when considering back contact we cannot overlook the carrier recombination occurring at the CZTSSe/$MoSe_2$ interface. This is not only because the high barrier at the back electrode inhibits effective hole transport to the Mo back electrode[14,15], but also due to severe recombination caused by the mismatched band alignment, secondary phases (such as Cu_2(S,Se), Zn(S,Se), Sn(S,Se), Mo(S,Se)$_2$), and non-uniform distribution of S or Se[13,16,17].

To address these issues in CZTSSe solar cells, current solutions primarily include the following: introducing high work-function ultrathin interlayer (IL) materials between CZTSSe and the molybdenum back electrode, such as TaN[18], TiN[19], TiB_2[20], MoO_x[21-26], ZnO[27,28], Al_2O_3[29,30], CuSe[16], GeO_2[31], Bi[32], Ag[33-35], graphene oxide[36], and transforming n-type $MoSe_2$ into p-type $MoSe_2$ through element doping, such as $MoSe_2$: Nb[37,38] and Mo(Se_{1-x},O_x)$_2$[39,40]. In fact, these methods are indeed effective in enhancing the open-circuit voltage (V_{OC}) and improving the overall performance of CZTSSe solar cells, However, even so, significant improvements in the device's overall performance are still limited.

In the case of an n-type material, an intrinsic electric field is formed at the n-IL/p-CZTSSe interface, hindering the movement of electrons towards the IL, this leads to an increase in carrier recombination and acts as an obstacle to holes entering the Mo back electrode. To promote carrier collection in the back interface region, a built-in back interface field should be established to reduce the energy barrier for carriers' transit.

Based on the above analysis, the insertion of a high work-function p-type hole-conductive material, MoO_3, between CZTSSe (or Cu_2ZnSnS_4, CZTS) and the Mo back electrode, can establish an interface field to expedite carrier separation. Currently, there are several methods for introducing a MoO_3 interface layer, including high-temperature annealing of the Mo electrode in a N_2atmosphere[22,23,41], magnetron sputtering[25], thermal evaporation[24,42], and spin-coating[43]. However, there is limited research on the correlation between the microstructure of MoO_3 and device performance, which could be a crucial factor influencing the quality and performance of photovoltaic device interfaces. Currently, there are no reported works related to this aspect.

This study investigates the novel use of anodization to in-situ introduce a porous MoO_3 array structure as a back interface contact, providing a detailed elucidation of the impact of MoO_3 microstructure under different oxidation times on CZTSSe photovoltaic devices. A porous, interpenetrating structure is anticipated at the interface between p-type CZTSSe and high work-function p-type MoO_3, aiming to achieve the following synergistic effects: i) Formation of a well-defined interface field to facilitate effective carrier separation. ii) Increase in the interface contact area, prolonging the light propagation path through porous scattering. iii) Acceleration of carrier collection along the pore walls toward the Mo back electrode. The study reveals a close correlation between device performance and the microstructure of MoO_3, with these synergistic effects collectively enhancing the energy conversion efficiency

(PCE), open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}), and fill factor (FF) of CZTSSe devices. The highest efficiency achieved for CZTSSe devices is 9.00%, with a short-circuit current density (J_{SC}) of 33.63 mA/cm^2. This represents a substantial improvement over untreated molybdenum-based CZTSSe solar cells (PCE=6.31%, J_{SC}=25.49 mA/cm^2), with a notable increase of 43% in PCE and 32% in J_{SC}, while V_{OC} also improved from 416 mV to 422 mV. Of course, further improvements in device efficiency can be achieved through optimization of other device assembly conditions. This study provides a novel approach for the design of back interface contacts in high-efficiency CZTSSe solar cells.

2. Experimental Section

2.1. Preparing MoO_3 Porous Arrays on a Mo Substrate

Porous structured MoO_3 arrays were meticulously crafted through direct anodic oxidation of the Mo back electrode on soda-lime glass (SLG). Initially, the pre-cleaned Mo-coated SLG (2×2.5 cm) underwent anodization in an ethylene glycol electrolyte solution comprising 0.5% NH_4F and 3 vol% deionized water at 0°C, applying a voltage range of 5–10 V, and oxidation time of 7 minutes. This method yielded porous MoO_3 arrays with diverse pore sizes and thicknesses on the Mo back electrode. The resulting material, characterized by a layer of porous structured MoO_3 arrays on anodized Mo, was designated as A-Mo. For comparison, planar-structured MoO_3 on Mo substrates were prepared by direct annealing in N_2 for 10 minutes.

2.2. Fabrication of CZTSSe-based Photovoltaic Devices

In summary, the preparation of Cu_2ZnSnS_4 (CZTS) precursor solution involved the sequential addition of CuCl (99.95%, Aladdin), $SnCl_2$ (99.99%, Aladdin), CH_4N_2S (99.0%, Aladdin), and $ZnCl_2$ (99.95%, Aladdin) into dimethyl sulfoxide (DMSO) (99.95%, Aladdin) under continuous stirring at room temperature until the solution achieved a clear bright yellow appearance. Subsequently, the A-Mo samples were immersed in the precursor solution to allow CZTS to infiltrate the MoO_3 pores. The CZTS precursor solution was then spin-coated onto the samples to form CZTS precursor films. The spin coating process involved a rotation speed of 2900 rpm, a rotation time of 20 seconds, and each film was heat-treated at 320 °C on a hot plate for 2 minutes in an air environment after each coating. This spin coating process was repeated 9 times, which was determined to be the optimal number of repetitions for this study.

The CZTS precursor films, along with selenium (Se) particles, were placed into a sealed graphite box and selenized at 560 °C for 30 minutes in a rapid heating furnace under a flow of nitrogen (N_2) protection to produce CZTSSeabsorbed layer. Finally, a CdS buffer layer of approximately 40 nm, a ZnO layer of about 30 nm, and an indium tin oxide (ITO) window layer of around 200 nm were sequentially deposited onto the CZTSSeabsorbed layer using chemical bath deposition, radio frequency (RF) magnetron sputtering, direct current (DC) magnetron sputtering, and evaporation techniques to complete the device fabrication. For reference, similar devices were assembled using untreated Mo and planar-structured MoO_3 substrates, following the same fabrication processes as described above. No anti-reflection layer was utilized during the device assembly. The total cell area of the final devices was 0.11 cm^2, defined by mechanical scribing.

2.3. Characterizations

X-ray diffraction (XRD) patterns were acquired using a Bruker D/max2400 X-ray diffractometer with Cu Kα radiation (λ=0.1540576 nm). Microstructural examination was conducted via JSM-6701F field emission scanning electron microscopy (FESEM). Capacitance spectroscopy (C–V), with a frequency of 50 kHz, sweeping range from 0.8 to 0.4 V, and a scan interval of 0.01 V, as well as electrochemical impedance spectroscopy (EIS) with a bias voltage of 0 V and a frequency range of 10–10^{5}Hz, were analyzed using an Autolab PGSTAT 302 N (MetrohmAutolab BV) under dark conditions.

The current density-voltage (J-V) characteristic curves were measured employing a Keithley 4200 source meter under standard AM1.5G irradiation from an AAA solar simulator (Newport-94023A), calibrated with a standard Si reference cell (Newport-91150). External quantum efficiency (EQE) of the cells was characterized using a Newport EQE system equipped with Si and Ge diodes as reference detectors.

3. Results and Discussions

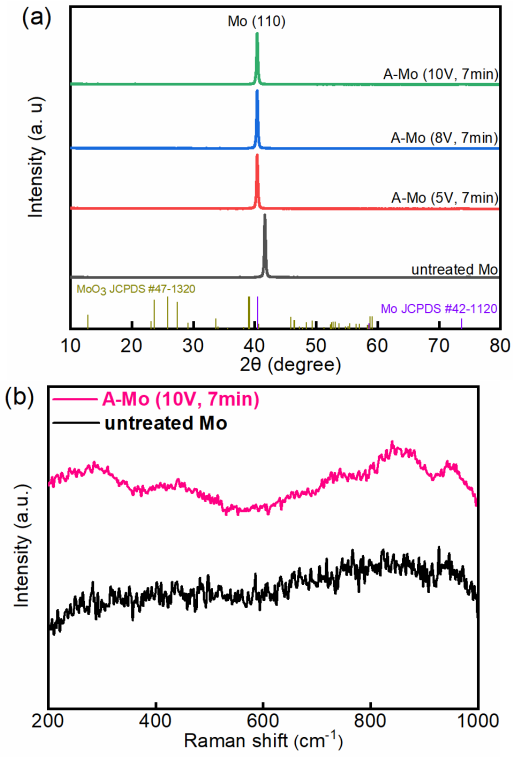

Fig 1. (a) XRD spectra of untreated Mo and Mo oxidized at different oxidation voltages. (b) Raman spectra of untreated Mo and Mo treated under conditions of 10V for 7 minutes.

The Mo samples oxidized at different oxidation voltages and untreated Mo samples were subjected to XRD (X-ray diffraction) testing. As shown in Fig. 1a, the XRD spectra indicate that, when compared to the Mo and MoO_3 standard reference data, the diffraction peaks can be attributed to Mo. However, the intensity of the diffraction peaks decreases with an increase in the oxidation voltage. This observation suggests that the thickness of the underlying molybdenum decreases, while the thickness of oxidized molybdenum increases. The reason why the oxidized samples do not exhibit

a pronounced presence in the XRD spectrum is because the oxidation voltage falls within a low voltage range, which is insufficient to promote the crystallization of molybdenum oxide. The relatively poor crystallinity of molybdenum oxide prevents its diffraction peaks from appearing in the XRD spectrum. Thus, to further determine the composition of samples oxidized at different voltages on the Mo substrate, we conducted Raman analysis on both the untreated Mo and the oxidized A-Mo (10 V, 7 min) samples, as shown in Fig. 1b, the Raman peaks observed in the oxidized samples correspond to MoO_3, indicating that the oxidized A-Mo samples are composed of MoO_3.

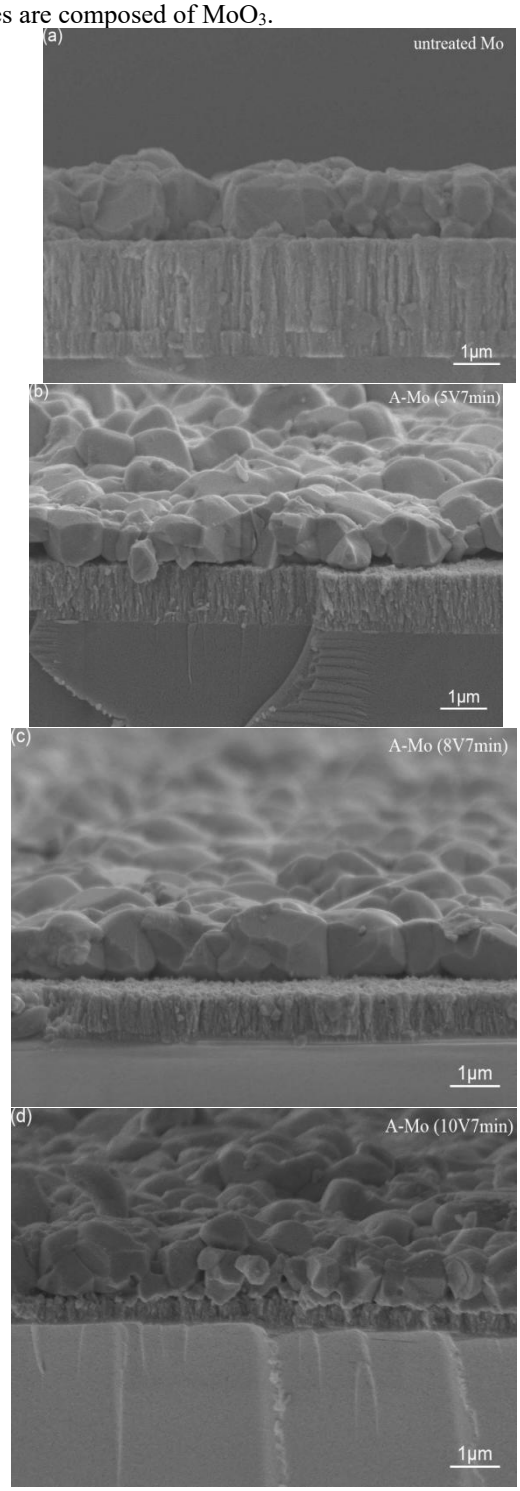

Fig 2. Cross-sectional SEM images of untreated Mo and anodized A-Mo samples. (a) Cross-sectional morphology of untreated Mo. Cross-sectional morphology of samples anodized under the following conditions: (b) 5 V, 7 min; (c) 8 V, 7 min; (d) 10 V, 7 min.

Fig. 2a-d depict the cross-sectional morphology of untreated Mo samples and A-Mo samples subjected to different anodic oxidation voltages (5 V, 8 V, 10 V) for 7 min. Fig. 2a reveals the cross-sectional morphology of the untreated Mo sample, displaying a striped arrangement structure. Meanwhile, a distinct interface between $MoSe_2$ and Mo is clearly observed on the back electrode. However, Fig. 2b-d intuitively demonstrate that in the A-Mo sample, there is no apparent stratification of $MoSe_2$ and Mo, as observed in untreated Mo. Simultaneously, a dense array of pore-like protrusions is notably observed at the interface between the back electrode and the absorbed layer, further confirming the formation of a porous array structure after anodic oxidation. Moreover, with an increase in the oxidation voltage, a noticeable reduction in the thickness of the back electrode is observed. When the oxidation voltage is set at 10 V, the back electrode in A-Mo (10 V, 7 min) reaches its minimum thickness. This suggests the formation of fewer $MoSe_2$, and the synergistic effects of a lower work function MoO_3 in contact with Mo, as well as the reduced thickness of the back electrode, which collectively favor the collection of photogenerated charge carriers, leading to a significant enhancement in the device's J_{sc}.

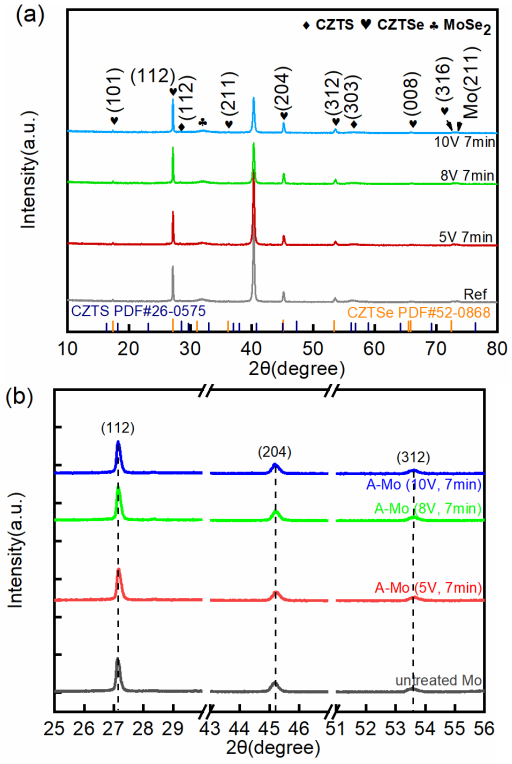

Fig 3. XRD spectra of CZTSSe/Mo and CZTSSe/A-Mo structural samples. (a) XRD spectra of samples with Mo and A-Mo back electrodes. (b) Zoomed-in XRD spectra of samples with Mo and A-Mo back electrodes, showing the (112), (204), and (312) diffraction peaks

On the aforementioned untreated Mo and processed A-Mo microstructure substrates, we investigated their influence on the phase structure of the CZTSSe absorbed layer. Fig. 3(a) displays the XRD (X-ray diffraction) pattern of the CZTSSe absorbed layer prepared on Mo substrates, both untreated Mo and those subjected to anodic oxidation at 5 V, 8 V, and 10 V for 7 min. It is observed that all diffraction peaks align well with the CZTSSe standard reference data, indicating that the substrate does not affect the phase structure. Aside from the

diffraction peak of $MoSe_2$ at 2θ=31.8°, no other secondary phases were detected. In the magnified XRD plot shown in Fig. 3(b), a slight shift of the (112), (204), and (312) diffraction peaks of CZTSSe on A-Mo substrates towards larger angles is observed compared to CZTSSe on Mo substrates.

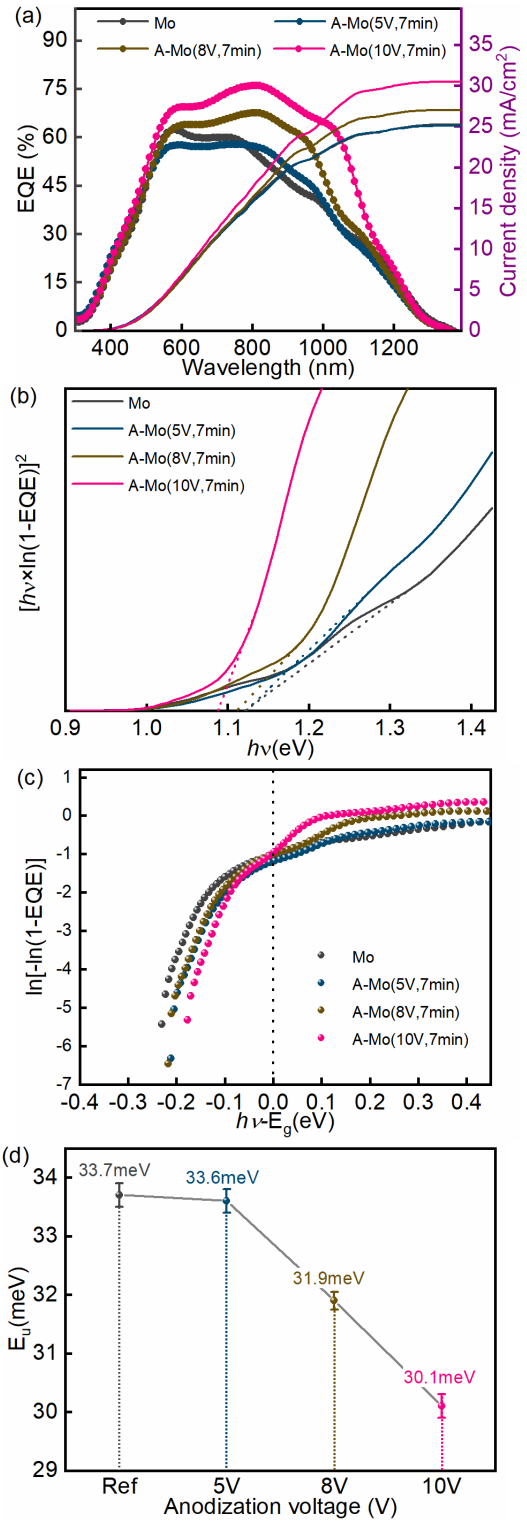

Fig 4. (a) EQE spectra of the CZTSSe solar cells assembled by Mo- and A-Mo (anodized at 5, 8, 10 V for 7 min) electrodes. (b) $[hv\times\ln(1\text{-EQE})]^2$ vs. hv plots for determining the E_g. (c) Urbach tail analysis and (d) corresponding E_U values for the cells in (a).

This suggests that oxygen (O) elements from MoO_3 may have penetrated the CZTSSe absorbed layer during the high-temperature selenization process and tend to aggregate at grain boundaries [30,31]. This results in certain lattice distortions, leading to peak shifts [32-34]. With an increase in the oxidation voltage, the diffraction peaks of Mo gradually weaken. This is attributed to the fact that, under the same oxidation duration, higher anodic oxidation voltages lead to a faster oxidation rate, causing the Mo layer to thin.

In furtherance of a detailed analysis of batteries assembled on A-Mo substrates, the inherent impacts of different voltage conditions on A-Mo structures on device performance were investigated. The corresponding External Quantum Efficiency (EQE) chart is presented in Fig. 4a. In comparison to batteries prepared on Mo substrates, it is evident that the spectral response within the range of 500-1100 nm is significantly enhanced under conditions other than the A-Mo sample treated with 7 min of oxidation at 5 V. This observation aligns with the trends in the statistical box plot of J_{SC} and is associated with the microstructure of MoO_3. The interwoven nested structure of MoO_3 effectively promotes the transport and collection of charge carriers at the interface. Moreover, the regularity of the porous array structure influences the spectral response characteristics of solar cells. The integral current density calculated from EQE aligns with the trends obtained from J-V tests, albeit being lower than the J_{SC} obtained from the J-V curve due to the influence of monochromatic light conditions.

Based on the EQE data, a plot of $(hv\times\ln(1\text{-EQE}))^2$ against hv was generated in Fig. 4b to determine the effective optical bandgap (E_g). The results indicate that the microstructure of MoO_3 influences the bandgap value of the absorbed layer, with a decreasing trend observed as the oxidation voltage increases. The bandgap for Mo-based cells is determined to be 1.12 eV, while for A-Mo (5 V, 7 min) cells, it remains at 1.12 eV. A-Mo (8 V, 7 min) cells exhibit a bandgap of 1.11 eV, and A-Mo (10V, 7 min) cells have a bandgap of 1.09 eV. The calculation of open-circuit voltage loss (V_{OC}-def) using the bandgap reveals that A-Mo-based cells have a V_{OC}-def of approximately 668 mV, whereas Mo-based cells have a V_{OC}-def of about 704 mV. Urbach energy (E_U) was computed using EQE data to analyze tail states. The variation of ln[-(ln(1-EQE))] with (hv-E_g) from Fig. 4c yields E_U values and their voltage-dependent changes, as shown in Fig. 4d. A-Mo (10 V, 7 min) displays the lowest E_U value, which may be attributed to the passivation of defects by oxygen entering the absorbed layer. This observation also underscores the impact of the regularity of the porous structure on the device's back contact, which affects the E_U value. The lower-voltage porous structure plays a role in reducing the quality of the back interface of the cell, resulting in a larger E_U value. Furthermore, the electrical characteristics near the heterojunction were analyzed through C-V testing. Fig. 5a displays the C-V and C^{-2}-V curves for Mo-based and various A-Mo-based cells, while Fig. 5b illustrates the relationship between free carrier concentration and depletion layer width, where $N_{C\text{-}V}$ and W_d values can be determined from the $N_{C\text{-}V}$ and W_d axes under zero bias voltage, as indicated in Table 1.

In this context, C, ε_0, ε_r, q, and S represent the measured capacitance, vacuum permittivity (8.85×10^{-12} F/m), the relative dielectric constant of the CZTSSeabsorbed layer film (8.6) [37], electronic charge, and device area (0.09 cm^2), respectively. As shown in Table 1, A-Mo (5 V, 7 min) based devices exhibit the highest $N_{C\text{-}V}$ and the lowest W_d, indicating a higher density of carrier capture traps. On the other hand, A-Mo (10 V, 7 min) based solar devices have wider W_d and lower $N_{C\text{-}V}$, suggesting a lower trap density, which can reduce

the tailing effect and, consequently, decrease the device's series resistance. $W_d$is associated with the separation ability of carriers, with a larger W_d indicating easier carrier separation, leading to a higher J_{SC} and improved photovoltaic performance of the device.

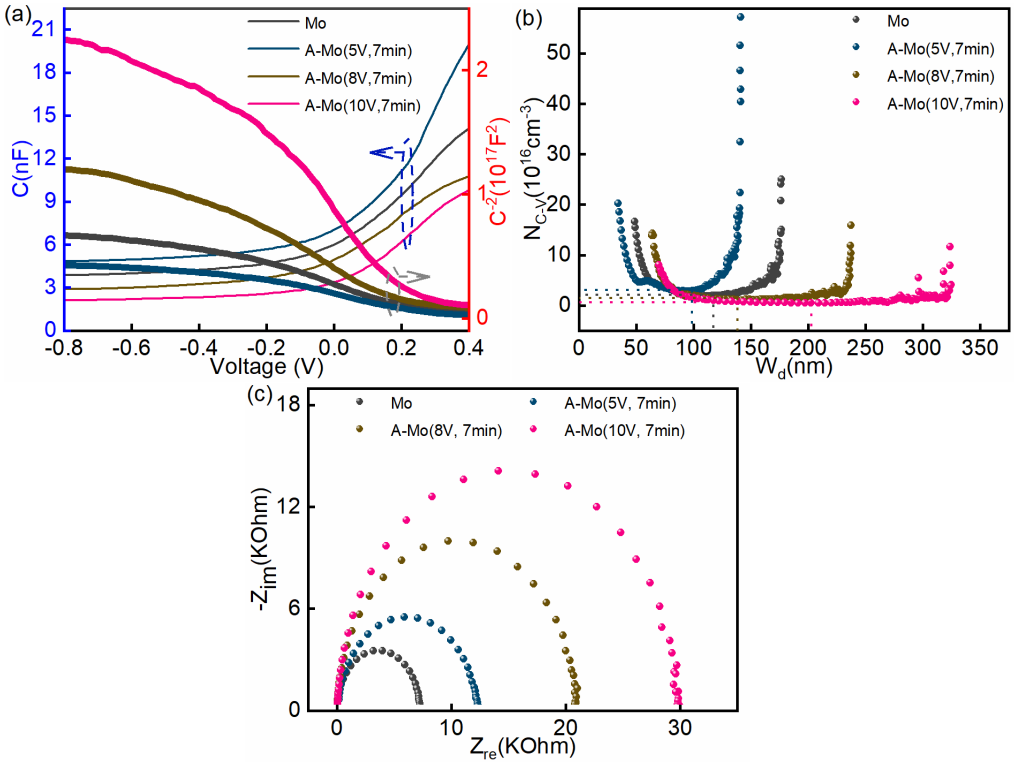

Fig 5. (a) C-V (Capacitance-Voltage) curves for Mo-based and A-Mo-based solar devices. (b) Relationship between carrier concentration and depletion layer width calculated based on the C-V curves. (c) EIS (Electrochemical Impedance Spectroscopy) Nyquist plots for CZTSSe cells prepared on different substrates

$$N_{C-V} = \frac{C^3}{q\varepsilon_0\varepsilon r S^2}\left(\frac{dC}{dV}\right)^{-1} \qquad W_d = \frac{\varepsilon_0\varepsilon_r S}{C}$$

Table 1. Mo- and A-Mo-Based CZTSSe Solar Cell Device Performance Parameters

Back electrode	C(nF)	E_U (meV)	N_{CV} (10^{15}/cm^3)	Wd (nm)	R_P (kΩ)	τ (ns)	n
Mo	6.02	33.7	19.3	114	7.23	43.52	2.02
A-Mo(5V,7min)	7.05	33.6	28.8	97	12.66	89.25	2.54
A-Mo(8V,7min)	4.96	31.9	11.1	138	20.68	102.57	2.16
A-Mo(10V,7min)	3.38	30.1	4.80	203	30.41	102.78	1.59

Subsequently, Nyquist plots of the EIS (Electrochemical Impedance Spectroscopy) were generated in Fig. 5c to analyze the recombination characteristics of minority carriers. It is evident from the semicircular diameters in the high-frequency region that the equivalent recombination resistance (R_p) for Mo-based and A-Mo (10 V, 7 min) based cells are 7.23 and 30.41 kΩ, respectively. Calculating the minority carrier lifetimes reveals an extension, as presented in Table 1. This extension in carrier lifetimes may be associated with the passivation effect of oxygen accumulating at grain boundaries [30,31].

To understand the influence of MoO_3 porous array structure back interface at different oxidation voltages on the fill factor (FF) of CZTSSe solar cells, the ideal factor (n) of the device was calculated using following equation.

$$\frac{dV}{dJ} = R_{SE} + \frac{nKT}{q}(J = J_{SC})^{-1}$$

In which, k and T represent the Boltzmann constant and temperature (300 K), as shown in Table 1. The n value for the A-Mo (10 V, 7 min) based CZTSSe solar cell is relatively small, approximately 1.59 (within the range of 1.3-2), while the n value for the A-Mo (5 V, 7 min) based cell is around 2.54 (>2). This indicates that a more regular MoO_3 array structure at higher voltages is advantageous for improving the quality of the device's back interface, reducing carrier recombination caused by defects or tunneling effects, and thereby achieving a higher device fill factor (FF).

Through a comparative analysis of the performance of Al/ITO/ZnO/CdS/CZTSSe/A-Mo and Al/ITO/ ZnO/CdS/ CZTSSe/ Mo cells, the influence of porous MoO_3 array structures at different voltages on CZTSSe cell performance was investigated. In Fig. 6, an optimization of the oxidation voltage for high-efficiency cells was conducted. Clearly, when compared to cells based on untreated Mo electrodes (with an average PCE of 5.1%), the efficiency of A-Mo cells oxidized at 10 V was the highest, averaging 7.6%. As depicted in Fig. 6a and Fig. 6c, based on previous research, considering the anodic oxidation process of the Mo layer, the oxidation voltage, which is positively correlated with the oxidation rate, results in a relatively thicker bottom MoO_3 blocking layer at

the same oxidation time when using lower oxidation voltages.

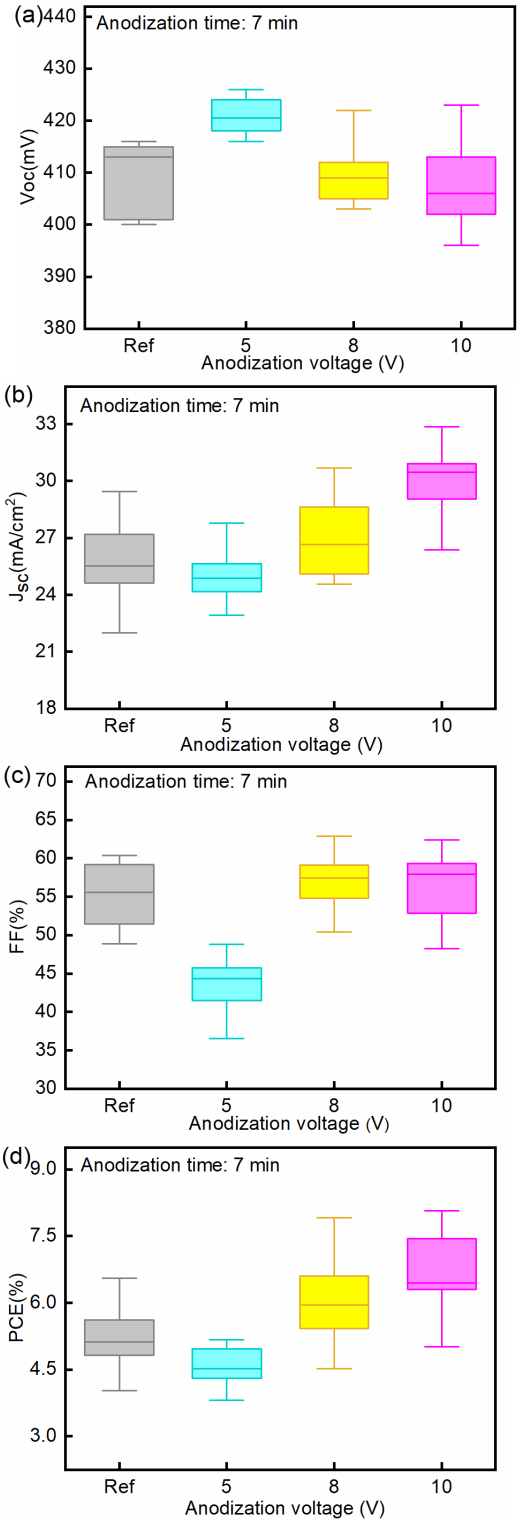

Fig 6. Statistical photovoltaic parameters of (a) V_{OC}, (b) J_{SC}, (c) FF, (d) PCE of the CZTSSe cells fabricated on Mo and A-Mo (anodized at 5, 8, 10 V for 7 min) back electrodes. At least 48 cells were statistically analyzed for each condition

An oxidation voltage of 5 V can enhance the open-circuit voltage (V_{OC}) but reduces the fill factor (FF). For larger oxidation voltages, not only can the relatively thinner MoO_3 blocking layer help increase V_{OC} and FF, but the larger pore size (105 nm at 10 V vs. 43 nm at 5 V) is more favorable for the separation and collection of charge carriers at the CZTSSe/A-Mo interface, consequently increasing the short-circuit current density (J_{SC}). The average J_{SC} at 5 V is 25.7 mA/cm², while at 10 V, it averages 30.5 mA/cm², as illustrated in Fig. 6.

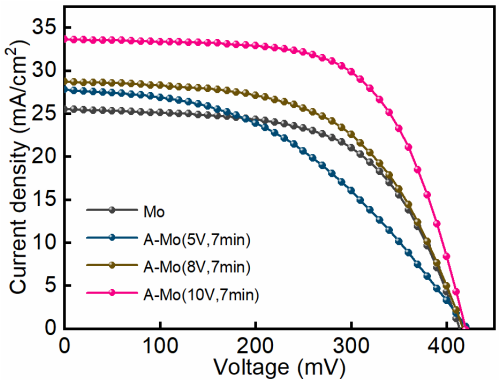

Fig 7. J-V Curves of CZTSSe Solar Cells Prepared on Mo and A-Mo Substrates

Table 2. The Detailed Photovoltaic Parameters of the Most Efficient CZTSSe Solar Devices Prepared on Mo and A-Mo (Anodic Oxidation at 7 min with Anode Voltage at 5, 8, and 10 V) Substrates.

Back electrode	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	PCE (%)
Mo	416	25.49	59.53	6.31
A-Mo(5V,7min)	426	27.79	43.64	5.17
A-Mo(8V,7min)	422	28.72	55.94	6.78
A-Mo(10V,7min)	422	33.63	63.35	9.00

Fig. 7 displays the J-V curves of untreated Mo-based and A-Mo-based solar devices oxidized at different voltages, and the performance parameters of the devices are summarized in Table 2. The performance of solar devices is influenced by the porous MoO_3 structure, and, in comparison to Mo-based cells, the efficiency of A-Mo solar cells processed at the optimal oxidation voltage reaches 9.00%, representing a 43% improvement. The J_{SC} increases from 25.49 to 33.63 mA/cm², marking a 32% enhancement. Furthermore, the FF increases from 59.53% to 63.35%. This indicates that the MoO_3 array structure corresponding to the optimal voltage can facilitate the improvement of solar device performance.

4. Conclusion

In this study, Anodic oxidation treatment of Mo glass was conducted at various oxidation voltages to introduce a MoO_3 array structure at the CZTSSe back interface. The nested array back interface structure facilitated the enhancement of CZTSSe solar cell performance. By employing the optimal oxidation voltage to introduce the well-ordered MoO_3 array structure at the back interface of solar devices, the formation of $MoSe_2$ at the back interface could be reduced, thereby improving the back interface quality. This, in turn, reduced Urbach energy, minimized the band tailing effect, and lowered non-radiative recombination of charge carriers. Consequently, this strengthened the separation, transport, and collection capabilities of charge carriers, ultimately improving device performance. Compared to untreated Mo-based solar cells, the device efficiency increased by 43% to 9.00% at the optimal voltage of 10 V, with J_{SC} increasing from 25.49 to 33.63 mA/cm² and FF increasing from 59.53% to 63.35%. This suggests that different back interface structures can significantly impact device performance, and the porous array structure based on the optimal voltage can effectively

enhance device performance.

Conflicts of Interest

There are no conflicts to declare.

Acknowledgments

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