**Academic Journal of Science and Technology**
ISSN: 2771-3032 | Vol. 12, No. 1, 2024

# Study of SOI-MOS Self-heating Effect Suppression Method in CMOS Process

**Yang Liu ***

Tianjin Sino-German University of Applied Technology, Tianjin, 300350, China

*** Corresponding author Email:** liu581199@gmail.com

**Abstract:** Silicon on Insulator Metal Oxide Semiconductor (SOI-MOS) technology, as a new fabrication method, has good thermal characteristics compared with the traditional CMOS technology, which can effectively reduce the self-heating effect of the device. However, with the continuous development of nanotechnology, the feature size of CMOS integrated circuits is gradually reduced, and the thickness of silicon on the insulating layer is gradually thinned, which makes the "self-heating effect" increase. The passage of current through a conductor may result in a localized temperature increase due to the material impedance and internal resistance of the conductor caused by the current. This temperature increase may affect the performance and stability of the device. Therefore, it is important to take measures to protect or regulate this "self-heating effect" in the design. In this paper, through the analysis of the thermal characteristics of SOI-MOS devices, this article has studied the methods of suppressing the self-heating effect of SOI-MOS devices based on thermal interface materials, and the experimental results show that these methods can effectively improve the thermal conductivity of the devices, thus suppressing the self-heating effect of the devices.

**Keywords:** SOI-MOS Device; Thermal Interface Material; Self-heating Effect; Heat Dissipation Technology.

## 1. Introduction

With the rapid development of integrated circuit technology, especially the wide application of CMOS process technology, the performance of semiconductor devices continues to improve, but the accompanying thermal management problems are also increasingly prominent. In the CMOS process, SOI-MOS devices are widely used because of their excellent performance and reliability. However, with the reduction of device size and the improvement of integration, the impact of self-heating effect on the performance of the device becomes more and more obvious, which poses a serious threat to the stability and lifetime of the device. The self-heating effect refers to the phenomenon that the temperature of a device rises due to the passage of current during operation, which in turn affects the performance of the device. For SOI-MOS devices, the self-heating effect is mainly manifested in the change of threshold voltage, the reduction of sub-threshold slope, and the reduction of carrier mobility. These effects can cause device performance degradation, and even cause device failure. Therefore, to improve the performance and reliability of SOI-MOS devices, it is of great significance to explore effective methods to suppress the self-heating effect. At present, a variety of methods to inhibit the self-heating effect have been proposed by scholars at home and abroad, including the improvement of the device structure design, the use of high thermal conductivity materials as the thermal interface layer, and the development of a new type of heat dissipation technology. These methods often have various limitations such as high cost, complex processing or large impact on device performance. In view of the above, this paper aims to conduct an in-depth study on the self-heating effect of SOI-MOS devices in CMOS process and discuss the effective suppression strategies. By establishing an accurate self-heating effect model, analysing the effects of different thermal conductivity enhancement techniques on device performance, and studying the self-heating effect suppression method based on thermal interface materials, we expect to provide a new method to solve the self-heating effect problem of SOI-MOS devices.

## 2. Domestic and International Research Status

SOI-MOS devices are widely used in high performance integrated circuits due to their excellent electrical characteristics and low power consumption. As the device size shrinks with the advancement of the process node, the performance of the device is more and more affected by the self-heating effect, which not only causes the degradation of the device performance, but also may cause the device failure. The self-heating effect not only causes the degradation of device performance, but also may result in device failure. The suppression of the self-heating effect in SOI-MOS devices has become a hot research topic[1] .

International research on the self-heating effect of SOI-MOS devices mainly focuses on theoretical analysis and experimental verification. Some research teams have predicted the impact of self-heating effect on device performance by building complex physical models that take into account a variety of factors, such as device structure, operating conditions, and so on. Meanwhile, some researchers have also utilised advanced fabrication techniques and materials, such as ultra-thin silicon layers and localised heat dissipation techniques, in order to improve the thermal conductivity of the devices and thus reduce the impact of self-heating effects.

In China, the research on the self-heating effect of SOI-MOS devices has been gradually deepened with the rapid development of semiconductor technology. Several universities and research institutes in China have carried out relevant basic and applied research. A research team has studied the mechanism of self-heating effect generated by traditional MOS devices. An in-depth discussion was conducted and the research results were applied in SOI-MOS

devices. Domestic researchers have also made some progress in the research of thermal interface materials such as metal thermal interface materials and thermal conductive polymers application research, which are designed to improve the thermal management capability of devices and reduce the self-heating effect [2].

# 3. SOI-MOS Device Self-heating Effect Modelling

## 3.1. Self-heating Effect of Conventional MOS Devices Analysis

For SOI-MOS self-heating effect research has a certain foundation, but the traditional solution to the self-heating effect is usually to change the material or thickness of the $SiO_2$ buried layer, this method has a certain effect on improving the self-heating effect of SOI-MOS, the following figure shows us the material properties of Si, $SiO_2$ , Si $O_{34}$ , AlN at 27 ℃ [3] , respectively.

| | Si | $SiO_2$ | $Si_3N_4$ | AlN |
|---|---|---|---|---|
| $k$/(w/m °C) | 150 | 1.4 | 30 | 150～200 |
| $\alpha/10^{-6}\cdot °C^{-1}$ | 2.6 | 0.5 | — | 4.4 |
| $E_b/10^6\,V\cdot cm^{-1}$ | 0.2 | 13 | 10 | 14 |
| $E_g$/eV | 1.12 | 9 | 5 | 6.2 |
| $\varepsilon_r$ | 11.9 | 3.9 | 7～7.5 | 8.9 |
| $n$ | 3.5 | 1.46 | 2.05 | 2.15 |
| $\rho/\Omega\cdot cm$ | $>10^3$ | $>10^{14}$ | $>10^{14}$ | $>10^{13}$ |

**Fig 1.** The material characters of Si, $SiO_2$, $Si_3N_4$ and AIN at 27°C

It can be seen from the figure that AlN has high thermal conductivity, large dielectric constant, large resistivity, and high breakdown field strength, so theoretically the self-heating effect in the device channel can be effectively reduced by AlN as the buried layer of SOI.

When designing and fabricating ultra-thin silicon layers, a variety of factors need to be considered, including material selection, processing technology and structural design. The figure below shows us the lattice temperature distribution at the bottom of the silicon film inside the N-channel SOIMOSFET with different buried oxygen layer thicknesses [3].

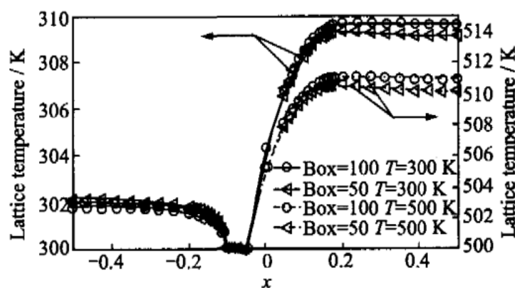


**Fig 2.** Lattice temperatures versus BOX thickness for various ambient temperatures. The slice position is at the bottom of thin Si film

## 3.2. Physical Characteristics of SOI-MOS Devices

SOI (Silicon on Insulator) technology significantly improves the performance of conventional silicon-based devices by adding a layer of insulating material to the silicon wafer, creating an interface between the semiconductor and the insulator. This structure not only increases the speed and efficiency of the device, but also reduces the power consumption, making SOI-MOS devices widely used in modern electronic devices. [4]

The self-heating effect can be expressed by the following equation:

$$P = I^2R \tag{1}$$

where $P$ is the power (in watts), and $I$ is the current through the device (in amperes), and $R$ is the equivalent resistance of the device (in ohms).

The main physical characteristics of a SOI-MOS device include its carrier mobility, threshold voltage, etc. The thermal conductivity is the amount of heat that passes through the material per unit of time, which directly affects the ability of the device to dissipate heat. Thermal conductivity refers to the amount of heat that passes through a unit area of material per unit time, which directly affects the heat dissipation capability of the device. For SOI-MOS devices, the level of thermal conductivity determines whether the device can effectively transfer the heat generated to the thermal environment when working.

$$\alpha = \frac{Q}{A\cdot\Delta T} \tag{2}$$

where $\alpha$ denotes the thermal conductivity, and $Q$ is the amount of heat passing through the material, and $A$ is the area of the material, and $\Delta T$ is the temperature change.

Carrier mobility, on the other hand, describes the speed at which carriers move in the presence of an electric field, a parameter that is directly related to the switching speed and operating frequency of the device. Higher carrier mobility means faster signal processing and lower power consumption.

$$\mu = \frac{v_d}{E} \tag{3}$$

where $\mu$ denotes the carrier mobility, and $v_d$ is the carrier drift velocity, and $E$ is the applied electric field strength.

In addition, the threshold voltage of the SOI-MOS device is also an important parameter for measuring the performance of the device, which reflects the minimum voltage at which the device begins to conduct. A lower threshold voltage reduces the leakage current of the device during low-voltage operation, which in turn reduces the overall power consumption.

$$V_{th} = V_{FB} + \frac{2kT}{q}\ln\left(\frac{n_s}{n_i}\right) \tag{4}$$

where $V_{th}$ is the threshold voltage, and $V_{FB}$ is the Fermi-Ohm boundary voltage, and $k$ is the Boltzmann constant, and $T$ is the absolute temperature, and $q$ is the electron charge, and $n_s$ is the surface doping concentration, and $n_i$ is the intrinsic carrier concentration.

In summary, the physical characteristics of SOI-MOS devices determine their application performance in electronic devices. By optimising these characteristics, the performance and reliability of the devices can be further enhanced to meet the demands of modern electronics.

## 3.3. Analysis of the Self-heating Effect of SOI-MOS Devices

SOI-MOS devices show excellent performance in high-frequency, low-power applications, but their self-heating effect adversely affects device performance. In this section, the self-heating effect of SOI-MOS devices and its mechanism are analyzed.

The self-heating effect mainly originates from the Joule heat generated when the current passes through the conducting path during the device operation. For SOI-MOS devices, the generation of heat is closely related to the

structure of the device. Specifically, the heat transfer can be calculated by the following equation: $Q = \alpha P$

where $Q$ denotes the amount of heat generated per unit time, and $\alpha$ is the heat diffusion coefficient, and $P$ is the power density.

Considering the special structure of SOI-MOS devices, the selection of the thermal interface material (TIM) becomes particularly important. The thermal conductivity of the TIM ($k$) directly affects the heat transfer rate from the device to the substrate. Therefore, increasing the thermal conductivity of TIM is one of the effective means to suppress the self-heating effect [5]

The selection of thermal interface materials requires consideration not only of thermal conductivity, but also of factors such as compatibility with the device and cost. For example, although polymer materials have lower thermal conductivity, their excellent flexibility and good electrical insulation properties make them still competitive in some application scenarios. [6]

In summary, the analysis of the self-heating effect of SOI-MOS devices involves several aspects, including the mechanism of heat generation, the pathway of heat transfer and the selection of thermal interface materials. By optimising the device structure design and selecting high thermal conductivity thermal interface materials, the self-heating effect can be effectively reduced, thus improving the performance of the device. [7] The performance of the device can be improved by optimising the device structure design and selecting high thermal conductivity thermal interface materials.

# 4. Thermal Conductivity Enhancement Techniques for SOI-MOS Devices

## 4.1. Research on Thermal Interface Materials

In SOI-MOS devices, Thermal Interface Material (TIM) plays a crucial role in filling the gap between the chip and the heater to improve the thermal conductivity efficiency. Thermal Interface Material (TIM) is usually classified into three main categories according to their different thermal conductivity. Copper, silver and other metal thermal conductivity is very high, but because of its high price, and the device may produce corrosion and other problems, the application is more limited. Such as thermal conductivity polyether ketone (PEEK) and polytetrafluoroethylene (PTFE) and other polymers, its thermal conductivity is low, but inexpensive, widely used. Composites combine the advantages of metals and polymers, such as metal-based composites (MBC) and ceramic-based composites (CBC), which also provide good mechanical strength and chemical stability while maintaining high thermal conductivity.

The performance of thermal interface materials not only depends on thermal conductivity, but also needs to consider its temperature resistance, electrical insulation, bonding strength, cost and other factors. Selection of the appropriate thermal interface material requires comprehensive consideration of the operating environment and life of the equipment. The application of thermal interface materials also need to pay attention to its installation method and thickness, which will have an impact on the final thermal conductivity.

With the development of technology, new thermal interface materials are emerging, such as nanocomposites and graphene. These new materials exhibit higher thermal conductivity and better mechanical properties, providing new possibilities for improving the thermal management efficiency of SOI-MOS devices. Future research will focus on the development of thermal interface materials with higher thermal conductivity, better thermal stability and lower cost to meet the increasingly demanding thermal management requirements [8]

## 4.2. Ultra-thin Silicon Layer Research

Ultra-thin silicon layers play a key role in improving the thermal conductivity of devices and help mitigate the impact of self-heating effects on SOI-MOS device performance. By optimising the silicon layer thickness, the thermal management performance of the device can be effectively enhanced. In this section, the effect of different thicknesses of ultrathin silicon layers on the thermal performance of the devices will be explored.

In order to better understand the impact of ultra-thin silicon layers on the device performance, numerical simulations were used to analyse the thermal conduction characteristics at different silicon layer thicknesses [9]

$$T_{max} = \frac{P}{kA} \tag{5}$$

where $T_{max}$ is the maximum temperature, and $P$ is the power density, and $k$ is the thermal conductivity, and $A$ is the effective heat transfer area.

By varying the thickness of the silicon layer, the effect of different thicknesses on the maximum operating temperature of the device can be observed. Table 1 shows the effect of different silicon layer thicknesses on the maximum operating temperature under the same conditions.

**Table 1.** The effect of different silicon layer thicknesses on the maximum operating temperature

| Silicon layer thickness (nm) | Maximum operating temperature (°C) |
|---|---|
| 10 | 95 |
| 20 | 85 |
| 30 | 75 |

From the above table 1, it can be seen that the maximum operating temperature of the device decreases with the increase of the silicon layer thickness. This proves that the self-heating effect of the device can be effectively controlled by adjusting the thickness of the silicon layer. Further experiments and simulations show that the appropriate thickness of the silicon layer not only reduces the maximum operating temperature of the device, but also improves the lifetime of the device. Excessively thick silicon layer will also bring cost and size limitations, so it is necessary to find a best balance. The study of ultra-thin silicon layer is of great significance to improve the thermal management performance of SOI-MOS devices. By precisely controlling the thickness of the silicon layer, the thermal performance of the device can be significantly improved, and thus the overall performance and reliability of the device can be improved. Future research will continue to explore new techniques to further optimise the performance of ultra-thin silicon layers.

# 5. Summary

In this paper, we provide a new idea to reduce the power consumption and improve the performance of SOI-MOS devices by thoroughly investigating the self-heating effect of SOI-MOS devices in CMOS process and proposing various suppression methods. Based on the analysis of the self-

heating effect of traditional MOS devices and the physical properties of SOI-MOS devices, this study establishes a self-heating effect model applicable to SOI-MOS devices and explores three main thermal conductivity enhancement techniques: thermal interface materials, ultra-thin silicon layers, and local heat dissipation techniques. [10]. The research results of thermal interface materials, as the key link connecting the device and the heat dissipation system, show that different types of thermal interface materials, such as thermally conductive polymers, metals, and silicon oxides, can effectively enhance the heat transfer efficiency. Especially in the field of micro- and nanoelectronics, these researches provide strong support for solving the thermal management problems of SOI-MOS devices [11]

# References


[1] Wang, Y., Zhou, X., Zeng, M., et al. (2021) Effect of Annealing Temperature on the Performance of OSG Films. Electronics World, (20): 20-21.

[2] Yang, S., Liu, Y. (2023) Current Status and New Developments of SiC Power LDMOS Devices. Semiconductor Technology, 48(11): 949-960.

[3] Gao, Y., Zhang, X., Liu, M., et al. (2006) Study of Self-Heating Effect in SOI Devices Based on Equivalent Capacitance Method. Research & Progress of SolidState Electronics, (04): 450-455.

[4] Luo, N., Cao, J. (2022) Current Status and Prospects of High-Temperature SOI Technology. Electronics & Packaging, 22(12): 89-97.

[5] Lu, H., Cao, J., Wu, B. (2019) Optimization and Characterization of Metal Silicide Process in 90 nm CMOS Technology Platform. Integrated Circuit Applications, 36(09): 17-19.

[6] Luo, N. (2022) High-Temperature Semiconductor Technology Maximizing the Performance of Silicon Carbide. China Integrated Circuit, 31(06): 31-36.

[7] Fan, W., Yan, J., Feng, R., et al. (2021) Research on Optimization of Bipolar Device Structure and Process Using Low-Temperature Oxidation Technology. China Integrated Circuit, 30(06): 89-93.

[8] Yang, F., Hang, C., Tian, Y. (2021) Research Progress on Preparation and Sintering Performance of Nano-Paste for Power Device Packaging. Electronics & Packaging, 21(03): 12-21.

[9] Li, X., Wang, M., Wu, J., et al. (2020) Study on the Effect of Conducted Electromagnetic Interference on Silicon-On-Insulator Process Devices. Research & Progress of Solid State Electronics, 40(02): 149-153.

[10] Su, J., Zhu, X., Ji, X., et al. (2024) Research Progress on Physical Preparation Process of Si-Based SiC Films. Journal of Changzhou University (Natural Science Edition), 36(01): 9-17.

[11] Jiang, H., Yu, X., Xue, M., et al. (2021) Application and Latest Research Progress of Silicon Carbide in Thermal Conductive Materials. Journal of Nanchang Hangkong University (Natural Science Edition), 35(02): 51-60.