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High -resolution Time Interval Measurement Research based on FPGA

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Abstract: In modern scientific research and engineering practice, high -precision measurement of time interval between two or more physical events is often required. After years of development, there are currently many ways to measure a variety of high -precision time interval. If you implement different technologies, it can be divided into two categories: simulation and numbers. The simulation method is mainly to convert T to voltage by charging capacitance and then convert it into a digital amount through the modulus. However, the traditional simulation methods include the shortcomings of temperature sensitivity and long conversion time. Therefore, digital methods are generally used to achieve measurement. Common digital measurement methods include direct counting method, tap latency method, and cursor method. However, common measurement methods cannot meet actual needs. Therefore, this article relies on the FPGA platform to achieve a time interval measurement method with resolution to Ana second -level.

Keywords: FPGA; Time Interval Measurement; Multi -phase Clock Sample.

1. Preface

Usually, we understand time as time or time interval -the former indicates when an event occurs, also known as the absolute time, and the latter indicates the length of the incident. Time has one dimension, and absolute time does not have the actual physical significance in the measurement system. The actual measurement mainly involves the relative time relationship between two or more events. The time measurement involved in this paper refers to the relative time interval.

Time interval measurement, in our daily life, the impact of errors is not very large, and the measurement accuracy reaches the second or microsecond levels. Learning and other applications such as aerospace, satellite launch and monitoring, navigation communication, and scientific measurement, national defense and national economic construction, precise time interval measurement is particularly important. Time interval measurement has always been regarded as a very reliable identification and detection method. Especially during the above -mentioned research process, the time -based coordinates of quantitative research and time -sequential measurement are provided by precise time, so the requirements for time measurement accuracy are very important. Strict, otherwise it will cause unavoidable major losses.

The development and improvement of TDC technology have very great practical significance and long -term strategic significance. How to use TDC to achieve higher and stable time measurement accuracy has become the goal of continuously pursuing exploration by many scientific researchers.

2. Related Theories and Methods

2.1. Direct Counting Method

The direct counting method is also known as a rough count method. The principle is to use the reference clock to fill the pulse filling the start signal and the end signal, so as to achieve the time interval between the start signal and the end signal. Periodus T, so it is often used in areas where the measurement accuracy is not high, as shown in the figure below is the basic measurement principle of the direct counting method.

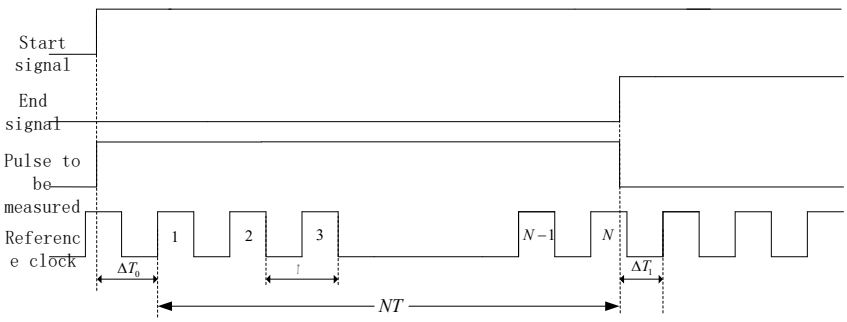

Figure 1. The principle of direct measurement method

As shown in the figure above, measurement through the direct count method, when the cycle of the reference clock is T and the value of the counter is n, the time interval measured in this method is:

$$t = NT \tag{1}$$

But in fact, it can be clearly seen from the figure that the actual time interval should be:

$$t1 = T0 + NT - T1 \tag{2}$$

Therefore, the measurement error is:

$$-T < T0 - T1 < T \quad (3)$$

As can be seen from the above figure, although the direct counting method has the advantages of simple circuit implementation and large measurement range, there are also large measurement errors, and the measurement accuracy is related to the system clock frequency. Therefore, in order to reduce the measurement error of the direct counting method, the signal frequency of the base clock is generally increased. However, if you want to measure the accuracy of 1NS and above, the reference clock frequency must reach 1GHz and above, which will greatly increase the power consumption and complexity of the circuit, and the cost will also increase.

2.2. Castle Card Ruler Method

The measurement principle of the cursor method is derived from the staple ruler in daily life. The cursor method requires two clock signals of different frequencies. The CLK1 with larger cycles is used as the benchmark clock and CLK2 with a smaller cycle as a clock. When the signal starts, the counter 1 starts the count. When the signal comes, the counter 2 also starts counting until the phase of the two clock signals is overlapped. The two counter stops counting at the same time to obtain the time interval signal to be tested. The measurement principle of the cursor method is shown in the figure below:

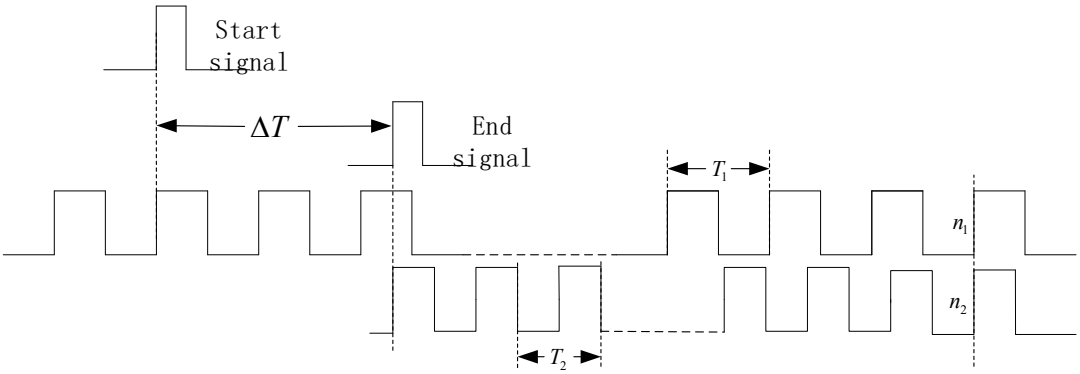

Figure 2. The principle of measuring the cursor method

As shown in the figure above, when the signal comes, the wait time T1, until the rising edge of the clock signal CLK1 comes, the count will be counted. When the rising edge of CLK1 and CLK2 stops counting, the count value is obtained. When the signal comes, wait time T2, until the rising along the clock signal CLK2 starts to count. When the rising along CLK1 and CLK2 stops the counting time, the counting value N2 is obtained. At this time, the time interval to be tested is:

$$T = n1T1 - n2T2 = (n1 - n2)T1 + n2(T1 - T2) \quad (4)$$

From the above two forms, the resolution of the final measurement value is determined by the cycle difference between CLK1 and CLK2. When the frequency of CLK1 and CLK2 closer, the higher the resolution of the measurement value.

In the formula, the error of the final measurement value -T1 ≤ Δt ≤ T2,

It can be seen that the higher the frequency between CLK1 and CLK2, the higher the accuracy of the measurement value; the more hours the cycle is, the higher the resolution of the measurement value.

In summary, whether it is the direct measurement method (rough count), or the tap delay method (fine count) and the cursor method (detailed counting) each have the advantages and disadvantages, so the current mainstream measurement method is "rough count+fine count" The measurement method, the TDC measurement used in this article is also used by this method.

3. TDC Module Design

The above measurement methods cannot be competent for high -precision measurement design requirements, so TDC design is used to meet the requirements of this system design. Many chips for TDC measurement have appeared, such as ACAM's TDC-GP22 chip. However, the external chip will cause abnormalities such as decreased chip performance or failure over time over time. Therefore, the use of FPGA -based TDC design can reduce the problem of external chips and cause the entire system to be unable to work. On the occasion, it became more flexible and fast. At present, TDC design based on FPGA mainly has two methods: TDL and MPCS. However, TDC -based TDC circuits have a lot of resources. In order to design and realize TDC with less resource consumption and simple structure, this article uses a multi -phase clock sampling method to complete the design of the TDC circuit to complete the collection of phase difference data.

The TDC design based on MPCS is combined with "rough measurement"+ "fine measurement". The rough measurement uses the direct counting method, and the detailed measurement adopts a multi -phase clock sampling method. Through the combination of these two methods, the advantages of the high -resolution of the high -resolution method of the direct counting method and the high -resolution method of the multi -phase clock sampling method can be taken into account. The FPGA -based TDC module design is shown below.

System clock SYS_CLK through the clock management unit (MMCM) to get a 200MHz clock clk_out, clock clk_out connects the rough measurement module to measure the phase difference between the two ways to enter the signal Signal1 and Signal2, and save the results into the register In t1. In addition, the clock clk_out then moves through the clock management unit to get the same frequency as the clock clk_out frequency, and the 7 clock clk_out1, clk_out2, and clk_out7. Each clock phase is 45°. Connect to the detailed measurement module, take a closer look at the phase difference between the input signal Signal1 and Signal2 to be

tested in two roads. In the register t2, the rising edge of the test input signal Signal2 is measured by the rising edge of the clock signal clk_out next to it. The result is stored in the register t3, and the total measurement value of the total measurement value is calculated through the measurement results module.

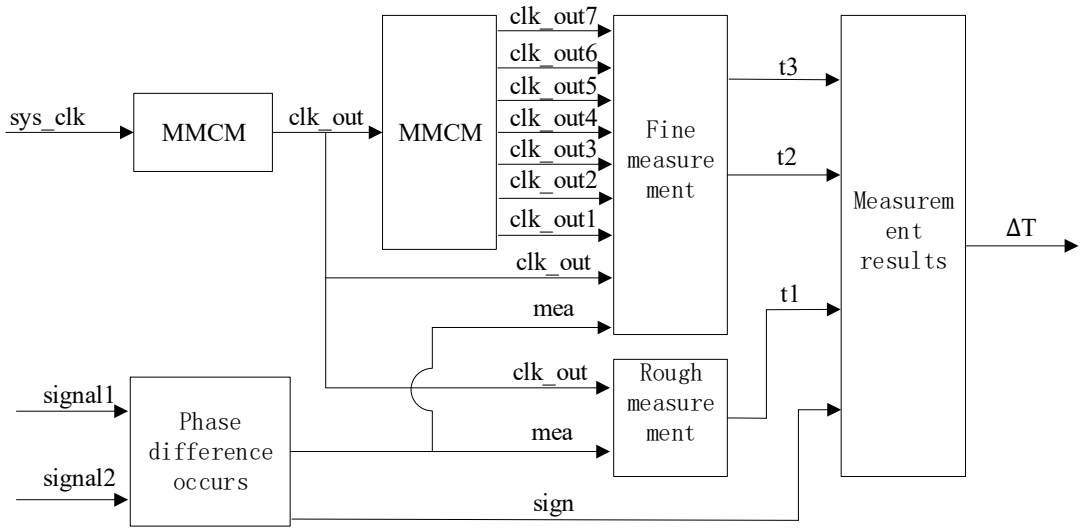

Figure 3. TDC module measurement principle

4. FPGA Implementation

The figure below is the three possible simulation results of the TDC module when the time difference is measured. As shown in the figure above, the Signal1 signal and the Signal2 signal are shown three shots. If it occurs, edge detection can also be achieved. Connect the input terminal of the Signal1 signal and the Signal2 signal with the input terminals of the two different trigger groups. 8 clocks of the same frequency of the same frequency are connected to the clock input end of the D trigger, and the FCNT and FCNT0 are obtained. Get FCNT2 and FCNT20 synchronized with clock clk_out to reduce the occurrence of sub -stable. When the Signal1 signal and the Signal2 signal are detected, the FCNT2 and FCNT20 are locked to obtain the FCNT3 and FCNT30, and the results obtained by the shooting of FCNT3 and FCNT30 are just the same as the locking result of the previous register group.

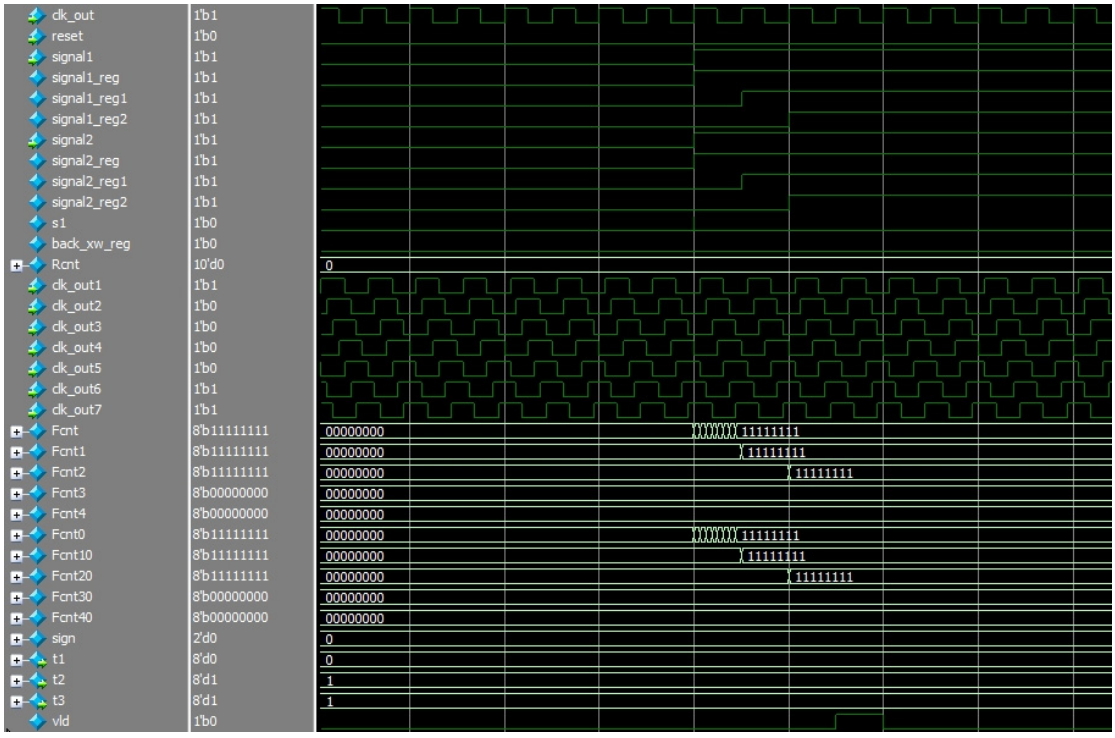

Figure 4. Signal1 is the same as Signal2

After the measurement is completed, the result of the register is decoded to minimize the multiplier of the locking result of the FCNT4 and FCNT40 decodes (0.3125). And save the results after decoding into the register t2 and register t3. When the vld is high, it means that the value in the register sign, t1, t2, and T3 is valid. The time interval between time △T is obtained through the next formula:

$$\Delta T = t1 + t2 - t3 \tag{5}$$

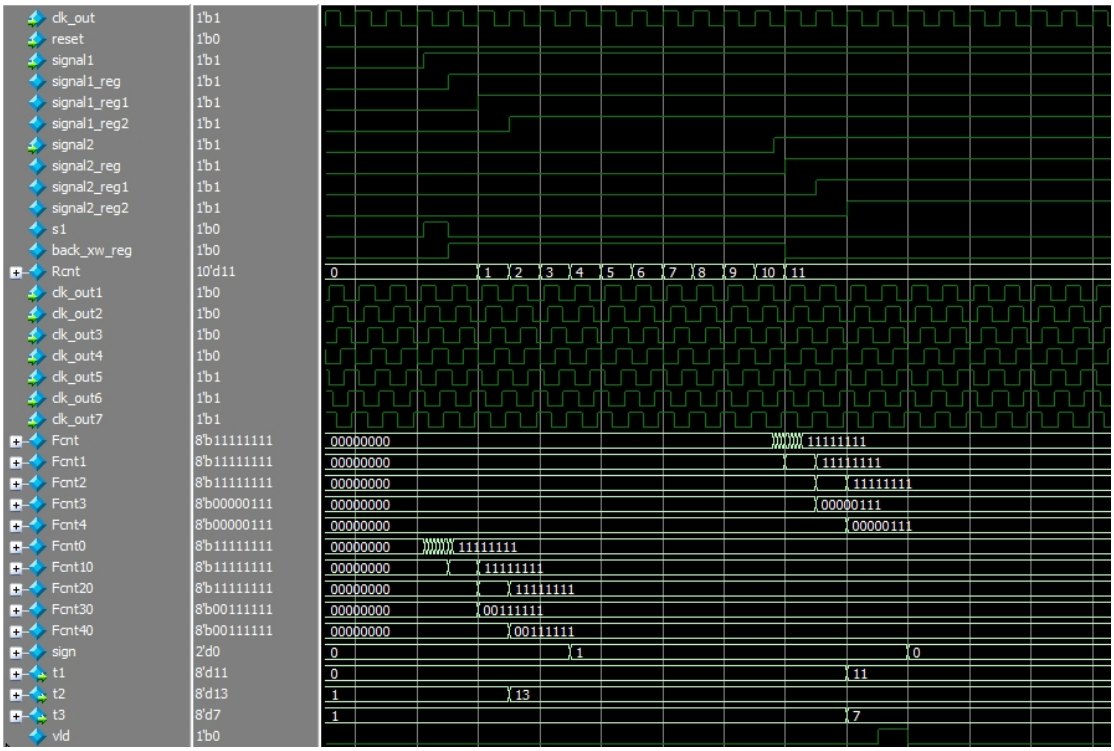

Figure 5. Signal1 is first in Signal2

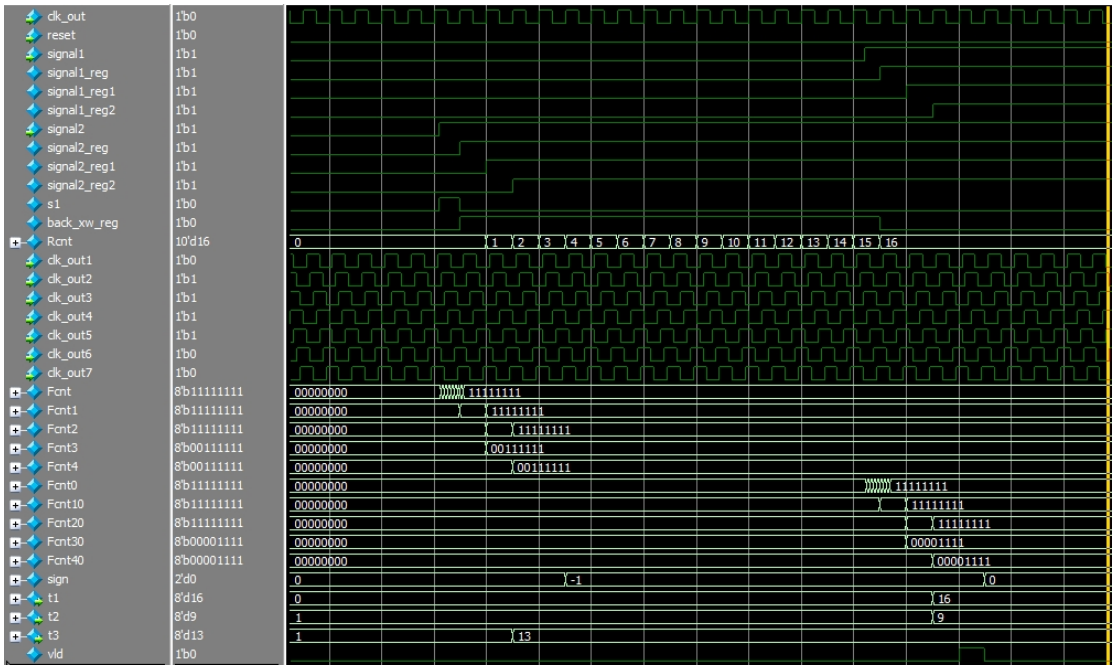

Figure 6. Signal2 is first in Signal1

For the rising edge of the Signal1 in the figure above and the rising edge of Signal2, the actual time interval is 0ns. According to the upper formula, the time interval measured by the TDC module is 0ns and the error is 0ns. For the rising alongs of the Signal1 in the figure above, the rising edge of Signal2 is reached. The actual time interval is 57ns. According to the upper formula, the time interval measured by the TDC module is 56.875ns and the error is 0.125ns. For the rising edge of the Signal1 in the figure above, the rising edge of Signal2 is reached. The actual time interval is -81ns. According to the upper formula, the time interval measured by the TDC module is -81.25ns, and the error is 0.25ns. Met the design requirements.

5. Result Analysis

On the basis of summing up the current popular time interval measurement method, this article analyzes FPGA -based interval measurement technology and puts forward our methods. We have selected a suitable solution based on the FPGA -based TDC system to complete the design. Through the simulation test, the resolution can reach the Ana seconds, and the error is also within Ana seconds. These research results have contributed to the development of time interval measurement technology.

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