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Analysis of Current Imbalance in Paralleled Silicon Carbide Power MOSFETs

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Abstract: In order to adapt to the application scenarios of high power variable current, it is an effective solution to parallel multiple silicon carbide (SiC) power. However, the static parameters of SiC MOSFET devices are dispersed, the parasitic parameters of power loop are asymmetric, and the working junction temperature of the devices is different. All these factors will lead to non-uniform current stress between parallel devices.This article is based on the SiC MOSFET device provided in Wolfspeed,to explore the impact of circuit parameters mismatch on current sharing in parallel components. The influence of the circuit parameters on the static and dynamic current sharing of the parallel SiC MOSFET device is obtained, and the influence of each factor on the specific process is summarized, and the most influential factor on the current change in the case of parameter mismatch is compared.

Keywords: Parallel SIC MOSFET, Parasitic inductance, Parasitic capacitance, Control variable method, Uneven current of current.

1. Introduction

In the field of new electronic devices, power electronics is an important link in the power energy industry chain, the core component is power semiconductor devices. Silicon carbide (SiC) MOSFET is considered to be the most potential development of new semiconductor devices. However, it is difficult for SiC MOSFETs meet the requirements of high power applications due to the flow limit resistance of sic devices. There are generally two methods so as to solve the problem that a single SiC MOSFET discrete device does not meet the current demand, . The first one is using a multi-chip parallel power module; the second one is using multiple single discrete devices directly in parallel. Due to the dispersion of parameters between parallel devices,There are differences in junction temperature, lack of consistency in loop parasitic parameters,, there will inevitably be the phenomenon of uneven current, resulting in temperature rise and electromagnetic interference differences between devices, current inequality will lead to large losses, high temperature. Furthermore, the aging degree of the device is different. If the current imbalance is not dealt with during this period, the performance of the device will be gradually reduced, and the thermal failure of the device will be more likely, which will further expose the application circuit to great risks[1-5].

Inhomogeneity current analysis of parallel devices includes static current inhomogeneity after conduction and dynamic current inhomogeneity during switching [5-6]. Static current imbalance refers to the drain current imbalance phenomenon caused by the mismatch between the on-resistance and the driving voltage when the parallel SiC MOSFET is fully conducting. Dynamic current imbalance refers to the current imbalance phenomenon in the switching process caused by the difference of the drain current in each branch due to parasitic parameters and drive loop.

Regarding the influencing factors of

Uneven flow of electric current, there are, literatures [7-9] have tested and evaluated the discretization of SiC MOSFET device parameters, but also analyzed the influence of device parameter inconsistency on steady-state and transient current imbalance [10]. The existing literature had already studied its mechanism and countermeasures. The analysis of literature [11-12] shows that the dispersion of device parameters has a direct impact on the static and dynamic current imbalance. The on-resistance affects the static current balance of parallel devices. On the other hand， the threshold voltage affects the dynamic current balance between devices. The pins of the device package will also introduce the parasitic inductance of drain and source, as a consequence, the dispersion of these parameters will also affect the current balance of parallel devices [13-14].

The parasitic parameters are located in the driving loop and power loop of the device and their differences will affect the drain current and switching time of SiC MOSFET in the switching process to a certain extent. Therefore, the influence of parasitic parameters on the switching process should be analyzed and suppressed. In this paper, through the use of software LTspice simulation method, control variables, analysis of inductance, capacitance mismatch in static and dynamic switching, the impact of current changes. The amplitude of current change was compared with the parameter change of the same amplitude, then the most influential factors were summarized.

2. Circuit Principle and Heterogeneous Current Analysis

2.1. Test circuit analysis

In this paper, the test circuit of SiC MOSFET device in parallel as shown in Fig.1 is established. The test circuit can flexibly change the parasitic inductance value of three peripheral circuits of the parallel device.Q_1 and $Q_2$are two SiC MOSFET devices operating in parallel,C_{gs1},C_{gd1},$C_{ds1}$and C_{gs2},C_{gd2},$C_{ds2}$are respectively gate-source capacitance, gate-drain capacitance and drain-source stage capacitance of Q_1 and Q_2. In order to ensure the consistency of the driving signal, V_{g1} and V_{g2} are

adjusted to the exact same driving signal. R_g is the gate driving resistance; L_g is the gate parasitic inductance introduced into the driving line; L_{d1} and L_{d2} are drain parasitic inductance caused by peripheral wiring of corresponding devices Q_1 and Q_2, L_{s1} and L_{s2} are source parasitic inductance caused by peripheral wiring of corresponding devices Q_1 and Q_2. L is the load inductor, Q_m is the SiC MOSFET power semiconductor, the KS pole is connected with the Tc pole, so that it can play the role of continuing current after the device is turned off. C_p is the parasitic capacitance of the load inductor and power semiconductor. U_{DC} is the DC bus voltage and C_m is the DC bus capacitance[8].

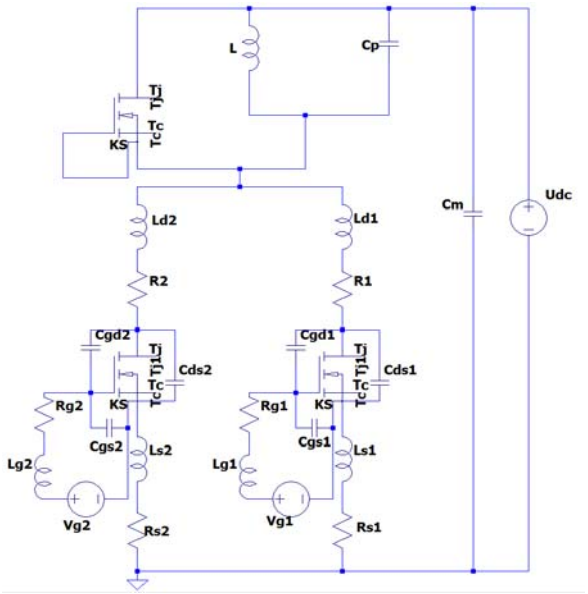

Figure 1. Test circuit diagram

2.2. Analysis of SiC MOSFET operating principle in parallel

Taking the test circuit shown in Fig.1 as an example, the static and dynamic current sharing between multiple SiC MOSFET devices is analyzed. In this case, there are three devices under test. The top test device is turned off by over-gate back-bias, and the switching characteristics of its diode are tested in the experiment. The bottom two SIC MOSFET devices are operated in parallel. In the test device, the opening and closing process of the lower tube is shown in the Fig.2 and Fig.3.

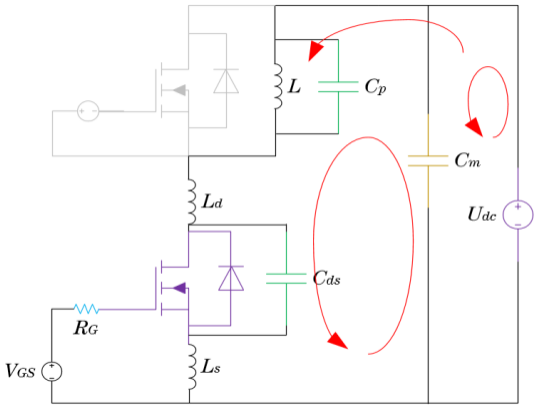

Figure 2. Simplified circuit of parallel SiC MOSFET opening process

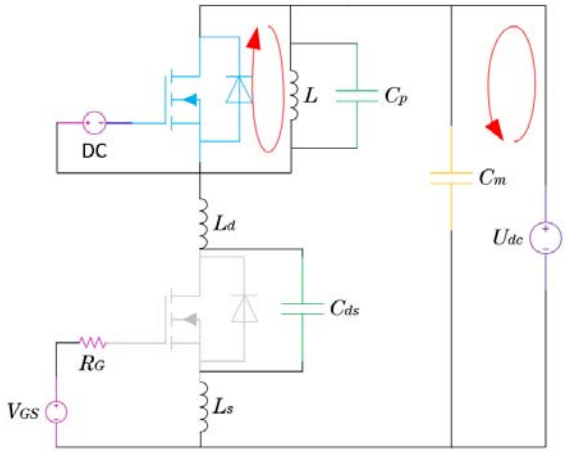

Figure 3. Simplified circuit of SiC MOSFET turn-off process in parallel

When the lower tube is turned on, the DC power supply and DC capacitance supply power to it together. When the lower tube is turned off, the current on the inductor L continues to flow through the anti-parallel diode of the upper tube. In the process of conducting the lower tube, the parasitic inductance of the bus and capacitor and the load inductance, the input capacitance of the load inductance C_p, and the parasitic capacitance of the device together constitute the power oscillation loop C_{ds}, forming the voltage and current oscillation[4].

3. Influence of Circuit Parameter Mismatch on Current Sharing

In an ideal situation, the parameters of the parallel devices are exactly the same. According to Ohm's law and Davenen's voltage theorem of closed loop, the voltage at both ends of the parallel devices is the same, the impedance on the parallel branch is the same, and the current must be the same. There will be no current imbalance in the process of parallel use. However, in the actual parallel use process of SiC MOSFET, the difference of various uncontrollable factors will lead to the occurrence of current imbalance. Circuit parameter mismatch is mainly reflected in the difference of drain and source parasitic inductances.

3.1. Effect of difference in drain inductance

By referring to the parameter table of SiC MOSFET device C3MOO32120K provided in official website of Wolfspeed, the order of magnitude of key values L_{d1} is obtained. For the convenience of comparison, the value which is easy to compare will be selected from the corresponding order of magnitude. The simulation experiment of drain inductance mismatch is carried out by LTspice, and the relevant data are shown in Tab.1.

Table 1. Test value of drain inductance mismatch

Device	*Size*	*Device*	*Size*	*Device*	*Size*	*Device*	*Size*
L_{d1}	*1nH*	L_{d2}	*10nH*	C_{gd1}	*10pF*	C_{gd2}	*10pF*
L_{g1}	*1nH*	L_{g2}	*1nH*	C_{gs1}	*1000pF*	C_{gs2}	*1000pF*
L_{s1}	*1nH*	L_{s2}	*1nH*	C_{ds1}	*100pF*	C_{ds2}	*100pF*
R_{d1}	*1mΩ*	R_{d2}	*1mΩ*	L	*100uH*	C_p	*1nF*
R_{g1}	*20Ω*	R_{g2}	*20Ω*	C_m	*1000uF*	U_{DC}	*500V*
R_{s1}	*20Ω*	R_{s2}	*20Ω*				

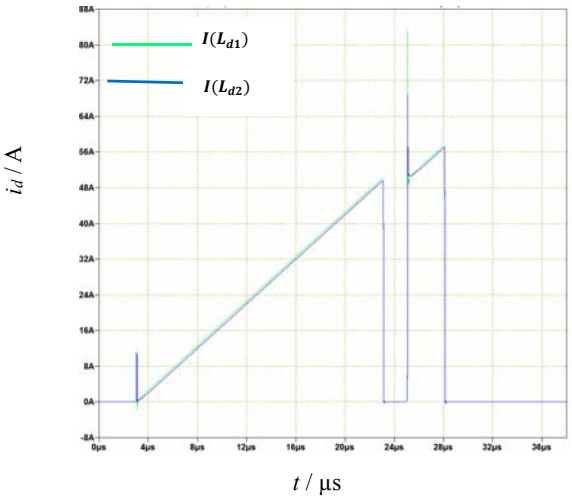

Figure 4. Simulation diagram of drain inductance mismatch

It can be seen from the Fig.4 that the inductance difference is mainly reflected in the influence on the switching instantaneous current change, which has little influence on the static current.

Table 2. Experimental results of drain inductance difference in static state

Type	*Node1/(μs,A)*	*Node2(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$
$I(L_{d1})$	5.63,6.09	22.11,47.23	2.496e+6	57.42
$I(L_{d2})$	5.63,6.71	22.11,47.78	2.493e+6	56.94

According to the static experimental data in Tab.2, the party with larger drain inductance bears less current and the current change rate is slower.

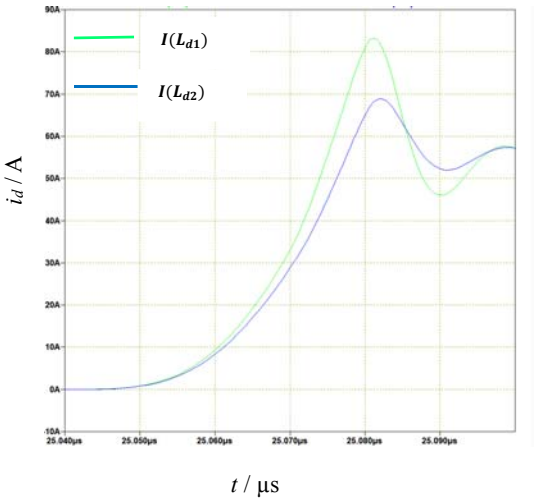

Figure 5. Simulation diagram of drain inductance mismatch at opening moment

Table 3. Experimental results of drain inductance difference at opening moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(L_{d1})$	25.06,8.19	25.08,72.10	3.4e+9	83.1	18.8
$I(L_{d2})$	25.06,6.98	25.08,61.13	2.7e+9	61.8	20.2

Through the simulation results of the opening moment in Tab.3, it can be inferred that the increase of drain inductance will lead to the decrease of current change rate and current peak value, result in the extension of the opening time.

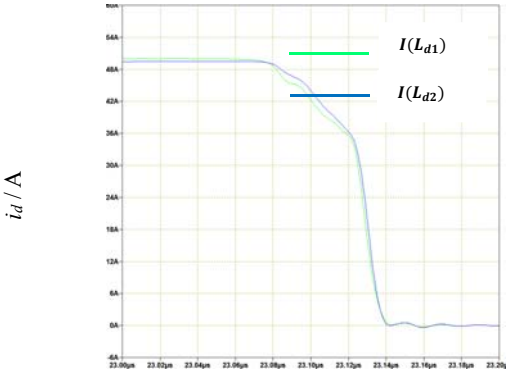

Figure 6. Simulation diagram of drain inductance mismatch at turn-off moment

Table 4. Experimental results of the difference in drain inductance at the turn-off moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(L_{d1})$	23.09,44.98	23.14,4.95	-9.5e+8	-49.7	41.7
$I(L_{d2})$	23.10,44.51	23.14,4.82	-1.1e+9	-49.5	36.8

Through the simulation results of the turn-off moment in Tab.4, it can be concluded that the increase of drain inductance in the turn-off process will lead to the increase of current change rate, the decrease of the maximum current difference, and the shortening of the turn-off time. However, the overall impact on the turn-off moment is negligible compared with the turn-on moment.

Based on the experimental results obtained from the data of 90% and 10% of peak values, it can be inferred that the branch with smaller parasitic gate inductance has a faster opening speed and a smaller current than the other branch. Overall observation shows that the drain parasitic inductance will cause sharp current oscillation after opening. With the increase of the drain parasitic inductance, the amplitude and frequency of current oscillation will decrease. After reaching a stable working state, the effect will almost disappear, and no obvious effect will be caused until the shutdown process.

3.2. Effect of source inductance difference

Refer to official website of Wolfspeed provided in the SiC MOSFET device C3MOO32120K parameter table, get the order of magnitude of the key value L_s.Set parameters as shown in Tab.5.

Table 5. Source inductance mismatch test values

Device	*Size*	*Device*	*Size*	*Device*	*Size*	*Device*	*Size*
L_{d1}	*1nH*	L_{d2}	*1nH*	C_{gd1}	*10pF*	C_{gd2}	*10pF*
L_{g1}	*1nH*	L_{g2}	*1nH*	C_{gs1}	*1000pF*	C_{gs2}	*1000pF*
L_{s1}	*1nH*	L_{s2}	*10nH*	C_{ds1}	*100pF*	C_{ds2}	*100pF*
R_{d1}	*1mΩ*	R_{d2}	*1mΩ*	*L*	*100uH*	C_p	*1nF*
R_{g1}	*20Ω*	R_{g2}	*20Ω*	C_m	*1000uF*	U_{DC}	*500V*
R_{s1}	*20Ω*	R_{s2}	*20Ω*				

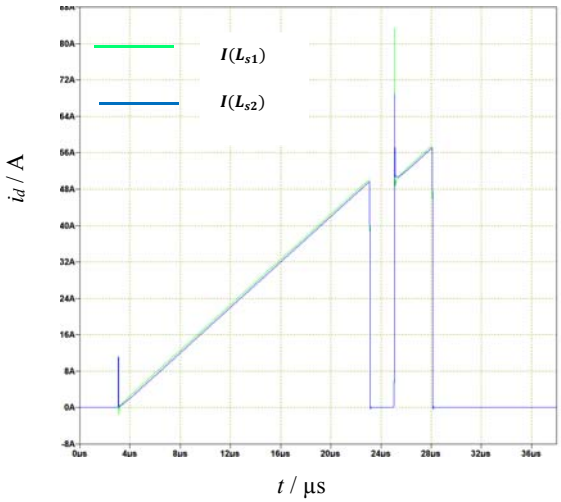

Figure 7. Simulation diagram of source inductance mismatch

Table 6. Experimental results of source inductance difference in static state

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$
$I(L_{s1})$	4.43,3.67	22.14,47.86	2.494e+6	57.47
$I(L_{s2})$	4.43,3.08	22.14,47.30	2.492e+6	56.94

According to the static data in Tab.6, the side with the larger source inductance is subjected to less current and the rate of current change is slower.

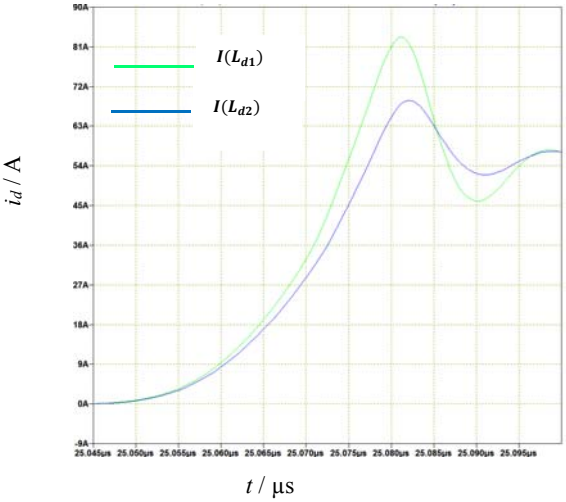

Figure 8. Simulation diagram of source inductance mismatch at the opening moment

Table 6. Results of source inductance difference at opening moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(L_{s1})$	25.06,8.21	25.08,74.69	3.4e+9	83.2	19.3
$I(L_{s2})$	25.06,6.84	25.08,61.96	2.7e+9	68.81	20.3

According to the static data in Tab.6, the side with the larger source inductance is subjected to less current and the rate of current change is slower.

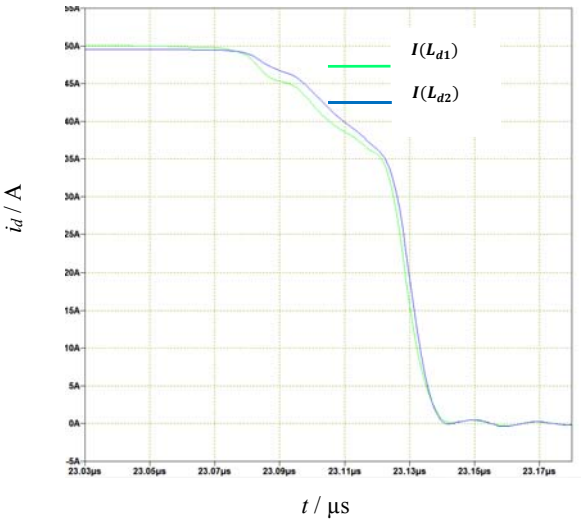

Figure 9. Dynamic diagram of source inductance mismatch at turn-off moment

Table 7. Results of source inductance difference at turn-off moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(L_{s1})$	23.09,44.96	23.13,5.06	-9.4e+8	-49.9	42.2
$I(L_{s2})$	23.09,44.50	23.13,4.87	-1.1e+9	-49.5	36.7

By selecting the data of experimental results obtained at two points, peak 90% and peak 10%, which can be inferred that on the branch with larger source inductance, the opening time of SiC MOSFET is relatively long, the turn-off time is short, and the overall switching time is relatively long. The tip current at the opening moment is small, as a result, the source parasitic inductance can be increased appropriately for the purpose of protecting the circuit. However, too much increase will reduce the switching speed.

3.3. Effect of parasitic capacitance C_{gs1} difference at gate source

Reference official website of Wolfspeed provided in the SiC MOSFET device C3MOO32120K parameter table, the order of magnitude of the gate source parasitic inductance is 10^3. To make the data more intuitive, set it to the integer data shown in Tab.8.

Table 8. Test values of gate-source capacitance mismatch

Device	*Size*	*Device*	*Size*	*Device*	*Size*	*Device*	*Size*
L_{d1}	*1nH*	L_{d2}	*1nH*	C_{gd1}	*10pF*	C_{gd2}	*10pF*
L_{g1}	*1nH*	L_{g2}	*1nH*	C_{gs1}	*1000pF*	C_{gs2}	*1200pF*
L_{s1}	*1nH*	L_{s2}	*1nH*	C_{ds1}	*100pF*	C_{ds2}	*100pF*
R_{d1}	*1mΩ*	R_{d2}	*1mΩ*	*L*	*100uH*	C_p	*1nF*
R_{g1}	*20Ω*	R_{g2}	*20Ω*	C_m	*1000uF*	U_{DC}	*500V*
R_{s1}	*20Ω*	R_{s2}	*20Ω*				

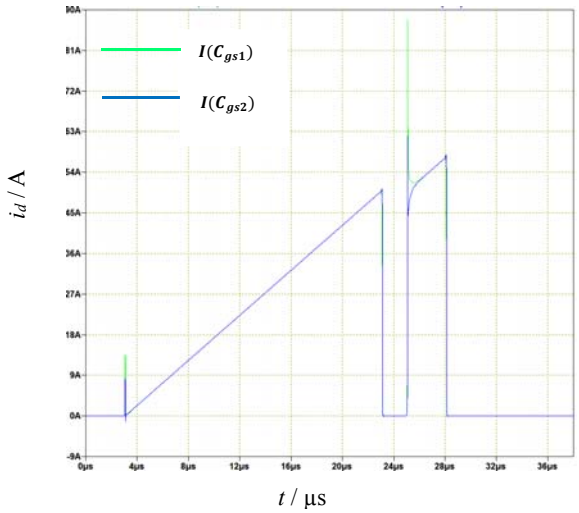

Figure 11. Simulation diagram of gate-source capacitance mismatch

Table 9. Experimental results of gate source capacitance difference in static state

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*
$I(C_{gs1})$	4.01,2.33	22.46,48.38	2.495e+6
$I(C_{gs2})$	4.01,2.34	22.47,48.38	2.495e+6

By observing the Fig.11 and the experimental data in Tab.9, it can be concluded that the mismatch of the gate-source capacitance will hardly bring any effect in the static process.

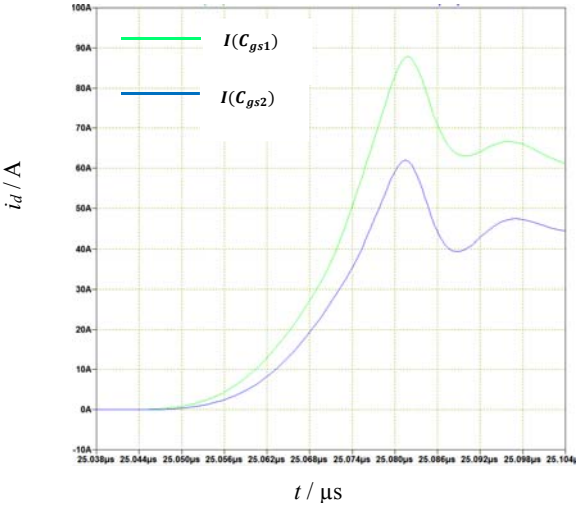

Figure 12. Simulation diagram of gate source capacitance mismatch at the opening moment

Table 10. Experimental results of parasitic capacitance difference of gate source at opening moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(C_{gs1})$	25.06,8.88	25.06,79.28	3.6e+9	88.2	19.6
$I(C_{gs2})$	25.06,6.19	25.08,55.46	2.6e+9	61.5	18.6

Through the simulation results of the opening moment in Tab.10, it can be inferred that the increase of the parasitic capacitance of the gate source will reduce the tip current, slow down the rate of current change, and shorten the opening time.

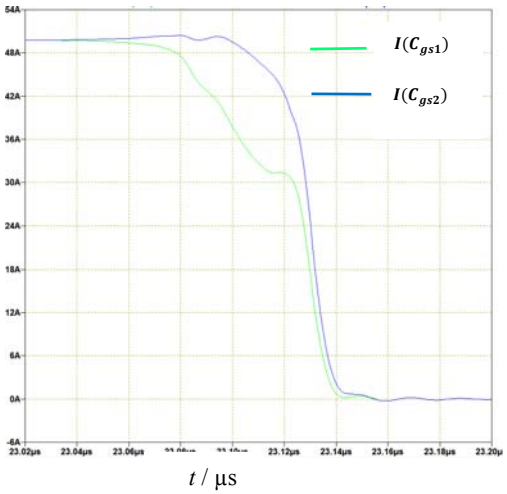

Figure 13. Simulation diagram of gate source capacitance mismatch at turn-off moment

Table 11. Experimental results of parasitic capacitance difference at the gate source at the turn-off moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(C_{gs1})$	23.08,44.84	23.14,4.84	-7.9e+8	-49.6	50.92
$I(C_{gs2})$	23.11,45.61	23.14,5.05	-1.8e+9	-50.0	22.39

By comparing the simulation results of the turn-off moment in Tab.11, it can be inferred that the increase of gate-source parasitic capacitance will lead to the increase of current change rate and maximum current difference during the turn-off process; however, the turn-off time will be shortened.

3.4. Effect of parasitic capacitance C_{gd} difference on gate-drain pole

By referring to the device parameter table of C3MOO32120K, the order of magnitude of gate-drain parasitic capacitance can be obtained as 10^1. To facilitate the comparison of the impact on current changes, the parasitic parameters of gate-drain capacitance will be increased in the same proportion as shown in Tab.12.

Table 12. Gate drain capacitance mismatch test values

Device	*Size*	*Device*	*Size*	*Device*	*Size*	*Device*	*Size*
L_{d1}	*1nH*	L_{d2}	*1nH*	C_{gd1}	*10pF*	C_{gd2}	*12pF*
L_{g1}	*1nH*	L_{g2}	*1nH*	C_{gs1}	*1000pF*	C_{gs2}	*1000pF*
L_{s1}	*1nH*	L_{s2}	*1nH*	C_{ds1}	*100pF*	C_{ds2}	*100pF*
R_{d1}	*1mΩ*	R_{d2}	*1mΩ*	*L*	*100uH*	C_p	*1nF*
R_{g1}	*20Ω*	R_{g2}	*20Ω*	C_m	*1000uF*	U_{DC}	*500V*
R_{s1}	*20Ω*	R_{s2}	*20Ω*				

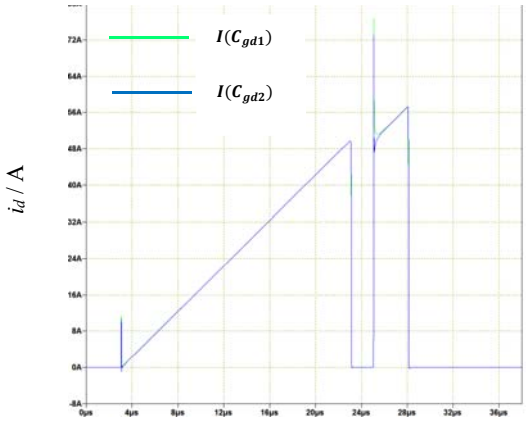

Figure 14. Simulation diagram of gate capacitance mismatch

Table 15. Experimental results of gate drain capacitance difference in static state

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*
$I(C_{gd1})$	4.82,4.36	20.71,44.02	2.495e+6
$I(C_{gd2})$	4.82,4.36	20.71,44.02	2.495e+6

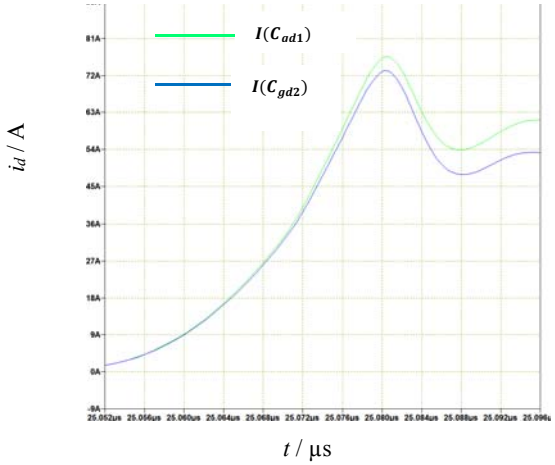

Figure 15. Dynamic diagram of gate drain capacitance mismatch at opening moment

Table 16. Experimental results of difference of gate drain parasitic capacitance at opening moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(C_{gd1})$	25.06,7.70	25.08,69.34	3.2e+9	77.09	19.07
$I(C_{gd2})$	25.06,7.19	25.08,65.53	3.0e+9	72.73	19.11

Through the simulation results at the opening moment in Tab.16, it can be inferred that the increase of gate-drain parasitic capacitance will lead to the decrease of current change speed and peak current during the opening process, but will prolong the opening time.

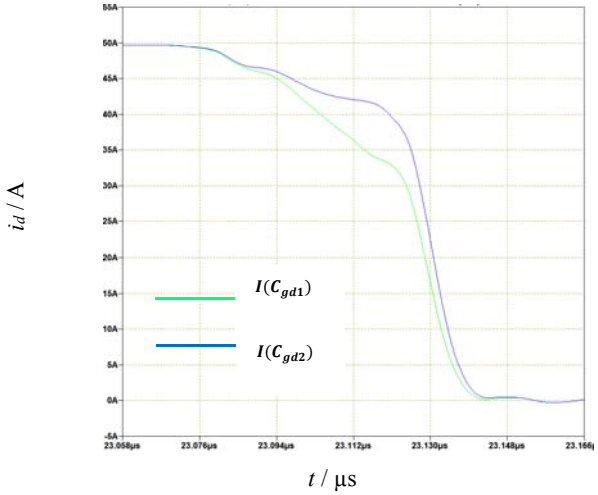

Figure 16. Dynamic diagram of gate-drain capacitance mismatch at turn-off moment

Table 17. Results of gate-drain capacitance differences at the moment of turn-off

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(L_{d1})$	23.09,44,72	23.14,4.91	-9.6e+8	-49.6	41.59
$I(L_{d2})$	23.10,44.72	23.14,5.00	-1.1e+9	-49.4	36.97

According to the simulation results of the turn-off moment in Tab.17, it can be inferred that the increase of gate-drain parasitic capacitance will lead to not only the increase of current change speed, but also the decrease of current change and the shortening of turn-off time in the turn-off process.

3.5. Influence of device temperature difference

Due to the asymmetric heat dissipation condition and asymmetric aging of the device, the junction temperature of the device will be different during operation. Since many characteristic parameters of SiC MOSFET devices are extremely sensitive to temperature, the difference of operating temperature of devices could also affect the unbalance current of parallel devices. In the on-state, the temperature function of the on-resistance R_{dson} is shown below.

$$R_{dson}(T_j) = R_{dson}(25^oC)(1+\frac{\alpha}{100})^{T_j-25^oC} \quad (1)$$

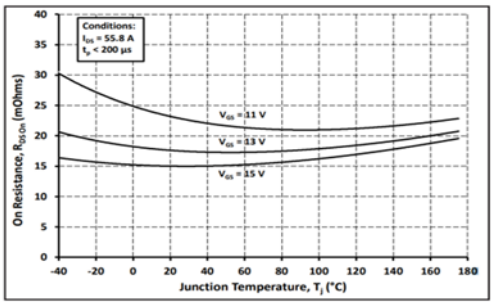

Figure 17. Curve of Rdson and temperature change

Combined with Rds and temperature change curve, as shown in Fig.17, under normal working conditions, with the increase of temperature, the resistance value of the on-resistance will increase. In order to detect the specific influence brought by temperature, Tj1 = 50 C and Tj2 = 75 C were set during the experiment.

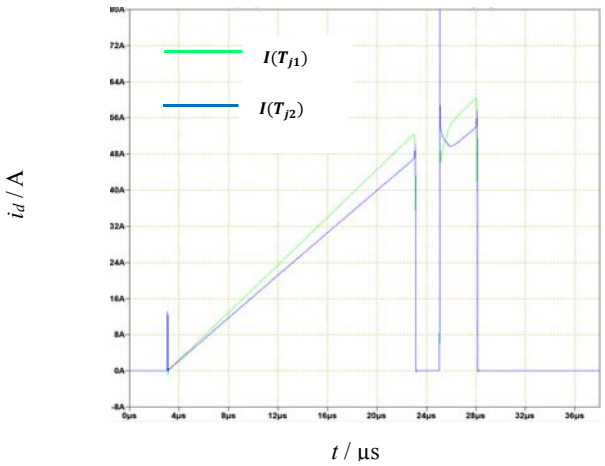

Figure 18. Simulation diagram of temperature mismatch

Table 18. Temperature differences in static results

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$
$I(T_{j1})$	5.42,6.12	21.57,48.70	2.63e+6	60.37
$I(T_{j2})$	5.42,5.60	21.57,43.61	2.35e+6	54.00

By comparing the simulation results of Tab.18 at different temperatures under static conditions, it can be inferred that the increase of node temperature will lead to the decrease of current change speed and peak current in the static working

process.

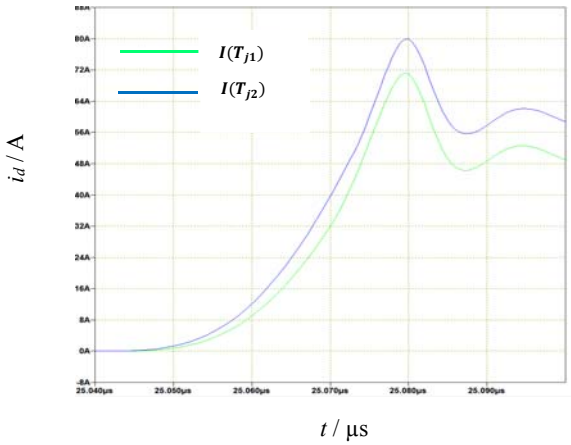

Figure 19. Simulation diagram of temperature mismatch at the opening moment

Table 19. Results of temperature difference at opening moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(T_{j1})$	25.05,7.17	25.08,64.44	3.1e+9	71.42	18.48
$I(T_{j2})$	25.06,7.90	25.08,71.48	3.2e+9	79.50	19.58

By comparing the simulation results of Tab.19 at different temperatures in the opening moment, the increase of node temperature will lead to the decrease of peak current during the opening process.

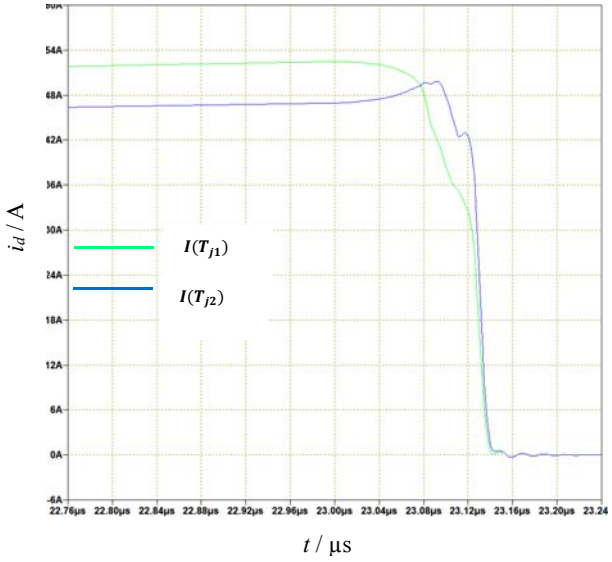

Figure 20. Simulation diagram of temperature mismatch at the turn-off moment

Table 20. Experimental results of temperature difference at the turn-off moment

Type	*Node1/(μs,A)*	*Node2/(μs,A)*	*di/dt*	$\Delta I_{MAX}/A$	$\Delta t_{max}/ns$
$I(T_{j1})$	*23.08,47.15*	*23.13,5.13*	*-7.87e+8*	*-52.32*	*53.38*
$I(T_{j2})$	*23.10,45.25*	*23.14,4.98*	*-1.31e+9*	*-49.76*	*30.53*

By comparing the simulation results of Tab.20 at different temperatures in the turn-off moment, it can be inferred that the increase of node temperature will lead to the increase of current change velocity and shortening of shutdown time during the shutdown process.

It can be found that with the increase of junction temperature, the on-resistance of the device increases and the threshold voltage decreases. In the steady state, experimental device one (junction temperature 50 degrees) shares more current than experimental device two (junction temperature 75 degrees). In the dynamic process, the junction temperature of the device is higher, the threshold voltage is smaller, and the current is larger

4. Conclusion and Prospect

4.1. Explore the most influential factors for current variation

To facilitate the comparison of drain inductance and source inductance, the influence degree of gate-source capacitance and gate-drain capacitance on the current change velocity, maximum current difference and opening time, the current change ratio is defined as the ratio of the current change velocity of two parallel devices to the current change value of the device without change. The time change ratio is the time change value of two parallel devices compared with the time change value of the device without change. The ratio of the maximum current difference of the two parallel devices is the maximum current difference of the device with no change in the ratio.

The specific formula is as follows:

Current change ratio:

$$\eta 1=\left|\frac{di_1/dt-di_2/dt}{di_1/dt}\right| \tag{2}$$

Maximum current difference ratio:

$$\eta 2=\left|\frac{\Delta t_{max1}-\Delta t_{max2}}{\Delta t_{max1}}\right| \tag{3}$$

Time change ratio:

$$\eta 3=\left|\frac{\Delta I_{MAX1}-\Delta I_{MAX2}}{\Delta I_{MAX1}}\right| \tag{4}$$

The relevant data are shown in the figure below：

Table 21. Ratio of drain inductance to source inductance in static state

Influence factor	η_1	η_2
Drain inductance	0.0012	0.0084
Source inductance	0.0008	0.0093

Table 22. Ratio of drain and source inductance parameters at opening moment

Influence factor	η_1	η_2	η_3
Drain inductance	0.199	0.256	0.073
Source inductance	0.212	0.172	0.052

Table 23. The ratio of the parameters of drain and source inductance at the turn-off moment

Influence factor	η_1	η_2	η_3
Drain inductance	0.136	0.003	0.117
Source inductance	0.142	0.084	0.130

By comparing the ratio of the change of the drain

inductance and the source inductance at static state, the turn-on moment and turn-off moment, it can be inferred that under static state, the drain inductance has a greater influence on the current change, and the source inductance has a greater influence on the peak current. At the opening moment, the influence of the drain inductor on the peak current and opening time is greater than that of the drain inductor with the same amplitude, and the influence of the current change speed is not as great as that of the drain inductor. At the turn-off moment, the source inductance has a greater impact on the current variation and the maximum difference of the current, but not as much on the turn-off time as the source inductance.

Table 25. Parameter ratios of gate-drain and gate-source capacitors at the opening moment

Influence factor	η_1	η_2	η_3
Gate drain capacitance	0.056	0.056	0.002
Gate source capacitance	0.265	0.302	0.048

Table 26. Parameter ratios of gate-drain and gate-source capacitances at the turn-off moment

Influence factor	η_1	η_2	η_3
Gate drain capacitance	0.123	0.004	0.111
Gate source capacitance	1.306	0.009	0.560

Since the data in the static state are too close to each other, we will not make a comparison here. At the opening moment, the impact of gate-source capacitance on current change rate, peak current and opening time is greater than that of gate-drain capacitance. At the turn-off moment, the gate-source capacitance has a greater effect on the current change rate, the maximum current difference and the turn-off time than the gate-drain capacitance.

4.2. Paper summarizes

In this article, through the analysis of circuit principle, device parameters mismatch analysis. Using the SIC MOSFET device provided in wolfspeed, the author explores the effect of circuit parameter mismatch on current sharing in parallel components. Through the quantitative analysis of the images and data obtained by simulation, the influence of each factor on the current in different stages is obtained. By comparing the experimental data, the factor with the greatest influence on the current change in each link is obtained. Through the experiment of this article, we can more clearly get the influence of the device parameter mismatch on the current change of each link. In practical application, we can better improve the circuit parameters according to the actual needs to make the SiC MOSFET device play a greater role.

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