

Design of Multi channel Acquisition System for Phased Array Radar

Silong Li, Jixue Xiao*

College of Mechanical Engineering, Xihua University, Chengdu, Sichuan, China

*Corresponding Author: Jixue Xiao

Abstract: With the steady progress of digitization and information technology, the application field of phased array radar is expanding. At the same time, with the development of wireless communication technology, phased array radar is faced with the challenge of accurately identifying multiple targets in complex electromagnetic environment. The multi-channel acquisition system of phased array radar is the core part of phased array radar. The high performance multi-channel acquisition system has improved the multi-target detection accuracy and anti-interference ability of phased array radar fundamentally. The hardware design includes four main parts: power supply circuit, acquisition circuit, cache circuit and transmission circuit. The power supply circuit provides stable power for the whole system; The acquisition circuit mainly realizes the acquisition of signal by ADC chip and the analog-digital conversion. The cache circuit realizes the data cache of DDR3. The transmission circuit is to realize the communication between the system and the computer. In the software part, Xilinx Kintex-7 series FPGA is selected as the main control chip. The signal acquisition is realized by configuring clock chip and ADC chip. The digital signal is received by using Xilinx primitive. The signal frequency is reduced by digital down-conversion. Finally, construct UDP protocol stack to realize data transmission from system to computer. The results show that the system can run normally, the performance index is also within the specified range, and it has reliable practicability.

Keywords: Multi-channel; Phased Array Radar; FPGA.

1. Introduction

With the continuous development of science and technology, radar technology has also been innovated.^[1] Compared with traditional radar systems, phased array radar system has the characteristics of higher accuracy, versatility, strong anti-interference ability and high recognition rate of multiple targets, and is widely used in national defense, military, civil aviation, meteorology and other fields.^[2-4]

In the military field, phased array radar plays an important role, covering many aspects such as air defense, anti-missile, electronic warfare, and missile navigation. In the aspect of air and missile defense, phased array radar needs to monitor and analyze multiple targets to detect and track multiple targets at the same time. In electronic warfare, phased array radars can realize the recognition of signals to help jamming and countermeasures. In terms of missile navigation, phased array radar can assist missiles to achieve accurate strikes.^[5-6]

In the field of civil aviation, aircraft is one of the common means of transportation, with the characteristics of fast speed, wide coverage and high safety factor. The continuous increase of passenger flow puts forward high requirements for flight safety. In order to reduce the occurrence of open air accidents, phased array radar technology needs to be further developed. Phased array radar can quickly scan a wide range of airspace, accurately grasp the dynamics of the aircraft according to the returned information, such as the position of the aircraft, altitude, speed and heading information, etc., to provide efficient technical support for air control. Not only that, phased array radar can also be used to monitor low-level airport security, receive and identify low-flying drones, birds and other low-flying slow-flying small objects, for the airport to drive birds and aircraft low-flying to provide security.^[7-8]

Phased array radar also plays an important role in the field of meteorology. Phased array radar helps to improve the

accuracy of weather forecast, weather forecast can not only provide guidance for People's Daily life, but also can prevent disastrous climate. For example, according to the weather forecast to help people stay warm, early warning of typhoons, floods, mudslides and other natural disasters. Phased array radar can be used for meteorological detection, mainly embodied in severe weather monitoring and warning, precipitation monitoring and directional estimation, weather system structure analysis, wind field monitoring and so on.^[9-11]

To sum up, in the era of intelligence, the performance requirements of phased array radar systems are becoming more and more stringent. Therefore, it is of great significance to design a multi-target tracking, high adaptability and low cost phased array radar multi-channel acquisition system for national defense, military, civil aviation, meteorology and other fields.

2. Basic Theory Research and System Scheme Design

2.1. Basic Theory of Phased Array Radar

The whole system of phased array radar is mainly composed of antenna array, transceiver module (T/R module), driver (central signal generator), digital signal processor, computer terminal and so on. And the phased array radar has two working conditions of transmitting and receiving. The internal signal transmission process of the whole phased array radar system is shown in Figure 1.

The first is the transmission process, which generates radar signals in the central signal generator of the system, which are basically microwave signals modulated for transmission, and then the signal is sent to the T/R module, which is further amplified by the high power amplifier of the T/R module to ensure that there is enough power to be transmitted to the

antenna array. The signal not only needs to be amplified, but also needs to control the amplitude and phase of the signal to achieve the expected indicators, this step is achieved through the multi-function chip of the phase control in the T/R module. The phase control in the T/R module will adjust the phase of the signal emitted by each antenna unit to control the direction of the beam, and the amplitude control is to adjust the strength of the signal. To optimize the shape of the beam. The signal processed by the T/R module is transmitted to the various units of the phased array antenna, which receives these signals and makes corresponding phase and amplitude adjustments according to the control signal. By precisely controlling the phase and amplitude of each antenna unit, phased array radar is able to form a narrow, focused beam and point it in a

specific direction. The adjusted signal is transmitted from the antenna unit to form a radar beam, which is used to detect targets.

And then there's the reception process. When the radar beam meets the target, part of the signal will be reflected back, and the reflected signal will be received by the phased array antenna, and the received signal will be sent back to the T/R module. The low noise amplifier (LNA) of the T/R module amplifies the received signal, which is then sent to the receiver for filtering, digital down-conversion, analog-to-digital conversion (A/D conversion), i.e. field programmable gate array (FPGA), and subsequent general-purpose computer processing.

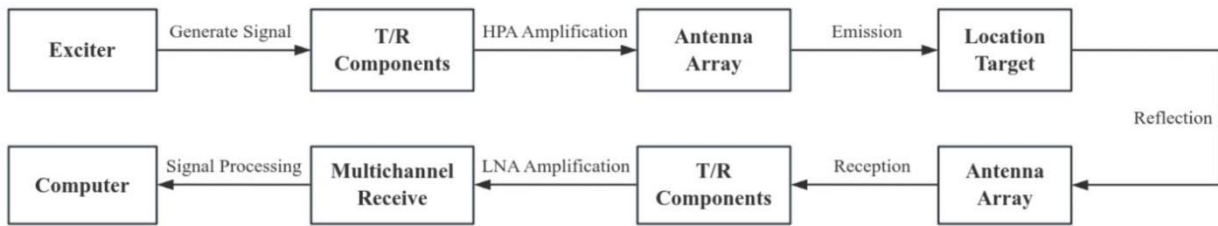


Figure 1. Signal Transfer Flow Diagram Within the System

2.2. Basic Theory of Digital Down-Conversion

Digital Down-Conversion plays a key role in modern communications and science and technology, especially in the fields of wireless communications, radar, satellite communications and software defined radio (SDR). In wireless communication, such as the antenna receives the RF signal, the direct processing cost is high and difficult, then through DDC, the signal is down-converted to IF or baseband, reducing the sampling rate, hardware requirements and system power consumption, simplifying the signal processing process, improve efficiency. The following is a brief discussion of the principles of DDC.

Digital Down-Conversion is usually composed of digital mixer, numerical control oscillator (NCO), filter, extractor,

etc. The digital mixer multiplies the input signal with the orthogonal signal generated by the NCO to achieve frequency down-conversion. After mixing, the signal is converted to the complex I and Q components of the baseband. NCO is the core component of Digital Down-Conversion, used to generate sine wave or cosine wave related to the frequency of the input signal, mainly composed of phase accumulator, phase adder and sin/cos table read-only memory, the role of NCO is to move the frequency of the input signal down to the baseband. The filter is usually a low-pass filter, which is used to filter out the high-frequency signals generated during the mixing process. Finally, the extractor is used to reduce the sampling rate of the signal. The basic structure of Digital Down-Conversion is shown in Figure 2.

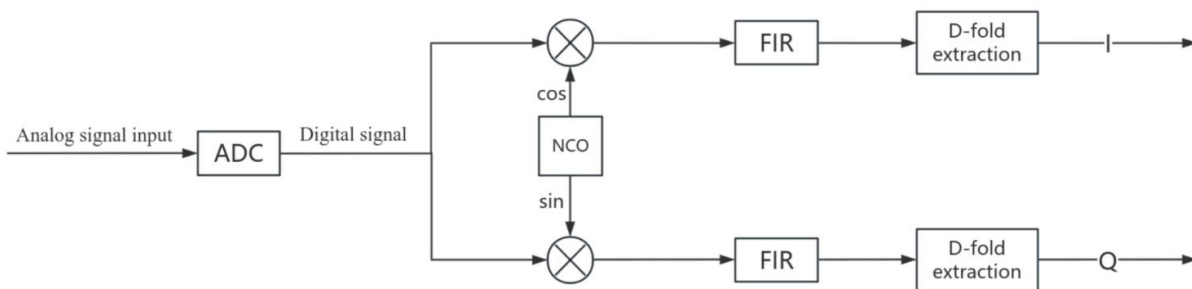


Figure 2. Basic Structure Diagram of Digital Down-Conversion

The initial analog signal is sampled, quantized, and converted to a digital signal by an ADC, while the NCO generates a sine and cosine signal that matches the frequency of the IF signal. The numerical control oscillator then multiplies the signal with the sine and cosine signal, thereby achieving a downward shift in frequency. The signal after mixing includes the target baseband signal and other high-frequency component signals. At this time, FIR digital filter is also needed to digitally filter the multiple frequency signals after mixing, filter out the high-frequency signal through the low-pass filter, and retain the target baseband signal to ensure

that spectrum aliasing will not occur during the extraction process. After analog-to-digital conversion, the sampling rate of digital signals is usually relatively high to meet the Nyquist sampling theorem. A high sampling rate will generate a large amount of redundant data, which increases the burden of storage and processing and is not conducive to subsequent work. During the extraction process, the sampling rate can be dynamically adjusted according to the actual bandwidth of the signal to match the bandwidth of the signal. After extraction, more efficient signal processing and analysis can be achieved.

2.3. Basic Theory of Digital Filter

Digital Filter is a kind of filter based on digital signal processing technology, which changes the relative proportion of signal frequency components by numerical operation, or filters out some frequency components, and is widely used in signal processing field. In the communication system, it is used to remove noise and adjust the signal spectrum to meet the frequency band requirements, and improve the reliability and accuracy of data transmission. In the biomedical field, digital filters are used to deal with electrocardiogram and electroencephalogram interference and noise, making medical signals clearer and more accurate. In audio processing, digital filters are widely used in noise reduction, equalization, reverberation and other processing processes. In image processing, digital filters are used for denoising, edge detection, image enhancement, etc. In radar signal processing, digital filter removes background noise, antenna sidelobe interference, ground reflection and other interference, and improves the radar system's detection capability and resolution of target information.

The FIR filter is mentioned in the introduction of the basic theory of digital down-conversion, and the FIR filter is briefly introduced. There are many kinds of digital filter classification, according to the implementation structure can be divided into FIR filter and IIR filter. FIR filter has the characteristics of non-distortion and high stability compared with IIR filter. Let the input signal be denoted as $x(n)$, the output signal as $y(n)$, and the impulse response of the digital filter as $h(n)$. The mathematical relationship among these three quantities can be formulated as:

$$y(n) = \sum_{k=-\infty}^{+\infty} h(k) \cdot x(n - k) \quad (1)$$

For FIR digital filter, the unit impulse response number of finite length digital filter is finite length. It is satisfied that:

$$h(n) = 0, \quad k < N_1, k \geq N_2 \quad (2)$$

N_1 and N_2 are finite values, N_1 is usually set to zero,

$N_2 = N$, FIR filter does not equal zero in $0 \leq k < N - 1$, the equation 2 can be converted to:

$$y(n) = \sum_{k=0}^{N-1} h(k) \cdot x(n - k) \quad (3)$$

FIR filter frequency response can be expressed as:

$$H(e^{j\omega}) = \sum_{k=0}^{N-1} h(k) e^{-j\omega k} \quad (4)$$

2.4. Design of Multi-Channel Signal Acquisition System

Through the understanding of the basic theory of Phased Array Radar, Digital Down-Conversion and Digital Filter, we can know that the process of signal reception is very important in phased array radar system. This paper mainly focuses on the signal acquisition system of Phased Array Radar, that is, the analog signal needs to be collected, the digital signal needs to be processed by Digital Down-Conversion, and then the baseband signal after filtering is transmitted.

The signal receiving process structure of phased array radar is shown in Figure 3. First, the antenna array needs to receive the reflected electromagnetic wave signal, and then the system will preprocess the signal into the analog signal inside the phased array radar and amplify it. The RF processing unit moves the frequency of the analog signal to the frequency range collected by the AD. This is followed by the multi-channel signal acquisition system designed in this paper, which is shown in the dotted line box in Figure 3. The preliminary analysis of the system can be learned that it needs to be composed of five parts, the first is AD acquisition, analog signal acquisition and conversion into digital signal. The second part is data processing, converting the IF digital signal into a baseband signal. The third part is the signal transmission, the processing of the packaged data signal is transmitted to the PC for subsequent processing. The fourth part is the clock, which provides a stable clock for each part. The fifth part is the power supply to ensure the stable operation of the system.

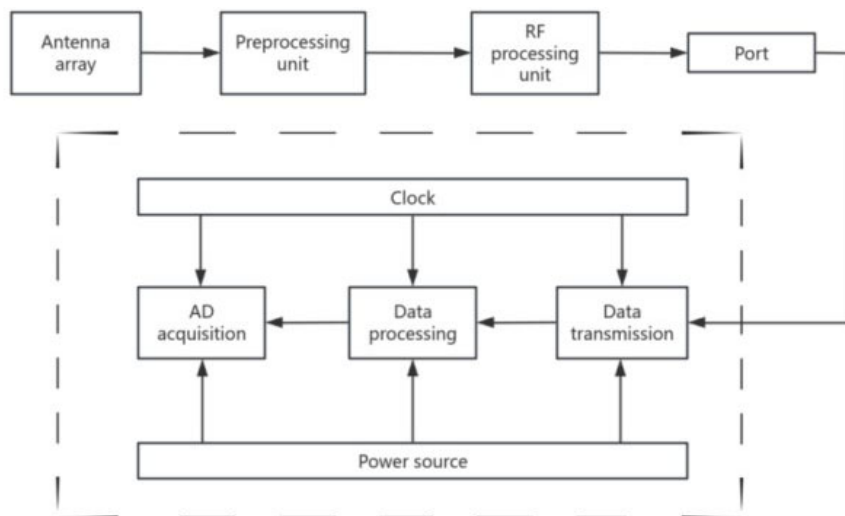


Figure 3. System Structure Diagram

2.4.1. AD Collection Scheme

In AD acquisition, the ADC chip acts as a bridge between

analog signals and digital signals. The performance of an ADC chip is usually the key to affect the application field of

a system, so it is very important to choose an ADC chip that meets the engineering practice. In this paper, ADS62P29 is selected as the AD acquisition process analog-to-digital

conversion chip, Its internal function block diagram is shown in Figure 4.

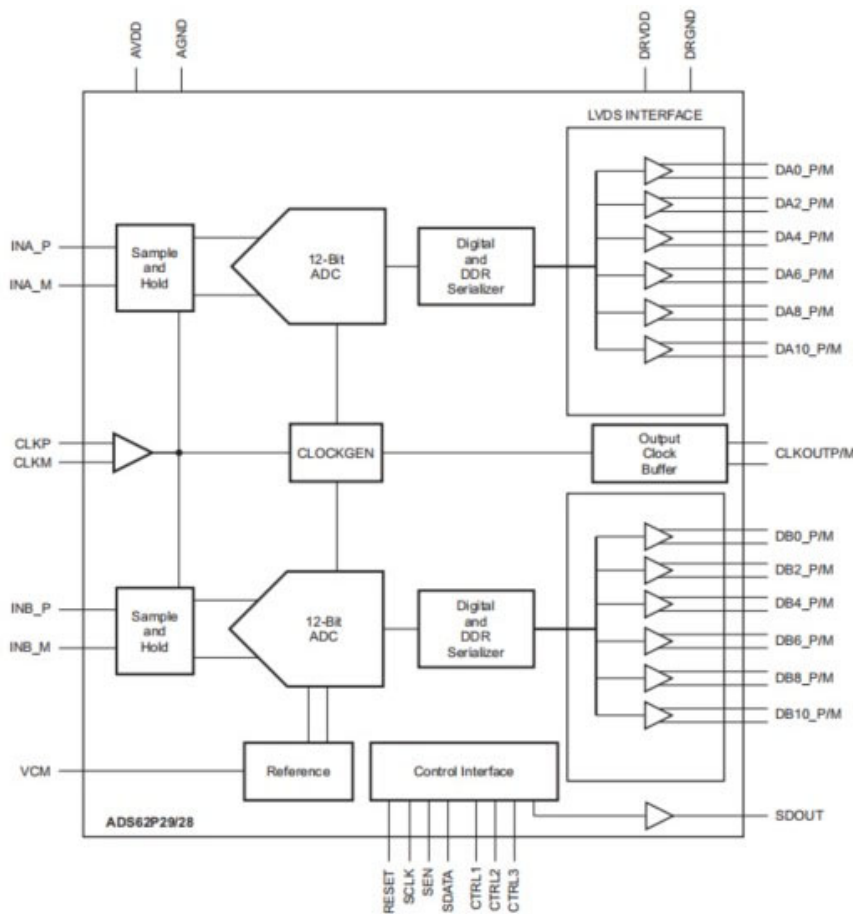


Figure 4. ADS62P29 Block Diagram

2.4.2. Data Processing Scheme

Digital signal processing chip can be divided into ASIC, DSP, FPGA. The data processing process is mainly the Digital Down-Conversion processing of the received signal. The following is the analysis of three proposed schemes to achieve Digital Down-Conversion.

(1) Digital Down-Conversion based on ASIC. ASIC is a kind of customized integrated circuit designed for a specific application, which can realize various functions according to the needs of the project. In the realization of Digital Down-Conversion, ASIC can directly implement the down-conversion algorithm through hardware logic, usually including mixing, filtering and extraction operations.

(2) Digital Down-Conversion based on DSP. DSP is a microprocessor specially used for digital signal processing, which realizes Digital Down-Conversion algorithm through C/C++ or assembly language. DSP can perform mixing, filtering and extraction operations through instruction set.

(3) Digital Down-Conversion based on FPGA. An FPGA is a programmable logic device that can implement a Digital Down-Conversion algorithm using a hardware description language such as VHDL or Verilog. The logic unit inside the FPGA can be configured according to the needs to realize the functions of mixing, filtering and extraction.

In the realization of digital down-conversion, FPGA, ASIC, DSP are three common technology choices. Each technology

has its own unique advantages and limitations and is suitable for different application scenarios. The three scenarios are illustrated in Table 1.

Table 1. Comparison List of ASIC, DSP, FPGA

	ASIC	DSP	FPGA
Property	Extremely high	Intermediate	High
Power Dissipation	Low	Higher	Higher
Flexibility	Low	High	High
Development Cost	High	Low	Intermediate
Development Cycle	Long	Short	Intermediate

Overall consideration, choose to use FPGA to achieve digital down-conversion. Xilinx FPGA has richer logic resources, more comprehensive IP core, more flexible wiring mode and more friendly development environment, so XC7K325T in Kintex-7 series is adopted as the main controller of this system in this paper. The main parameters are shown in Table 2.

Table 2. Main Parameters Table

Name	Parameters
Pin Count	676
Package Size	27mm×27mm
Pin Spacing	1mm
Logic Cells	326080
LUTs	203800
Flip-Flops	407600
Block RAM	16020
DSP Slices	840
CMT	10
Speed Class	-2
Operating Temperature Range	-40°C~100°C

2.4.3. Data Transmission Scheme

Ethernet is a local area network communication protocol that supports multiple transmission rates and uses the CSMA/CD mechanism. Ethernet has the characteristics of long distance transmission, high broadband, flexible network topology, and wide compatibility. In this system, the signal interface from FPGA to PC is realized by PHY chip YT8511. There is a lot of data in the transmission process, so in the hardware design will consider a memory as a data cache, the design uses NT5CC128M16IP-DI as a signal transmission process cache.

2.4.4. Clock Scheme

A Phased Array Radar receiving system consists of several receiving channels, each of which requires precise time synchronization and phase consistency to ensure the coherence of the received signals. The high precision synchronization of clock signal can effectively reduce the phase error and improve the detection accuracy and resolution of Phased Array Radar. Through the high precision clock synchronization, the precise sampling and phase alignment of multi-channel received signals can be realized, thus improving the coherent accumulation performance of Phased Array Radar.

In this system, the LMK04906 clock chip is used in the AD acquisition process. The chip is a high-performance clock jitter attenuator and clock distributor, which is widely used in the fields requiring low jitter and high precision clock signals. It can receive multiple input clock signals and generate

multiple output clock signals of different frequencies, which is suitable for a variety of high-speed communication and data processing scenarios, with low jitter, low power consumption, and improved signal integrity performance. For FPGA clock, the clock accuracy required is relatively low, and its drive clock uses 100M NSC5344B-100M crystal oscillator.

2.4.5. Power Source Scheme

The high reliability and stability of the power supply is the basis of the normal operation of the phased array radar receiving system. The power supply provides stable electric energy for each component of the phased array radar receiving system, which requires accurate current and voltage supply to ensure the normal operation of the system. In this system, high sensitivity is needed to detect weak echo signals and wide dynamic range is needed to process signals of different intensity. The stability of the power supply directly affects these performance indexes. Not only that, the system also needs to respond quickly to the change of the target signal, and the fast response ability of the power supply can ensure that the stable power supply can be provided when the load changes, so as to ensure the real-time performance of the system. In short, a stable and efficient power supply not only supports the operation of all aspects of the system, but also the key to ensuring system performance and reliability.

In this system, JW5060T and AMS1117 chips are selected to provide stable power management. The JW5060T is a single-chip buck switch regulator based on the I2C architecture, with a low-voltage design that reduces energy loss and improves efficiency. JW5060T internal design of a variety of protection circuits to ensure the stability of the chip in complex environments. AMS1117 is a low-voltage differential linear regulator, and JW5060T jointly bear the power supply of each module of the system.

3. Hardware Design of MULTI-CHANNEL Acquisition System

3.1. Clock Chip Circuit

The pins of the LMK04906 can be divided into power and ground pins, input clock pins, output clock pins, control interface pins, and other functional pins. The output pin of LMK04906 has OUT0 to OUT11, that is, it can output a maximum of 6 groups of LVPECL differential clock signals, and its circuit schematic is shown in Figure 5.

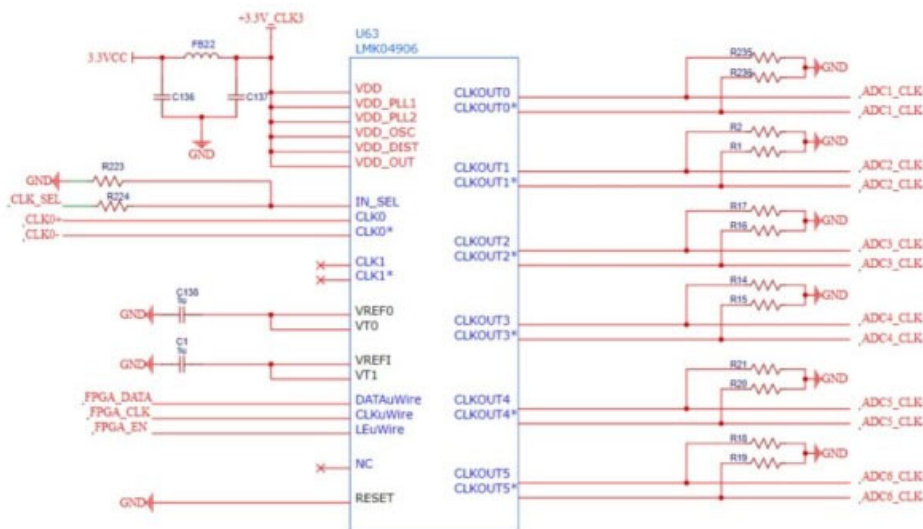


Figure 5. LMK04906 Circuit Schematic Diagram

3.2. Analog to Conversion Chip Circuit

The ADS62P29 has two power supplies, where the AVDD is connected to a 3.3V input and the DRVDD is connected to a 1.8V input. The input of the CLK_P and CLK_M pins comes from the output of the LMK04906 clock chip. The digital output pins and control interface pins of the ADS62P29 are connected to the FPGA. For the FPGA, the

signal output of the digital output pin is used as the input of the FPGA, and the digital signal after the conversion of the ADS62P29 is further processed, and the output signal of the FPGA is used as the input of the ADS62P29. The configuration and working mode of ADS62P29 can be changed through the control interface pin. Figure 6 shows the circuit schematic diagram of the ADS62P29.

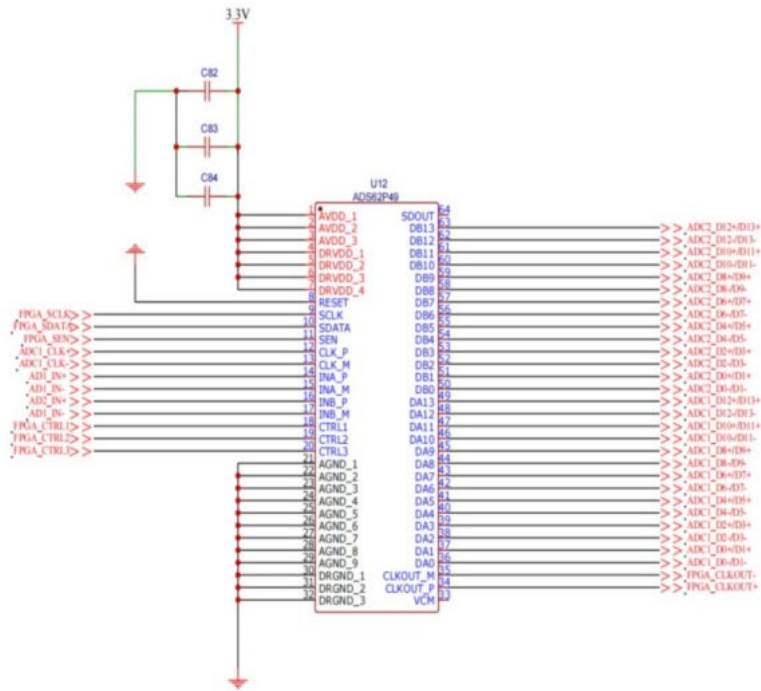


Figure 6. ADS62P29 Circuit Schematic Diagram

3.3. Data Cache Circuit

DDR3 SDRAM is the third generation of DDR, compared with DDR2 has better performance and faster transmission speed, DDR is also called double data rate, its biggest feature

is the bilateral edge trigger, that is, the rising edge and falling edge of the clock can be read and write data, can quickly store and send a large number of data. The circuit schematic diagram of NT5CC128M16IP-DI is shown in Figure 7.

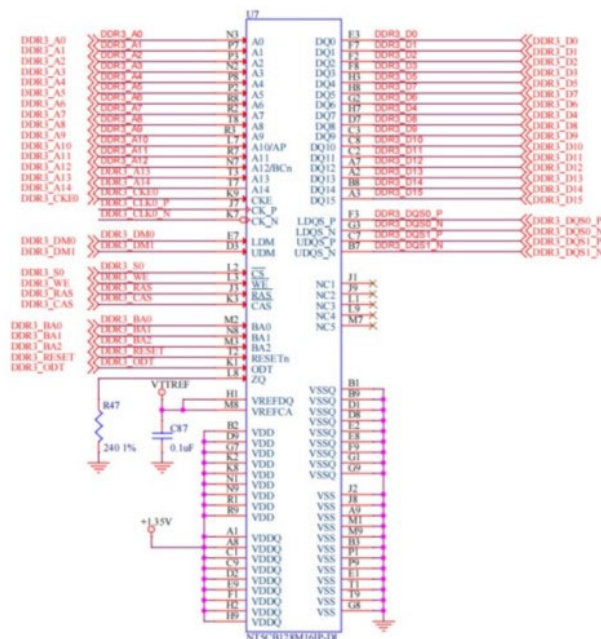


Figure 7. NT5CC128M16IP-DI Circuit Schematic Diagram

3.4. Data Transmission Circuits

During signal transmission, the FPGA sends the packaged

data to the PC through RJ45 after YT8511 processing. The circuit schematic diagram of Ethernet PHY chip YT8511 is shown in Figure 8.

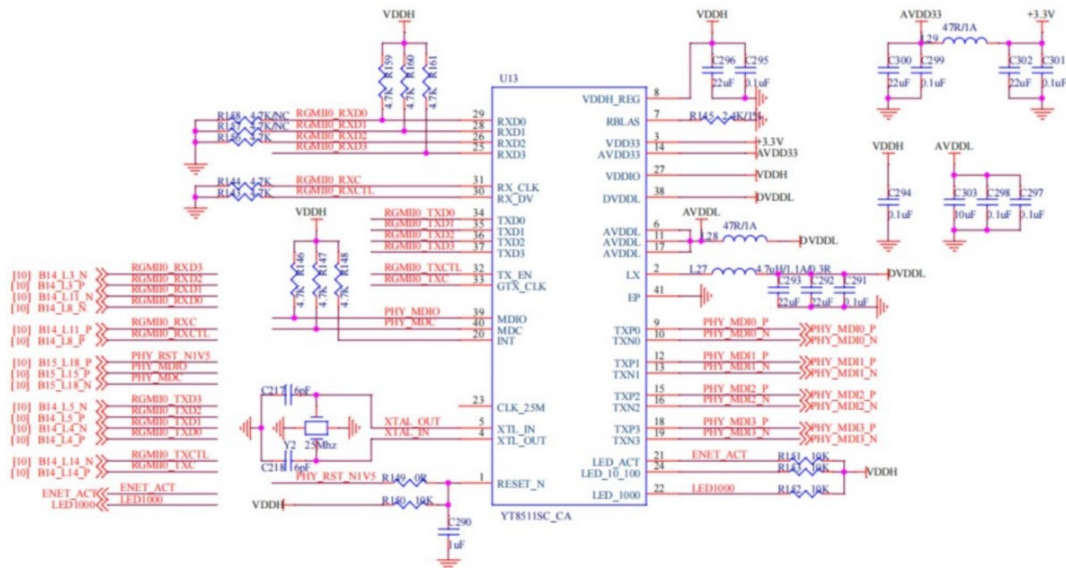


Figure 8. YT8511 Circuit Schematic Diagram

4. Logical Design of MULTI-CHANNEL Acquisition System

FPGA is evolved from the basis of PAL, GAL, CPLD, and it is a semi-customized circuit in the field of ASIC, which can realize the functions of hardware circuits through logic code. The field of FPGA application can be divided into six categories: communication field, digital signal processing field, video image processing field, high-speed interface design field, artificial intelligence field and IC verification

field. In this design, the communication between the phased array radar multi-channel signal acquisition system and PC, the digital signal processing and the high-speed interface design in the process of signal transmission are realized by FPGA. FPGA, as the main controller, realizes the conversion of analog-digital signals by controlling ADS62P29, then processes and cache digital signals through its own internal logic resources, and finally transmits them out through the high-speed interface. Figure 9 is the working flow chart of the phased array radar multi-channel signal acquisition system.

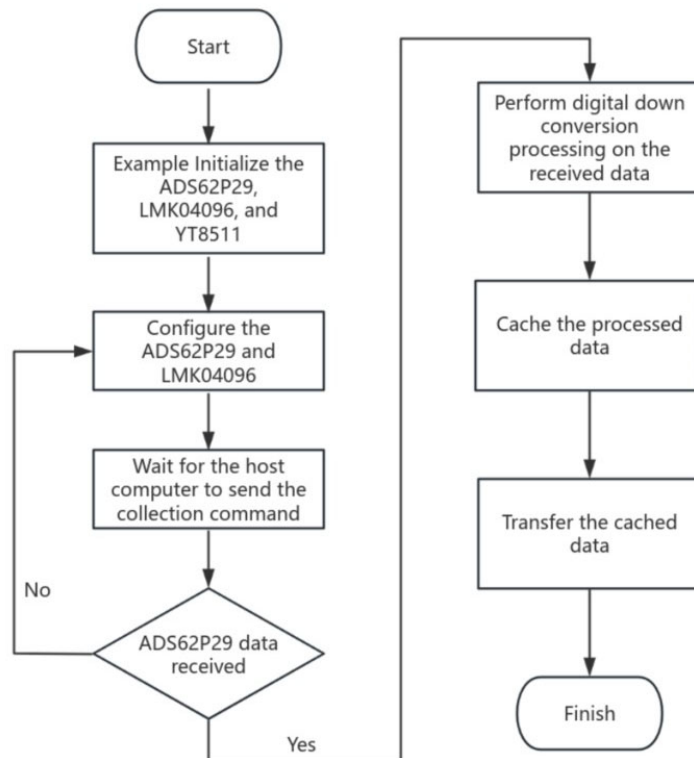


Figure 9. Multi-Channel Acquisition System Work Flow Chart

The operation process of the phased array radar multi-channel acquisition system is as follows: First, after powering the system, wait for each module of the system to warm up. Then the FPGA controls the ADC chip ADS62P29, the clock chip LMK04096 and the physical layer PHY chip for the initialization process. Then wait for the host computer to send the acquisition command, and the system starts to run. If the correct data is not received, the ADS62P29 and LMK04906 need to be re-configured. On the contrary, the FPGA performs digital down-conversion processing on the received data, and

then the FPGA caches the processed data to DDR3. Finally, the data in DDR3 is read and packaged into UDP datagram format and transmitted to the PC over Ethernet.

The main logical structure of the system consists of three parts: data receiving module, data processing module and data transmission module. Since a piece of ADS62P29 can process two IF analog signals, 16 IF analog signals only need 8 channels for processing. Take one channel as an example, and the schematic diagram of single channel logic is shown in Figure 10.

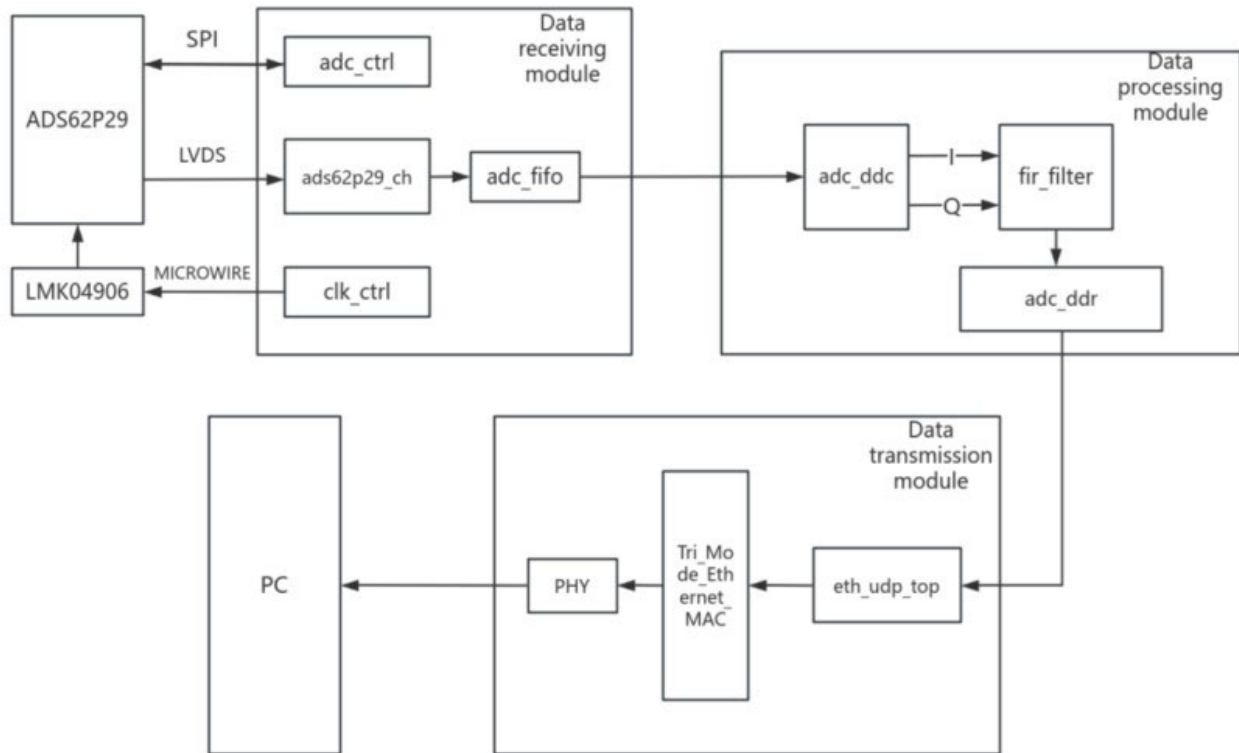


Figure 10. Multi-Channel Acquisition System Logic Diagram

In the data receiving module, FPGA configures LMK04906 clock chip through MICROWIRE protocol to supply stable clock signal to ADC chip ADS62P29. With stable clock and driver, ADS62P29 will collect analog signal and transform it analog-to-digital. Then the differential signal is output to the ads62p29_ch through the LVDS interface. In the ads62p29_ch, the differential signal is transformed into a single-ended signal that can be processed directly by the FPGA. Finally, these single-ended signals are cached in the adc_fifo. In the data processing module, FPGA will read the data in adc_fifo, and then through adc_ddc digital mixing processing of the data, through fir_filter low-pass filtering of the processed data, and finally the filtered baseband signal is cached in adc_ddr. In the data transmission module, eth_udp_top reads the data in adc_ddr and packages it into Ethernet frame format and implements the function of UDP protocol, and then realizes the signal transmission from data to PC through Tri_Mode Ethernet MAC IP core. The data collection, processing and transmission processes of the remaining channels are the same as above.

5. MULTI-CHANNEL Acquisition System Experiment

The multi-channel signal acquisition system of phased array radar needs accurate amplitude and phase control to achieve the flexibility of beam pointing. Generally, the amplitude deviation is required to be controlled within $\pm 1\text{dB}$ to ensure the accuracy of signal superposition. The phase consistency between channels is generally required to be within $\pm 2^\circ$ to ensure the positioning accuracy of the target. The amplitude and phase of the system are captured by vector network analyzer. The amplitude and phase data captured by the vector network analyzer will be sent to the computer through the command of the upper computer software, and the captured data will be converted and analyzed.

In order to more intuitively understand the amplitude variation of 1-16 channel signals, the line chart of amplitude variation as shown in Figure 11 is drawn based on the data obtained by the vector network analyzer. Where the horizontal and vertical coordinates are the number of routes and

amplitude respectively. The red line is the 16-way amplitude mean for comparison, and the blue line is the actual value, reflecting the amplitude change. The maximum difference of

signal amplitude between each channel is 0.98dB, which meets the range requirements of amplitude deviation.

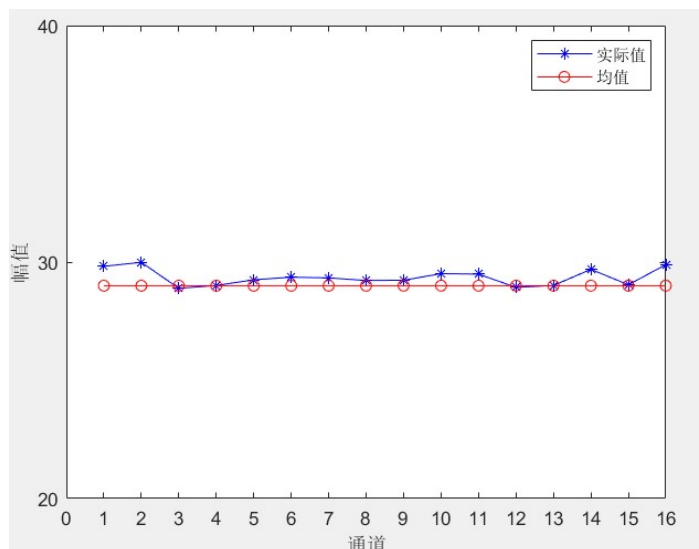


Figure 11. Amplitude Change Line Chart of 16 Channels

For phase deviation analysis, the line diagram of phase change as shown in Figure 12 is also drawn. The horizontal coordinate is the number of routes, and the vertical coordinate is the phase value. The blue phase mean value can clearly

reflect the change of the actual value of the red phase, and the maximum phase difference between each signal is 1.5° , which meets the deviation requirement of the phase value.

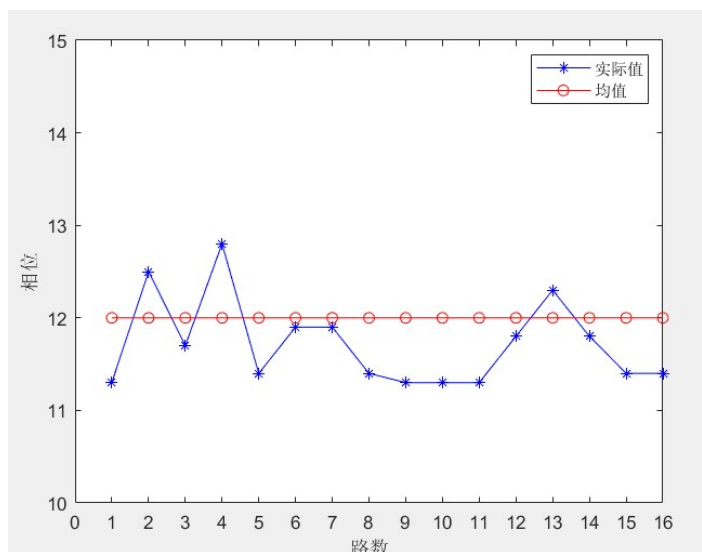


Figure 12. Phase Change Line Chart of 16 Channels

Under the same conditions, after many experimental tests, the amplitude and phase data obtained are within the specified range. Therefore, the multi-channel signal receiving system has better signal synchronization, signal superposition, signal acquisition accuracy, signal processing effectiveness and real-time signal transmission, which meets the index requirements of this topic.

References

[1] Yuhang W .Review of the Evolution of Phased-Array Radar[J].SHS Web of Conferences,2022,144

[2] Tsui James.Microwave receivers with electronic warfare applications [M]. The Institution of Engineering and technology, 2005

[3] Fields T W,Sharpin D L,Tsui J B.Digital channelized IFM receiver[J].1994,3:87-90

[4] Wu jiangfeng,Cusmai Giuseppe,Chou Acer Wei-Te. A 2.7 mW/Channel 48-1000 MHz Direct Sampling Full-Band Cable Receiver[J]. IEEE Journal of Solid-State Circuits, Volume 51, Issue 4,2016,845-859

[5] Nickel U R O.Subarray configurations for digital beamforming with low sidelobes and adaptive interference suppression[C] Radar Conference, 1995.,Record of the IEEE 1995 International. IEEE, 1995: 714-719.

- [6] Richardson P G, Adams F J, et al. PACER(Phased Array Concepts Evaluation Rig): design, development and adaptive beamforming experiments[C] Phased Array Systems and Technology, 2000. Proceedings. 2000 IEEE International Conference on. IEEE,2000:421-424.
- [7] Nuzhdin V M, Ananenkov A. E, and. Marin D. V, "Radar of Complex UAV Detection and Neutralization," 2021 Systems of Signals Generating and Processing in the Field of on Board Communications, Moscow: IEEE, 2021.
- [8] Singh H. and Sharma M., "Electronic Warfare System Using Anti-Radar UAV," 2021 8th International Conference on Signal Processing and Integrated Networks (SPIN), Noida: IEEE, 2021.
- [9] V. K S ,Kishore K K .Structure and evolution of organized precipitation bands: C-band doppler weather radar observations over Thumba (8.5o N, 77o E)[J].Atmospheric Research,2023,284.
- [10] Haiping G .Design and Implementation of the Weather Radar Mobile Monitoring System Based on WeChat Enterprise [J]. IOP Conference Series: Earth and Environmental Science, 2021,769(2):
- [11] Qutie J ,Haijiang W ,Shipeng H, et al.Echo simulation of dual polarization Doppler weather radar based on the physical model[J].EURASIP Journal on Wireless Communications and Networking,2020,2020(1):