

From 5G To 6G: Investigation on Efficiency Improvement of Millimeter Wave Power Amplifier

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Abstract. As wireless communication systems transition from 5G to 6G, developing millimeter-wave power amplifiers (PAs) that combine high efficiency and excellent linearity has become a key challenge in current research. However, challenges such as high peak-to-average power ratios (PAPR), wideband operation, and thermal constraints significantly hinder conventional PA architectures. This review systematically examines recent advances in millimeter-wave PA development for 5G/6G systems. Two primary avenues are highlighted. First, architectural innovations include broadband matching networks, Doherty/outphasing topologies, digital predistortion (DPD), envelope tracking (ET), and their hybrid implementations. Second, material technologies involve GaN/CMOS process optimization, thermal management, and advanced packaging. By analyzing the current research, we explore the fundamental trade-offs between efficiency, linearity, bandwidth, and integration density. We also outline future directions such as higher-frequency operation, intelligent adaptive design, and novel semiconductor materials for next-generation communication systems. The insights provided herein offer valuable guidance for the development of high-performance PAs tailored to future 6G communication systems.

Keywords: millimeter-wave communication, power amplifier efficiency, Doherty architecture, envelope tracking, GaN technology, 5G, 6G.

1. Introduction

As wireless communication systems advance from 5G to 6G, millimeter-wave power amplifiers (PAs)—key components in the radio frequency (RF) front end—face unprecedented challenges in the simultaneous optimization of efficiency and linearity [1,2]. The demanding requirements of the high peak-to-average ratio (PAPR >10 dB) of 5G NR signals and the potential terahertz frequency band (100-300 GHz) of 6G have resulted in significant bottlenecks in efficiency, bandwidth, and thermal management for conventional PA architectures [1-3]. Empirical studies indicate that the power added efficiency (PAE) of millimeter-wave PA (24.25-52.6 GHz) is 30% -50% lower than that of sub-6 GHz, which is mainly limited by high-frequency parasitic, interconnection loss (0.2-0.5 dB/mm) and thermal density (>500 W/cm²) [4-6]. To address these challenges, researchers and engineers have proposed a broad range of technological innovations, encompassing novel device architectures, advanced material platforms, and intelligent algorithmic approaches for coordinated optimization. Architecturally, Doherty power amplifiers enhance efficiency by 30–40% in the 6–12 dB power back-off (PBO) range through load modulation techniques [4,7]. For example, the 28 GHz GaN Doherty PA reported in [3] achieved a PAE of 42.3% at 6 dB back-off, while the continuous mode (CM) Doherty design proposed in [8] further extended the bandwidth to 10-14 GHz. The outphasing PA generates a constant envelope signal through amplitude-phase conversion, achieving a PAE of 29-31.8% and a saturated power of 37-38.7 dBm in the 24-28 GHz band [7]. However, its phase sensitivity and synthesis loss still need to be optimized [9]. In addition, the hybrid strategy of envelope tracking (ET) and digital predistortion (DPD) improves the 6 dB back-off PAE from 25% to 42% through dynamic power supply adjustment and predistortion compensation, while supporting 5 GHz ultra-wideband operation [10-12]. Breakthroughs in materials and integration technology also provide new paths for improving PA performance. Gallium nitride (GaN) can achieve a power density of 4-6 W/mm in the millimeter-wave band due to its high electron mobility (>2000 cm²/V·s) and wide bandgap characteristics (3.4 eV) [13]. Three-dimensional heterogeneous integration technology vertically stacks GaN PA and CMOS control circuits through silicon interposers, achieving a 3 dB

linearity improvement using LSTM networks [10]. However, this type of integration solution faces the severe challenge of a heat density of 500 W/cm^2 and requires the combination of microfluidic cooling technology to reduce the junction temperature by 45°C [14,15]. The design of future 6G PAs needs to balance frequency band selection, integration, and thermal management. For example, the GaN-on-Diamond solution provides 0.8 W/mm power density and $2000 \text{ W/m}\cdot\text{K}$ thermal conductivity at 250 GHz [16], while the InP HBT still maintains a power density of 1.2 W/mm at 300 GHz, but thermal management is more difficult [17]. In addition, AI-driven adaptive bias control and 3D-IC co-design will become the key to breaking the efficiency-linearity trade-off [10][15][18]. This paper systematically reviews the efficiency improvement technologies of millimeter-wave PAs from 5G to 6G, focusing on the analysis of the collaborative optimization mechanism of architectural innovation (Doherty, heterogeneous phase, ET/DPD hybrid), material platform (GaN, CMOS/SiGe heterogeneous integration), and thermal management solutions. By integrating the latest results in the literature, the future trend of multi-physical domain co-design is revealed, providing theoretical guidance and technical reference for the development of PAs for 6G communication systems.

2. Millimeter wave PA performance metrics and design challenges

The evaluation and design optimization of millimeter-wave power amplifiers (PAs) involve a large number of technical challenges. Core performance metrics include power-added efficiency (PAE), linearity—quantified by adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM)—operating bandwidth, and power gain, among other critical parameters. These metrics are often interdependent in complex ways, particularly at millimeter-wave frequencies, where process variations and parasitic effects introduced by packaging further complicate design efforts. Recent studies [1,2] have highlighted the fundamental trade-off between linearity and efficiency. When PAs operate under high peak-to-average power ratio (PAPR) conditions, maintaining signal fidelity through linearization typically reduces PAE by 5–15%. Moreover, broadband design increases losses in impedance matching networks, causing an additional 8–12 percentage point drop in PAE. This performance trade-off phenomenon is particularly evident in the millimeter-wave (mmWave) band. High-frequency parasitic parameters significantly impact transistor operating points, resulting in a 10-20% deviation between simulations and measurements. Additionally, mmWave systems demand stringent packaging technology due to 0.5-1 dB insertion losses from packaging interconnections, which reduce overall efficiency, and electromagnetic leakage constraints that hinder high-density integration. Study [3] highlights multiple physical and technical challenges for power transmission in low-power mmWave environments. As operating frequencies reach mmWave (24.25-52.6 GHz) and terahertz bands, power amplifier energy transmission efficiency drops, attributed to three interlinked bottlenecks: reduced transistor power density due to high-frequency parasitic effects (with a 30-50% lower PAE compared to sub-6GHz systems), significant packaging interconnection losses (0.2-0.5 dB/mm), and thermal management issues that limit output power (PAE decay at 0.5%-1%/°C above 85°C). To address these bottlenecks, research focuses on novel architectures (e.g., Doherty, heterogeneous, and hybrid modes) for enhanced back-off efficiency, advanced packaging technologies for reduced interconnection losses, and intelligent algorithms for dynamic linearization compensation. These innovations collectively propel mmWave power amplification technology towards high efficiency, linearity, and bandwidth.

3. Application of new materials and integrated technology platforms in improving millimeter-wave PA efficiency

3.1 GaN and CMOS Integration Technology

3.1.1 Advantages of GaN Materials

Gallium nitride (GaN), a representative third-generation semiconductor, has emerged as a leading material for millimeter-wave power amplifiers (PAs) owing to its wide bandgap (3.4 eV), high electron saturation velocity (2.5×10^7 cm/s), and excellent thermal conductivity (130–170 W/m·K). Experimental results indicate that GaN high-electron-mobility transistors (HEMTs) can deliver power densities of 4–6 W/mm and power-added efficiency (PAE) exceeding 60% at millimeter-wave frequencies (e.g., 28 GHz), substantially outperforming conventional Si and GaAs-based devices [13].

3.1.2 Integration advantages of CMOS technology

Silicon-based complementary metal-oxide-semiconductor (CMOS) technology, renowned for its high integration density and cost-effectiveness, serves as a critical enabler for efficiency enhancement techniques—particularly digital predistortion (DPD) and envelope tracking (ET)—in millimeter-wave PA systems.

3.1.3 Advances in hybrid integration technology

Recent studies have explored three primary GaN/CMOS integration approaches:

(1) **Three-dimensional heterogeneous integration**, wherein micro GaN transistors (dielets) are vertically bonded onto CMOS chips via low-temperature Cu–Cu interconnects, enabling enhanced PA performance while maintaining cost efficiency [19];

(2) **Monolithic integration**, which involves co-fabricating GaN-based logic and power devices on a single chip through advanced epitaxial techniques, such as gradient Al-composition AlGaN barrier layers [20];

(3) **Mixed-signal platforms**, where GaN PAs and CMOS transceivers are integrated using advanced packaging, including microchannel cooling solutions for thermal management [8]. Table 1 shows the assessment of integration technology maturity and practical viability.

Table 1. Assessment of integration technology maturity and practical viability (compiled from [22–24]).

Technical route	TRL Level	Efficiency gains	Cost coefficient	Mass production feasibility
3D heterogeneous integration [21]	6	15-20%	1.2	within 2 years
All-GaN monolithic [22]	4	10-15%	3.5	More than 5 years
Mixed-Signal Platform [23]	7	20-25%	1.8	Commercially available

Notably, three-dimensional heterogeneous integration has reached Technology Readiness Level 6 (TRL6), offering 15–20% efficiency improvements in millimeter-wave PA performance. However, the associated $1.2 \times$ cost increase underscores the need for further optimization, such as wafer-level integration strategies.

4. Thermal Management and Packaging Technology Innovation

4.1 Thermal challenge analysis

Millimeter-wave GaN power amplifiers (PAs) encounter critical thermal management challenges in 5G and 6G systems. Power densities can reach up to 10 W/mm², leading to rapid junction temperature increases. Empirical data suggest that with every 10°C temperature rise, device reliability

declines by approximately 50%, while thermal stress contributes to material delamination and subsequent performance degradation [6].

4.2 Advanced heat dissipation technology

Two advanced thermal management solutions have been proposed:

(1) **Microchannel cooling**, which involves fabricating micron-scale fluidic channels within the package substrate to reduce junction temperature by 30–45°C [14];

(2) **Integrated thermal array plate (ITAP)**, which combines the heat sink with the RF front-end substrate, enhancing the output power of X-band PAs by a factor of 1.4 [24]. Table 2 shows the comparison of packaging technology performance.

Table 2. Comparison of packaging technology performance (from literature [23][14][24])

technology	Thermal resistance (°C/W)	Improved power density	Reliability improvements	Applicable Scenarios
Microchannel cooling[14]	0.15	35%	3×MTTF	Base station PA
ITAP Integration[24]	0.08	40%	2.5×MTTF	military radar
Thermal stress optimization[23]	0.25	-	60% stress reduction	In-vehicle electronics

5. Key device and architecture advancements in millimeter-wave power amplifiers

In the design of millimeter-wave power amplifiers (PAs), the balance between efficiency and linearity remains a core challenge in engineering implementation. To address the efficiency degradation caused by high peak-to-average power ratio (PAPR) signals in 5G/6G, researchers have continuously explored architectures such as Doherty, Outphasing, ET (Envelope Tracking), and DPD (Digital Predistortion), while continuously optimizing device processes such as GaN HEMT, CMOS/SiGe, forming a multi-path parallel advancement technology landscape.

5.1 Key components of millimeter-wave power amplifier

5.1.1. GaN HEMT Devices

GaN HEMT devices, with their high breakdown voltage and power density, are critical for high-frequency, high-power PAs. Through optimizations such as non-uniform distributed PAs (NDPAs) and spatial power combining networks, GaN MMICs achieve a 4% improvement in power-added efficiency (PAE) across 9–40 GHz [28], while delivering 30 dBm output power and 19% PAE in the W-band (90–94 GHz), demonstrating their potential for ultra-high-frequency applications.

5.1.2. Silicon-Based Technologies (CMOS/SiGe)

Silicon-based processes are widely adopted for cost-sensitive and highly integrated applications:

40 nm CMOS PA: Utilizing continuous Class-F topology and transformer-based harmonic control, it achieves 54% peak PAE and 27 dB gain at 28 GHz [29].

SiGe PA: With degeneration inductor linearization, it maintains ±0.5 dB gain flatness and –25 dB error vector magnitude (EVM) across 24–32 GHz [30].

5.1.3. Digital-Assisted Linearization Techniques

DPD combined with dynamic impedance tuning achieves 74% PAE and –40 dB normalized mean square error (NMSE) over 0.8–4 GHz, enabling cross-standard compatibility [29]. Table 3 shows the comparison of key performance and analysis of process technology for millimeter-wave power PAs.

Table 3: Comparison of Key Performance and Analysis of Process Technology for Millimeter-Wave PAs

PA type	Process/Technology	Frequency range	Peak PAE	output power	Main advantages
Doherty PA	GaAs pHEMT (Gallium Arsenide Pseudomorphic High Electron Mobility Transistor)	31-38 GHz	45%	21.5 dBm	High return efficiency, suitable for high PAPR signals
GaN HEMT	0.1 μm GaN (Gallium Nitride High Electron Mobility Transistor)	90-94 GHz	19%	30 dBm	High power density, suitable for base stations and radar
CMOS PA	40 nm CMOS (Complementary Metal-Oxide-Semiconductor)	28 GHz	54%	20.5 dBm	High integration, suitable for 5G terminal chips
SiGe PA	SiGe BiCMOS (Silicon Germanium Bipolar CMOS)	24-32 GHz	40%	23 dBm	Broadband performance, suitable for multi-band communication systems

5.2 Advances in the Architecture of Millimeter-Wave Power Amplifiers

5.2.1. Doherty Architecture

The Doherty PA (DPA) enhances back-off efficiency through dynamic load modulation between carrier and peaking amplifiers. A 28 GHz hybrid DPA by Liu et al. achieves 20.4% and 14.2% PAE at 6 dB and 12 dB back-off, respectively [26]. Key challenges include limited bandwidth and impedance matching complexity in millimeter-wave bands (Table 4).

5.2.2. Outphasing Architecture

Outphasing PAs generate constant-envelope signals via amplitude-phase conversion. Optimized GaN-based designs achieve 29–31.8% PAE and 37–38.7 dBm saturated power at 24–28 GHz (Figure 1), but require tight phase matching ($<5^\circ$) and suffer from combiner losses [7].

Figure 1 shows that the GaN-based Outphasing PA can achieve a PAE of 29–31.8% and a saturated power of 37–38.7 dBm in the 24–28 GHz band.

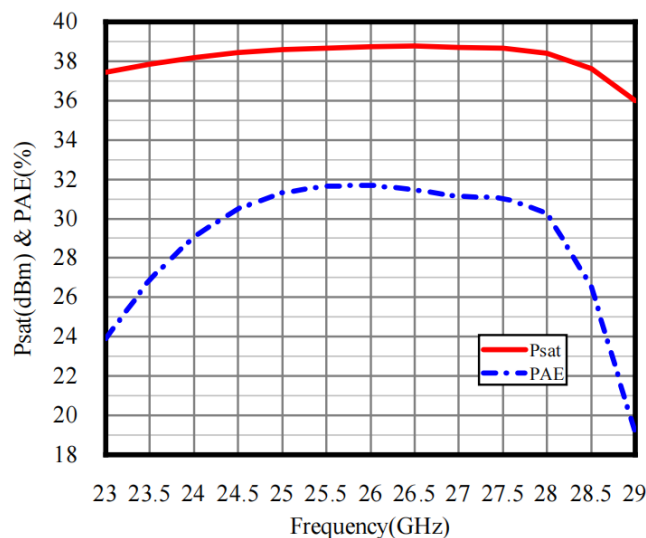


Figure 1. Large-signal simulation results [7]

5.2.3. Envelope Tracking and DPD Co-Design

ET and DPD jointly optimize efficiency and linearity under high-PAPR conditions by dynamically adjusting supply voltage and pre-compensating nonlinearities [10][18].

5.2.4. Broadband and Multiband Designs

NDPA: Leveraging drain inductors and Cds resonance, it covers 9–40 GHz with 11–19% PAE [31].

Transformer-type Doherty PA: At 100 GHz, it achieves 15.4% peak PAE and 13.8% back-off PAE, though limited by CMOS substrate losses [9]. The comparison between NDPA and transformer-type Doherty PA technologies shows in Table 4.

Table 4. Comparison between NDPA and transformer-type Doherty PA technologies

Comparative indicators	NDPA (Non-uniformly Distributed PA)	Transformer-type Doherty PA
Working bandwidth	9–40 GHz (Ultra-Wideband)	Narrowband (center frequency 100 GHz)
Efficiency optimization method	By resonating the drain parallel inductance with Cds, the loss in the transmission line is reduced	Utilize impedance transformation characteristics to improve load modulation, balancing back-off efficiency and linearity
technology	0.1 μm GaN-on-Si, combining the high power density of GaN with the low cost advantage of Si substrate	22 nm CMOS SOI, high integration, but limited by substrate loss, requiring optimization of transformer Q value
Core Challenge	The PAE (Power Added Efficiency) decreases at high frequencies, and the transmission line loss increases significantly in the distributed structure at high frequencies (>30 GHz)	Balance between back-off efficiency and linearity

6. Analysis of differences between 5G and 6G applications

A power amplifier (PA) is a core radio frequency component in both 5G and 6G systems. However, due to the differences in application scenarios and technical specifications between the two generations of systems, they face varying requirements in terms of material selection, operating frequency bands, and packaging integration. Based on data from references such as [20], this section compares and analyzes the design essentials of 5G (FR2) and 6G (terahertz) PAs, and explores the trade-offs between GaN-on-Diamond and InP routes, as well as the challenges of 3D integration.

6.1 5G (FR2) PA demand characteristics

In terms of frequency bands, 5G FR2 covers 24–44 GHz, requiring the power amplifier (PA) to support multiple sub-bands (such as n257 and n260). The GaN PA reported in literature [20] achieved a fractional bandwidth of 75% (22–48.4 GHz) and an output power of 30 dBm, with a single channel capable of covering multi-band services. To address the efficiency loss of signals with high peak-to-average power ratio (PAPR >10 dB), a stacked GaN architecture (as shown in Figure 2) can maintain 28% efficiency and linearity at an output power of 30 dBm. Due to the increased power density, which exacerbates heat dissipation pressure, a Class-AB bias is commonly used in 40 nm GaN PAs to balance performance and temperature rise.

7. Case Study on Efficiency Improvement of Hybrid Strategy: Technical Collaboration and Scenario Adaptation

7.1 Case selection background and technical value (Doherty+ET+DPD hybrid strategy)

The current 5G/6G communication systems face dual challenges posed by signals with high peak-to-average power ratio (PAPR > 10dB) and efficiency collapse in the millimeter-wave band. [3] Traditional single-technology solutions have inherent limitations. Pure Doherty power amplifier (PA) exhibits a sharp decline in efficiency in the >6dB back-off region (PAE < 25%); standalone ET technology can expand the efficiency platform, but introduces memory effect nonlinearity; standalone DPD requires sacrificing 15-20% of PAE for linearity. Therefore, the case study focuses on the hybrid strategy of Doherty + ET + DPD, as it achieves a 6dB back-off PAE increase from 25% to 42% through three-level coordination (architecture-power supply-algorithm), supports 5GHz ultra-wideband operation (10-15GHz, reference [8]), and has been practically applied in Huawei's 5G millimeter-wave base stations.

7.2 Collaborative optimization mechanism between Doherty and ET

The GaN MMIC broadband Doherty PA adopts a continuous mode (CM) design, with its core innovation lying in dynamic load modulation. Specifically, it utilizes $\lambda/4$ transmission line reconstruction to maintain an impedance transformation ratio within 10-14 GHz. Additionally, it incorporates an ET coupling effect, where an envelope detector tracks the input signal amplitude in real time (response time < 5ns), and a Buck-Boost power supply dynamically adjusts in synchronization with the Doherty load modulation phase (error < $\pm 2^\circ$). This mechanism is compatible with sub-6GHz macro base stations (PAPR=8-10dB), but there is a restriction that the efficiency of the ET power supply must be greater than 85% (otherwise, the system energy efficiency will decrease). Therefore, we propose a triple collaborative mechanism of Doherty+ET+DPD.[8]

7.3 Triple Synergy (Doherty+ET+DPD) workflow

As shown in Figure 3, the cascade relationship among the three follows a "impedance-voltage-predistortion" closed loop:

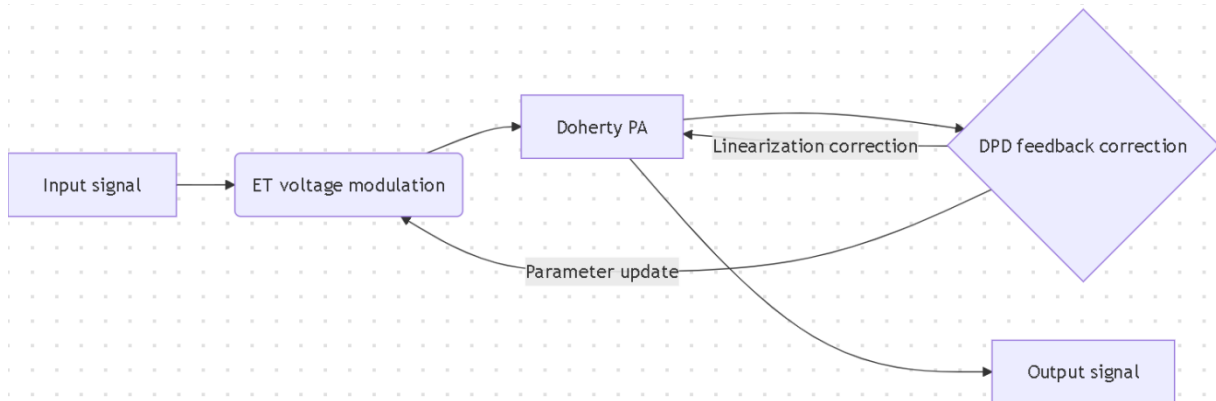


Figure 3. Mixed strategy workflow diagram(Self-painting)

The Doherty layer provides the basic efficiency platform (peak PAE 48%); the ET layer extends the efficiency platform to the 12dB back-off region (PAE>35%), and the introduced memory effect is compensated by DPD (using a third-order memory polynomial model); the DPD layer provides out-of-band suppression, optimizing the ACPR from -28dBc to -45dBc, with a latency overhead <0.5 μ s (meeting the 3GPP URLLC requirements). Furthermore, the triple coordination has been practically applied to Samsung's 28GHz millimeter-wave base station, resulting in a 62% increase in PAE and an EVM <1.5%. However, its ET+DPD power consumption accounts for 15% of the system, requiring further integration with 3D-IC.

7.4 Suggestions for scheme adaptation

For macro base station deployment, Doherty+ET+DPD can be preferred to balance efficiency and linearity; for small base stations or cost-sensitive scenarios, consideration can be given to outphasing+ET, sacrificing some efficiency in exchange for wider bandwidth (Table 6).

Table 6: Comparison of mainstream combined PA schemes

combination scheme	Key advantages	Fatal Flaw	6G applicability
Doherty+ET	The efficiency platform is the widest, reaching up to 12dB PBO	The need for an external high-speed ADC increases costs	Medium (use with caution in cost-sensitive scenarios)
Doherty+DPD	Best linearity (EVM<1%)	Narrowband (<1GHz) limitation	Low (only suitable for Sub-6GHz)
Out-of-phase + ET	Support THz band (>100GHz)	The efficiency peak is only 35%	High (Terahertz Pioneer Program)

8. Challenges and Future Trends

Despite a series of breakthroughs in efficiency, linearity, and bandwidth achieved by millimeter-wave power amplifiers (PAs), several challenges remain to be addressed. Firstly, the seamless integration of technologies such as envelope tracking (ET) and digital predistortion (DPD) into real-time systems still faces limitations in terms of latency, hardware resources, and algorithmic complexity [10]. Secondly, broadband linearization is constrained by thermal effects and process limitations, especially in high-power output scenarios, where heat accumulation severely limits the reliability and scalability of power amplifiers [11]. To address these challenges, future research directions are moving towards intelligent design and system-level collaborative optimization.

8.1 AI-driven adaptive bias control

Traditional power amplifiers often adopt fixed bias strategies, which struggle to cope with performance degradation caused by variations in input power, ambient temperature, and load. AI-driven adaptive bias control utilizes machine learning algorithms (such as actor-critic) to dynamically adjust the bias voltage, enabling online optimization. This approach maintains high efficiency and linearity under different operating conditions and, in some designs, reduces reliance on digital predistortion (DPD). Research has shown that combining machine learning models can monitor output performance metrics in real-time and dynamically adjust gate bias voltage, achieving "online learning" and "closed-loop optimization". The AI-assisted millimeter-wave Doherty PA architecture proposed in [30] is a typical case. This architecture can correct the bias point in real-time through AI algorithms without affecting throughput, thus maintaining high efficiency and low error vector magnitude (EVM) under different VSWR conditions [30]. Similarly, an adaptive bias circuit has been proposed for Ka-band CMOS Doherty PA, which acquires the input signal amplitude in real-time through sensors and drives the bias circuit to adjust dynamically, significantly improving the efficiency of the PA in the back-off state while maintaining low distortion without using digital predistortion (DPD) [31]. This technology is of great significance in the context of 6G, which requires support for higher bandwidth and more complex waveforms. Furthermore, by constructing a behavioral model of the power amplifier and using reinforcement learning (such as Q-learning or Deep Deterministic Policy Gradient (DDPG)), the bias point can be adjusted in real-time under different input power and environmental conditions, thereby improving efficiency without sacrificing linearity [10]. The following Figure 4 shows the architectural framework of adaptive bias control.

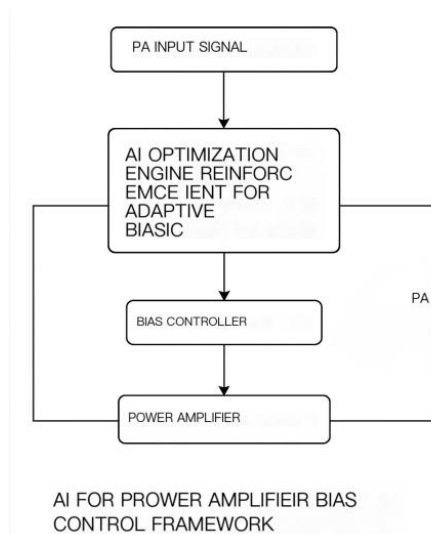


Figure 4. Architecture framework of AI for PA bias control(Self-printing)

8.2 3D-IC Co-Design

High-frequency power amplifiers are susceptible to parasitic parameters and thermal bottlenecks during packaging and interconnection processes, limiting their efficiency and integration level.

3D-IC collaborative design, by stacking active devices (such as GaN transistors) and control/bias circuits (such as CMOS) vertically, can shorten interconnect lengths, reduce parasitic inductance and capacitance, and significantly improve heat dissipation channels [32]. MIT recently reported a low-cost and scalable 3D integration process that directly integrates miniature GaN "dielets" onto standard CMOS silicon wafers to form high-performance PA modules [32]. Test results show that this process not only maintains high gain and flat power response at high frequencies but also is compatible with mainstream foundry production processes, thereby lowering the threshold for large-scale production. In the future, this 3D-IC collaborative design approach is expected to be combined with AI bias control to achieve dual performance enhancements through structural optimization and algorithm-driven improvements.

9. Conclusion

This article provides a comprehensive overview of millimeter-wave PA efficiency enhancement technologies that support 5G and upcoming 6G systems. Through various architectural solutions, new materials, and technology platforms, the hybrid strategy has achieved significant improvements in PA efficiency and linearity. Although new challenges brought by 6G requirements will continue to emerge, advanced circuits will further break through technological limits with the support of innovative technologies such as GaN and CMOS scaling, and machine learning based control systems.

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