The Optimization of Current Mirror Topologies in Low-Dropout Regulators

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Abstract. This review examines practical methods for reducing noise in current mirrors, which are essential building blocks in precision analog circuits like low-dropout regulators (LDOs). Three main noise control approaches are discussed: improvements to cascode current mirror structures, optimization of transistor parameters, and specialized biasing techniques. Cascode-based designs—such as stacked nonlinear mirrors, regulated folded cascode (RFC) amplifiers, and nonlinear nested current mirrors (NL-NCM) help lower mismatch and low-frequency noise while strengthening power supply rejection. Transistor-level methods incorporate dynamic threshold MOSFETs (DTMOS) and regenerative current mirrors to improve linearity and support low-power operation. Biasing strategies, including back-gate biasing in FDSOI processes and PTAT resistor feedback, further suppress noise by adjusting threshold voltages and limiting noise propagation. Each technique involves trade-offs between noise, power, area, and linearity. Looking ahead, combining architectural, process, and biasing improvements is a promising path for developing efficient, low-noise current mirrors suitable for sensor interfaces and other noise-sensitive systems.

Keywords: Current mirror, low-noise design, cascode amplifier, flicker noise, transistor, mismatch mitigation.

1. Introduction

Power supply noise can significantly degrade the stability of high-precision sensors and the integrity of pixel signals. Low-Dropout Regulators (LDOs) are often employed as post-regulators following switching DC-DC converters to further suppress voltage ripple and provide clean power to noise-sensitive circuits. Thus, low-noise LDOs play a critical role in sensor power supply architectures [1]. Simultaneously, in both CMOS image sensors and high-energy physics experiment readout systems, low-noise LDOs are required to suppress power supply interference, thereby enhancing the signal-to-noise ratio (SNR) of image sensor or detector readouts [2]. The noise in an LDO is primarily composed of error amplifier noise, power transistor noise, feedback network noise, and reference voltage noise. Circuit-generated noise is typically categorized into two types: the first is thermal noise, caused by feedback resistors and current mirror devices; the second is flicker noise, which is determined by transistor fabrication processes and biasing conditions. This paper focuses on optimizing the noise performance of current mirrors within the error amplifier. Specifically, it reviews noise reduction strategies through three approaches: optimizing cascode structures, optimizing transistors, and employing specialized biasing schemes.

2. Noise Characteristics of Current Mirrors

The noise behavior of current mirrors can generally be analyzed based on their fundamental noise model using the noise current spectral density formula:

$$\mathrm{in}^2=4kT\gamma g_m+\frac{Kgm^2}{C_{OX}WLf}. \qquad (1)$$

Where k is Boltzmann’s constant, T is the absolute temperature, r is the thermal noise coefficient (approximately 2/3), K is the flicker noise coefficient, gm is the transconductance, and W and L represent the device dimensions. Modifications to these parameters critically influence the noise performance of the current mirror [3].

3. Current Mirror Noise Suppression Techniques

3.1 Optimization of Cascode Current Mirrors

Based on literature research, strategies for optimizing current mirror noise can be categorized into four types: noise optimization in cascode current mirrors, transistor parameter optimization, implementation of specialized biasing schemes, utilization of nonlinear current mirrors. Regarding the optimization of cascode current mirrors.

To improve the traditional Simple Balanced Cascode Structure (SBCS), one study proposed an enhanced architecture employing a current reference circuit with stacked nonlinear current mirrors. In conventional structures, the current mirror typically consists of one linear and one nonlinear current mirror. The improved scheme replaces this with two vertically stacked nonlinear current mirrors. By introducing an additional damping factor into the current loop, interference suppression in reference current is achieved. The ratio of gm3 to gm4 critically influences the value of this damping factor, the formula is as follows:

$$d_{f,ges}=d_{f,1}\cdot d_{f,2}=\frac{g_{m,2}}{g_{m,1}}\frac{g_{m,4}}{g_{m,3}}=\frac{V_{ov,1}}{V_{ov,2}}\frac{V_{ov,3}}{V_{ov,4}}\text{ [4]} \tag{2}$$

Based on this method, noise, power supply variation sensitivity, and mismatch can be reduced by approximately 6 db. The second approach introduces an RFC (Regulated Folded Cascode) amplifier. By splitting the input transistors into PM1a, PM1b, PM2a, and PM2b, and employing a cross-coupled current mirror design, the transconductance is enhanced and current mirror matching is improved [5]. The cascode stage NM1a/NM1b plays a critical role in this circuit: by adjusting the drain potential connected to other current mirror devices, it suppresses mismatch-induced noise. The third strategy proposes a novel design—the Nonlinear Nested Current Mirror (NL-NCM). As shown in the structure presented in Fig. 1, the output current is enhanced through optimization of the current mirror architecture without requiring additional circuit components. This design reduces the circuit area while simultaneously providing stronger drive capability under highly constrained power and area conditions. Consequently, this method is particularly suitable for applications with high requirements for transient response and operation under large capacitive loads, especially where power budgets and area are limited [6].

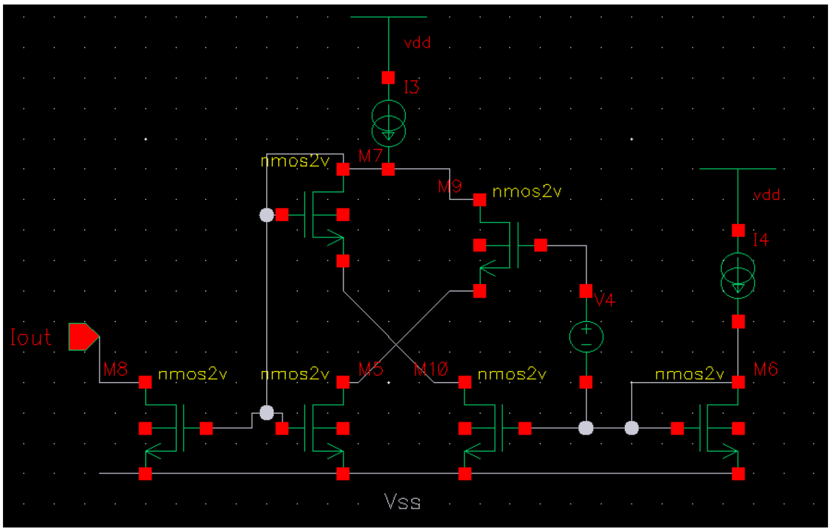

Figure 1. NL-NCM

A comparative analysis of these three schemes reveals the following conclusions: For applications prioritizing maximum noise reduction (particularly low-frequency 1/f noise and mismatch), the RFC amplifier in Scheme 2 proves to be the most effective solution. When the goal is to balance performance under tight power and area constraints, the NL-NCM in Scheme 3 is more suitable, excelling in scenarios with large capacitive loads and limited area. If quantitative performance improvement and power supply rejection (PSR) are critical, Scheme 1 (stacked nonlinear current mirror) offers a reliable and guaranteed choice.

3.2 Optimization of Transistor Parameters for Noise Reduction

The authors propose utilizing a body-driven floating-gate cascode regulated current mirror to construct a differential amplifier structure, thereby optimizing key metrics such as delay, power consumption, and power-delay product (PDP). The term "body-driven" MOSFET refers to adjusting the threshold voltage by modulating the substrate potential, enabling the transistor to operate at lower supply voltages while enhancing the performance of the current mirror. In subsequent improvements, Dynamic Threshold MOSFETs (DTMOS) were adopted to replace conventional MOS devices, as illustrated in Fig. 2. DTMOS Compared to standard CMOS, DTMOS transistors typically exhibit superior linearity characteristics, leading to significant noise reduction. Their characteristics render them suitable for circuit applications that impose stringent requirements on linearity and noise performance [7].

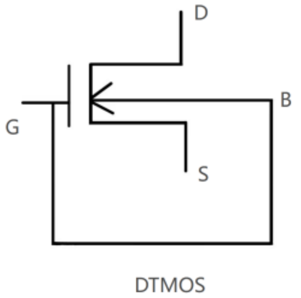

Figure 2. DTMOS

The second study presents a regenerative current mirror architecture combining NMOS and PMOS transistors with a feedback mechanism to provide positive feedback and enhance gain at low bias currents. To control the gain and avoid instability, an NMOS transistor with an externally adjustable gate voltage is added, constraining the open-loop gain to just below unity. This measure stabilizes the circuit and markedly improves the noise characteristics of the current mirror under low-power conditions [8].

In summary, the DTMOS-based method improves noise performance through threshold voltage control and enhanced transistor linearity, making it suitable for analog circuits that demand high fidelity and strict linearity. In contrast, the regenerative current mirror employs a positive feedback topology to achieve high gain under low bias currents, substantially reducing power consumption and facilitating the processing of weak signals in front-end readout circuits. These two methods provide complementary benefits: the former addresses noise reduction and linearity optimization, while the latter prioritizes energy efficiency.

3.3 Implementation of Specialized Biasing Schemes for Noise Suppression

The FDSOI platform introduces a flip-well structure that enables forward back-gate biasing, enhancing device controllability and providing greater flexibility for low-noise analog circuit design. Experimental results show that back-gate bias modulates the threshold voltage to influence drain current without degrading noise performance. At low gate-source voltages, it reduces the vertical electric field in the channel, suppressing gate leakage and supporting ultra-low-voltage operation. Overall, back-gate biasing offers improved control of threshold and noise characteristics, enhances adaptability in low-power and low-noise circuits [9], Back-gate biasing not only enhances the transfer characteristics of current mirrors but also serves as an effective circuit-level noise reduction technique.

Another study integrated a PTAT (Proportional to Absolute Temperature) resistor into the feedback path of the current mirror (Fig. 3), stabilizing the bias point while suppressing noise propagation. Compared with conventional polysilicon resistors, this approach offers temperature adaptability and higher resistance, effectively reducing low-frequency noise and mismatch. The introduction of temperature-dependent parameters significantly enhances the noise performance of current mirrors, surpassing traditional methods in both resistor selection and feedback design [10].

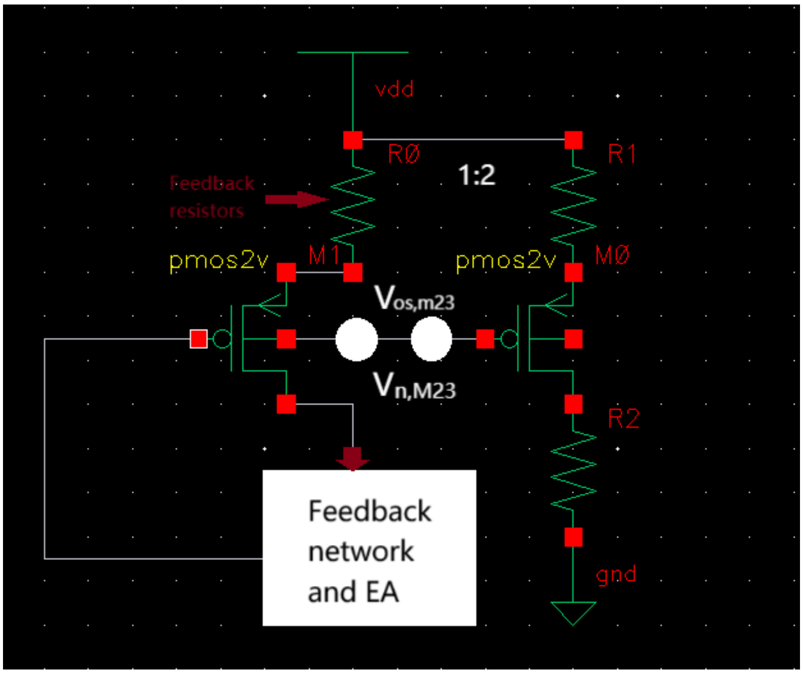

Figure 3. Resistor feedback

Comparative analysis indicates that back-gate biasing and PTAT resistor feedback represent distinct strategies at different design levels. Back-gate biasing leverages the structural advantages of FDSOI technology to regulate threshold voltage and suppress gate leakage, providing effective noise control in low-power, low-voltage operation. In contrast, PTAT resistor feedback acts at the circuit level, employing temperature-adaptive high-resistance elements to reduce low-frequency noise and enhance stability. Overall, the PTAT resistor feedback method offers targeted advantages in reducing low-frequency noise, while back-gate biasing demonstrates unique strengths in ultra-low-power applications. These two strategies exhibit complementary characteristics, and their combined use can achieve an optimal balance between precision and power consumption.

4. Conclusion

A review of recent research indicates that the current mirror plays a central role in low-noise LDOs, with its noise characteristics critically influencing the performance of the error amplifier and the overall output quality of the circuit. Focusing on noise reduction, existing efforts primarily concentrate on three categories of methods: structural improvements via cascode configurations, transistor-level parameter optimization, and circuit-level specialized biasing strategies. Each approach has distinct emphases: the former is particularly effective in addressing mismatch and low-frequency noise issues; transistor optimization offers advantages in maintaining linearity and reducing power consumption; while biasing schemes demonstrate flexibility and adaptability, especially excelling in low-power applications.

Overall, these methods are not mutually exclusive but rather complementary. In high-precision sensors and front-end readout systems where ultralow noise is paramount, structural and device-level optimizations are more advantageous. In contrast, under power- and area-constrained conditions, biasing and feedback strategies prove more effective. Future developments are likely to focus on collaborative multi-strategy design—integrating topological optimization, process enhancements, and advanced biasing control—to simultaneously achieve low power consumption, low noise, and high stability. Such integrated approaches will provide more reliable power support for high-precision analog circuits and sensor systems.

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