Towards High-Performance LDOs: Techniques for Achieving Ultralow Output Noise and High PSR

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Abstract. With the continuous scaling-down of semiconductor feature sizes and increasing integration of System-on-Chip (SOC), the performance requirements for internal power management modules have become increasingly stringent, particularly posing severe challenges in terms of low noise and high power supply rejection ratio (PSR). This paper systematically analyzes the basic structure, working principles, and noise sources of low-dropout regulators (LDOs), identifying the inherent limitations of traditional architectures in terms of reference source noise, error amplifier noise, and thermal noise from feedback networks, as well as the issue of sharp PSR degradation at medium-to-high frequencies. To break through these bottlenecks, this study summarizes and proposes several key techniques: for noise suppression, advanced methods such as chopper stabilization, capacitance amplification, pre-regulation, and BJT-based references are adopted to effectively suppress noise sources; for PSR enhancement, structures including feedforward ripple cancellation, cascode isolation, DC-DC auxiliary regulation, and voltage subtraction are introduced, significantly improving full-bandwidth power noise immunity. Through the synergistic optimization of these techniques, this research provides effective design ideas and technical pathways for achieving high-performance LDOs, which are suitable for a wide range of noise-sensitive applications such as RF communication, medical electronics, automotive electronics, and high-precision analog systems.

Keywords: SOC, LDO, Low noise, High PSR

1. Introduction

The semiconductor industry has progressed decisively into the deep-submicron and nanometer regime. As transistor feature sizes continue to shrink, System-on-Chip (SOC) designs now integrate increasingly complex functional modules—including digital processing cores, analog interfaces, radio frequency (RF) transceivers, memory arrays, and sensor front-ends [1]. While this integration enhances functionality and energy efficiency, it also introduces critical power integrity challenges. Different circuit blocks impose divergent demands on the power supply: digital circuits produce large transient currents during switching events, while noise-sensitive analog and RF modules—such as phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and high-speed analog-to-digital converters (ADCs)—require highly stable and clean supply voltages. It is in this context that the low-dropout regulators (LDOs), valued for its minimal external component count, ease of integration, and low-noise characteristics, has become a vital component in SOC power management systems [2].

Nevertheless, conventional LDO architectures face inherent limitations. Their output noise—originating from the bandgap reference's 1/f noise, the error amplifier's input-referred noise, and thermal noise from feedback resistors—often exceeds the stringent requirements of precision analog and RF circuits. Moreover, the power supply rejection ratio (PSRR) of these architectures degrades significantly beyond the unity-gain frequency of the regulation loop, leaving them ineffective against high-frequency switching noise from modern power converters [1]. These shortcomings restrict their use in advanced applications such as 5G/6G communication, autonomous vehicles, medical wearables, and IoT devices [3].

Evolving technological and societal demands are further elevating performance expectations for power management ICs. The global emphasis on energy efficiency requires LDOs to maintain low noise and high PSRR even at ultralow quiescent currents to extend battery life. At the same time, emerging applications in artificial intelligence and quantum sensing impose extreme demands on power supply quality, where even minor perturbations can compromise system performance [1]. As a result, low noise and high power supply rejection have transitioned from desirable attributes to essential capabilities in LDO design [4].

In response, research and development efforts have introduced innovative circuit techniques—including chopper stabilization, capacitance multiplication, feedforward ripple cancellation, and cascode-based topologies—that significantly improve noise and ripple rejection across wide frequency ranges. These advances allow modern LDOs to deliver highly stable and clean power to noise-sensitive circuits, reinforcing their role as enablers of robust and reliable electronic systems.

This paper examines the design challenges and evolving solutions in high-performance LDO regulators. It begins with an analysis of conventional LDO limitations, continues with a detailed discussion of advanced techniques for noise reduction and PSRR enhancement, and concludes with an outlook on future design trends for emerging process technologies and application scenarios.

2. Fundamentals of LDO

2.1. Architecture of LDO

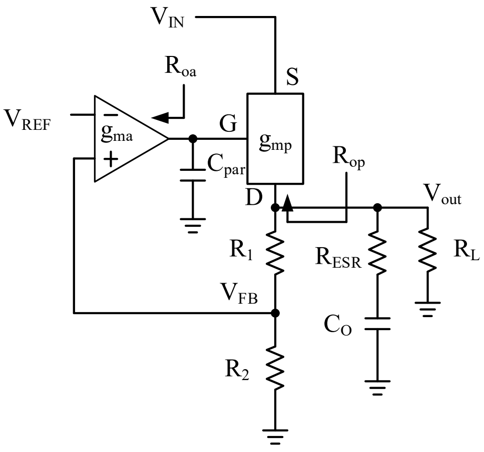

Figure 1. Architecture of LDO

2.1.1 Core Functional Modules

Denoted as g_{ma} in the Fig 1. The non-inverting input (+) is connected to the reference voltage V_{REF}, the inverting input (-) receives the feedback voltage V_{FB}, and the output drives the gate (G) of the pass element.

Function: Compares V_{REF} and V_{FB}, amplifies the difference with high gain, and drives the pass element. It serves as the "decision-making center" for closed-loop regulation.

Pass Element (Power Transistor) – The "Current Output Stage" for Voltage Regulation

Location & Connection: Usually a PMOS transistor (denoted as g_{mp} in the Fig 1). The source (S) is connected to the input voltage $V_{\mathrm{I}N}$, the drain (D) is connected to the output V_{OUT}, and the gate (G) is driven by the error amplifier output. Adjusts its conduction state based on the gate voltage. It regulates the drain-source current I_{DS} linearly to compensate for output variations (e.g., increasing conduction when load current rises to maintain V_{OUT} stability). Consists of resistors (R1 and R2 in the Fig1) connected in series between V_{OUT} and ground. The intermediate node provides the feedback voltage V_{FB} to the inverting input of the error amplifier.

Function: Feeds back output voltage information to the error amplifier to form a negative feedback loop. The output voltage is set by: $V_{\mathrm{OUT}} = V_{\mathrm{REF}} \cdot \frac{R_1+R_2}{R_2}$. Adjusting the R_1/R_2 ratio allows output voltage tuning [5].

2.1.2 Auxiliary Components

Compensation Capacitor ($\mathrm{C_p}$ in the Fig1) connected between the output of the error amplifier (or the gate of the pass element) and ground. Suppresses loop oscillation. The LDO loop contains multiple poles (e.g., at the EA output, pass element gate, and output node), which may reduce phase margin. C_p implements Miller compensation or pole splitting, pushing the dominant pole to a lower frequency and the secondary pole to a higher frequency, ensuring sufficient phase margin under all load conditions

Load Capacitor (C_0 in the Fig1) and Equivalent Series Resistor (R_{ESR}) parallelled with R_{ESR} is connected between V_{OUT} and ground, with load resistor R_L also in parallel. Filters output ripple and supplies charge during load transients (e.g., providing extra current when load current suddenly increases). R_{ESR}: Works with C_0 to form R_{ESR} compensation. The left-half-plane zero introduced by R_{ESR} cancels out the secondary pole in the loop, enhancing mid-to-high frequency stability (as referenced in literature: "R_{ESR} compensation is suitable for traditional external-capacitor LDOs") [4].

Bias Resistor (R_{oa} in the Fig1) connected between V_{IN} and the output of the error amplifier (or the gate of the pass element). Provides a quiescent bias current for the error amplifier or pass element, ensuring reliable startup even under low input voltage or light-load conditions (consistent with literature on "biasing design adapted to supply voltage and load characteristics").

2.2. Basic Working Principle of LDO

2.2.1 Power-On Startup Stage: Reference Establishment and Loop Initialization

Reference Voltage Source Startup: After the input voltage V_{IN} is applied, the bandgap reference circuit initiates operation first. It generates a stable, zero-temperature-coefficient reference voltage V_{REF} (e.g., a typical 1.25V silicon bandgap voltage) by summing positive temperature coefficient (PTAT) and negative temperature coefficient (CTAT) signals. A soft-start circuit controls the ramp-up of the reference voltage to prevent overshoot.

Error Amplifier and Feedback Network Initialization: Once V_{REF} stabilizes, the Error Amplifier (EA) becomes active. Its non-inverting input is connected to V_{REF}, and its inverting input receives the feedback voltage V_{FB} (initially 0V as V_{OUT} is not yet established). The EA output drives the gate of the pass element (PMOS), initially pulling it low.

Pass Element Turn-On and Output Voltage Establishment: The pass element (typically a PMOS transistor) gradually turns on, allowing current to flow from V_{IN} to the output, causing the output voltage V_{OUT} to rise. When V_{OUT} reaches approximately 90-95% of its target value (e.g., the Power Good threshold) [4], the soft-start phase concludes, and the feedback loop enters closed-loop regulation. V_{OUT} stabilizes at the set value determined by: $V_{OUT} = V_{REF} \cdot \frac{R_1+R_2}{R_2}$ [5].

2.2.2 Dynamic Response Stage: Handling Transient Changes

The LDO must quickly respond to load steps or input ripple:

Load Step Response: A sudden increase in load current (e.g., from 10mA to 100mA) causes a momentary drop in V_{OUT}. The EA, often aided by slew-rate enhancement circuitry, rapidly pulls the pass element gate voltage lower. I_{DS} increases sharply to quickly supply the additional current demand. V_{OUT} recovers to its set value (transient response time can be optimized to below 50μs)

The LDO utilizes a negative feedback control mechanism following the sequence of "reference establishment to loop startup to steady-state closed-loop operation to dynamic correction" to achieve efficient and stable linear voltage regulation. Its performance critically depends on the error amplifier's gain, the response speed of the pass element, and the design of the compensation network.

3. Summary of Main LDO Noise Sources

3.1 Intrinsic Noise — Noise generated internally by the LDO circuit itself

3.1.1 Bandgap Reference Noise

Thermal Noise: Generated by resistors and other elements within the reference circuit. Can be effectively suppressed by an external RC filter circuit (e.g., a 1 MΩ resistor and 100 pF capacitor combination to limit the bandwidth to 1.6 Hz) [6].

1/f Noise (Flicker Noise): Related to device material and surface effects. The 1/f noise of Bipolar Junction Transistors (BJTs) is typically lower than that of MOSFETs. Can be reduced by increasing device size or employing BJT-based designs [7].

3.1.2 Error Amplifier Noise

Input Stage Noise: The main noise source of the error amplifier. The noise performance (especially 1/f noise) of a BJT input pair is generally superior to that of a MOSFET input pair.

Noise Gain: The noise from the error amplifier is amplified to the output by subsequent stages, and this gain is influenced by the feedback network [6]. In a unity-gain configuration, the noise contribution from the feedback resistors can be eliminated.

3.1.3 Pass Element Noise

BJT Pass Element: Exhibits lower 1/f noise, but base current introduces shot noise.

MOS Pass Element: The primary contribution comes from the thermal noise of the on-resistance (RDS (on)), which can become a dominant output noise source under light load conditions.

3.1.4 Feedback Network Noise

Thermal Noise: The feedback divider resistors (R1, R2) generate thermal noise, which is directly superimposed on the output. This noise source can be eliminated in a unity-gain (buffer) configuration.

3.2 Extrinsic Noise — Noise coupled or conducted from external sources

3.2.1 Power Supply Ripple (Input Ripple / Supply Noise)

Low-Frequency Ripple: Primarily suppressed by the LDO's high loop gain and high Power Supply Rejection Ratio (PSRR). However, PSRR performance degrades under heavy load or low dropout conditions.

High-Frequency Ripple: At high frequencies (e.g., >1 MHz), loop gain decreases, and PSRR rolls off [6]. Suppression at these frequencies relies on the Equivalent Series Resistance (ESR) of the output capacitor and external LC filter networks.

3.2.2 Load-Induced Noise

ESR Noise: Variations in load current ($\Delta I/\Delta t$) flowing through the Equivalent Series Resistance (ESR) of the output capacitor generate instantaneous voltage noise ($\Delta V = ESR * \Delta I$). Using low-ESR capacitors (e.g., ceramic capacitors) can improve this [6].

Transient Response Noise (Droop): During sharp load current transients, the discharge of the output capacitor causes a temporary drop in output voltage (Droop). Improving the transient response (e.g., using a larger output capacitor or a faster loop) can minimize this noise.

3.2.3 Parasitic Coupling Noise

PCB Layout Parasitic: Trace inductance and resistance can cause voltage spikes during rapid current changes.

Electromagnetic Interference (EMI): External electromagnetic fields couple into sensitive nodes via radiation or capacitive coupling. Mitigation requires good PCB layout practices, shielding, and filtering.

Summary, the total noise of an LDO results from the combined effect of internal intrinsic noise and external interfering noise. Optimizing LDO noise performance requires a two-pronged approach:

firstly, suppressing intrinsic noise through circuit design techniques (e.g., using low-noise references, BJT inputs, filtering); and secondly, blocking external noise through adequate power supply filtering, careful PCB layout, and appropriate external component selection (e.g., low-ESR capacitors) [6].

4. Core Technologies for Reducing LDO Noise and Improving Power Supply Rejection Ratio (PSRR)

4.1 Key Technologies for Noise Reduction

4.1.1 Chopper Stabilization and Noise-Shaping Technology

Principle: As shown in Fig.2, it utilizes chopper modulation to shift low - frequency 1/f noise (primarily from the error amplifier and reference) to higher frequencies, where the noise is then suppressed by filtering. Combined with digital ΣΔ noise shaping, this approach broadens the noise spectrum to avoid noise concentration at the chopping frequency [8].

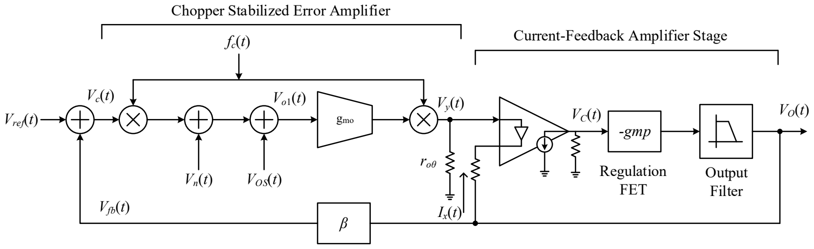

Figure 2. Diagram of chopper-stabilized LDO regulator with a fixed frequency chopping clock

4.1.2 Capacitance Amplification and Efficient Filtering Technology

Principle: As illustrated in Fig.3, this technique employs a "small capacitor + negative transconductance amplifier (-Gm)" to form a capacitance amplification circuit, effectively mimicking a large capacitor filtering effect. This design reduces the transmission of reference noise while significantly saving chip area [9].

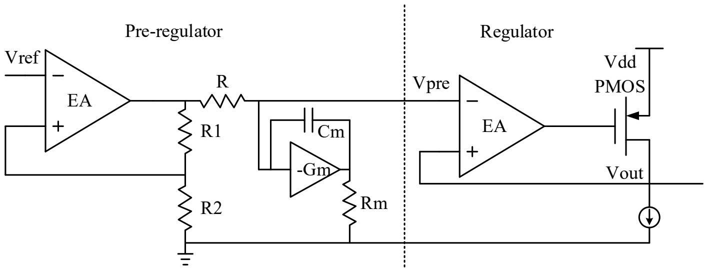

Figure 3. A compact low-noise LDO circuit with large-capacitance filtering capability

4.1.3 Pre-Regulation and Noise Isolation Technology

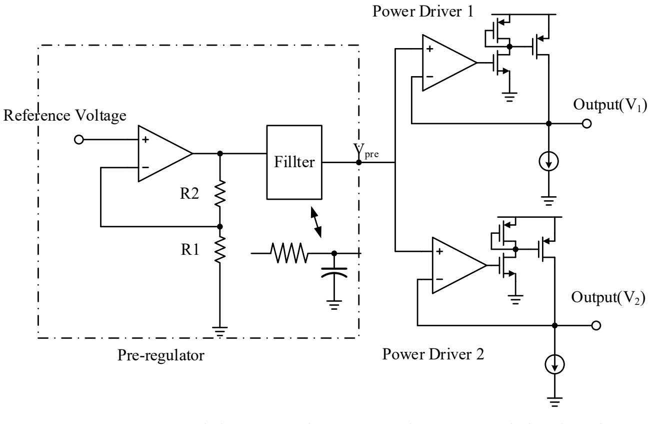

Figure 4. Proposed low noise regulators with dual output

Principle: As shown in Fig.4, it adopts a two-stage structure of a "pre-regulator + power drive stage". The pre-regulator uses RC low-pass filtering to suppress reference noise, while the power drive stage acts as a voltage follower to reduce the amplification of thermal noise from the feedback resistor network [10].

4.1.4 Device Selection and Local Noise Reduction Optimization

Principle: The circuit in Fig.5, a BJT-based bandgap reference circuit with reduced output noise, makes use of bipolar junction transistors (BJTs) to construct the bandgap reference (cutting down 1/f noise) and adds an RC noise reduction module at the error amplifier’s input to divert high-frequency noise [11].

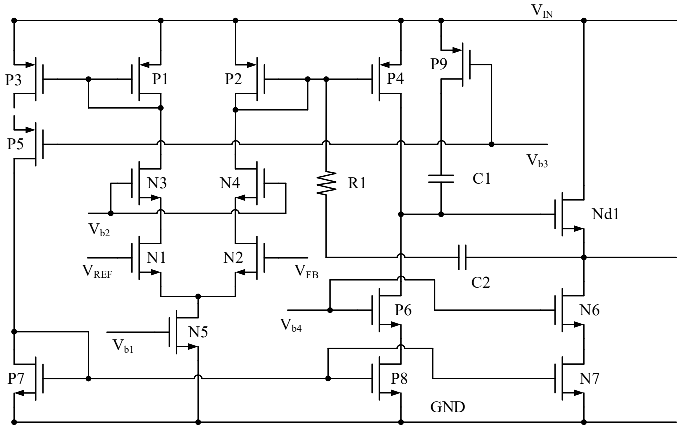

Figure 5. A BJT-based bandgap reference circuit with reduced output noise

4.2 Core Technologies for Improving PSRR

4.2.1 Feedforward Path and Ripple Cancellation Technology

As shown in Fig. 6, a feedforward path (e.g., a PMOS transistor pair Mn1/Mn2 in Fig.6) is introduced between the drain and gate of the pass transistor (PMOS) [12]. This path drives a current mirror to generate anti-phase ripple, so as to cancel the impact of power supply noise on the output. Its signal flow diagram is shown in Fig.7 [12].

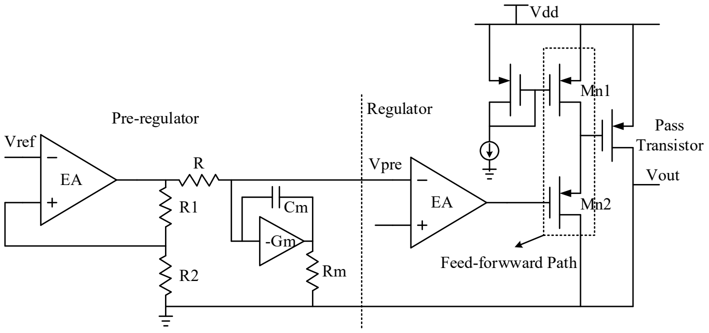

Figure 6. Proposed ultra-low noise and high PSRR LDO

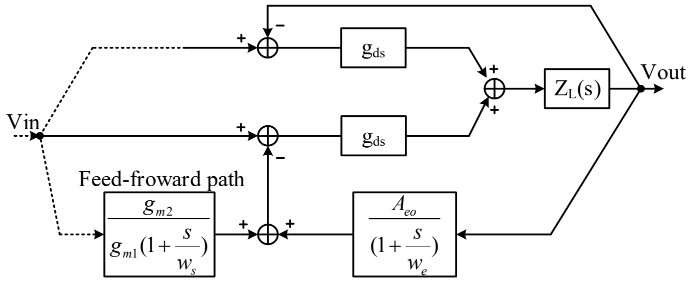

Figure 7. Signal flow diagram of current mirror driving and anti-phase ripple generation with noise cancellation mechanism for PSR

4.2.2 Cascode and High-Impedance Isolation Technology

Principle: As depicted in Fig. 8, the error amplifier adopts a folded - cascode structure to raise output impedance and strengthen power noise isolation [13]. Meanwhile, coupled with cascode Miller compensation, it secures loop stability over a broad frequency range and stops PSRR from degrading at high frequencies [13, 14].

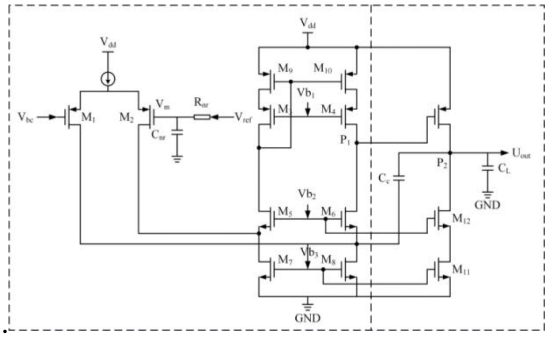

Figure 8. The schematic diagram of the error amplifier

4.2.3 DC-DC Auxiliary Regulation and Multi-Stage Suppression Technology

Principle: Employs a capacitive DC-DC converter (VRCC) to generate a stable Boost voltage, as illustrated in Fig. 9 [15]. Coupled with a cascode output stage, it enhances the suppression of input power noise, its circuit diagram is shown in Fig. 10 [15].

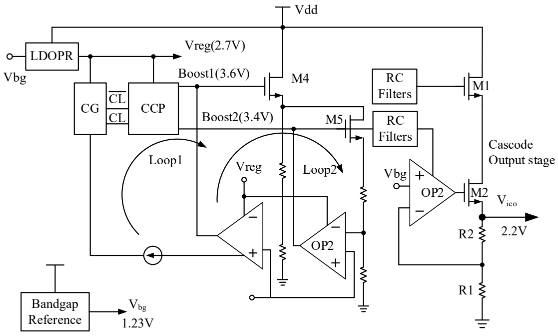

Figure 9. A voltage regulator using a capacitive dc–dc converter

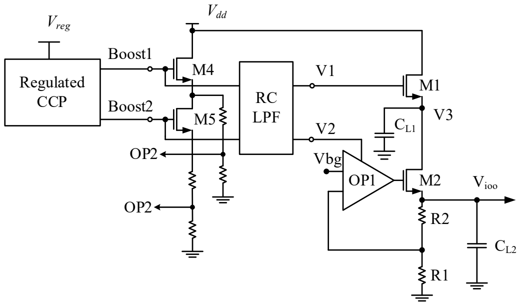

Figure 10. System-level diagram of cascode output stage with Boost voltage for high-frequency noise rejection

4.2.4 Voltage Subtractor and Feedback Optimization Technology

As shown in Fig. 11, it integrates a voltage subtractor (e.g., an NMOS transistor pair) into the power drive stage, enabling the error amplifier input to track power supply noise. This cancels ripple transmission through negative feedback [10]. Table 1 summaries the core technologies for reducing LDO noise and improving power supply rejection ratio.

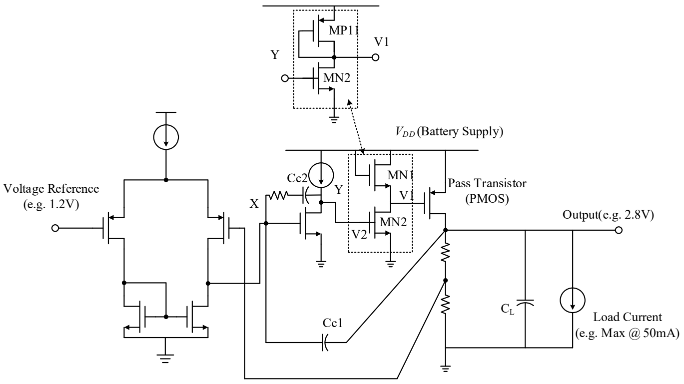

Figure 11. Implementation of PSR-boost technique

Table 1. Summary of Core Technologies for Reducing LDO Noise and Improving Power Supply Rejection Ratio (PSR)

Technology Category	Subcategory of Technology	Core Principle	Key Performance Indicators
		I. Core Technologies for Reducing LDO Noise	
1. Chopper Stabilization and Noise-Shaping Technology	Chopper Modulation + ΣΔ Noise Spectrum Spreading	Shifts low-frequency 1/f noise (from error amplifier/reference) to high-frequency bands via chopping; combines with first-order digital ΣΔ noise shaping to avoid noise concentration at the chopping frequency, followed by noise suppression through filtering.	- Noise spectral density: 32 nV/√Hz @ 100 kHz - Integrated noise: 14 μVrms @ 1 kHz~100 kHz - TCXO phase noise: 15 dB reduction @ 10 kHz offset
2. Capacitance Amplification and Efficient Filtering Technology	Small Capacitor + (-Gm) Amplifier (Mimicking Large Capacitor)	Constructs a capacitance amplification circuit using a "small capacitor C_m + resistor R_m+ negative transconductance amplifier (-Gm)" to equivalent a large filtering capacitor, suppressing reference noise transmission while saving chip area	- Filter capacitor: only 5 pF (100 pF required for traditional designs) - Integrated noise: 25.5 μVrms @ 10 Hz~1 kHz, 56.4 μVrms @ 1 kHz~1 MHz - PSR: -71.6 dB @ ≤49 kHz
3. Pre-Regulation and Noise Isolation Technology	Pre-Regulator + Power Driver Stage	Two-stage architecture: (1) Pre-regulator (reference buffer + RC low-pass filter) suppresses reference noise; (2) Power driver stage (voltage follower) eliminates thermal noise amplification from feedback resistors to achieve noise isolation.	- Integrated noise: 21.2 μVrms @ 1 kHz~100 kHz - PSR: 60 dB @ 10 kHz - Transient response: 1 μs (0→100 mA load, no ringing))
4. Device Selection and Local Noise Reduction Optimization	BJT-Based Bandgap Reference + Input RC Noise Reduction Module	(1) Constructs a bandgap reference using BJTs (reducing 1/f noise); (2) Adds an RC noise reduction module at the error amplifier input to shunt high-frequency noise; (3) Uses large-size input transistors to improve transconductance and reduce noise coupling.	- For 0.6μm BiCMOS: - Integrated noise: 15 μVrms@100 Hz~100 kHz - Bandgap noise: 3.7 μVrms@100 Hz~100 kHz

Technology Category	Subcategory of Technology	Core Principle	Key Performance Indicators
			- For 28nm CMOS: - Noise spectral density: 258 nV/√Hz@1 kHz - PSR: -81.9 dB@1 kHz
	II. Core Technologies for Improving LDO PSR		
1. Feedforward Path and Ripple Cancellation Technology	PMOS Current Mirror Feedforward Path	Introduces a PMOS pair (M1/M2) between the drain and gate of the power transistor (PMOS) to form a feedforward path; drives a current mirror to generate a ripple signal inverted to the supply noise, canceling noise at the output.	- For SMIC 0.18μm CMOS: - PSR: -71.6 dB@≤49 kHz, -65.7 dB@full frequency - For 0.6μm BiCMOS: - PSR: 75 dB@100 Hz, 72 dB@10 kHz
2. Cascode and High-Impedance Isolation Technology	Folded Cascode + Cascode Miller Compensation	(1) Adopts a folded cascode structure in the error amplifier to improve output impedance for supply noise isolation; (2) Uses cascode Miller compensation to push secondary poles/zeros beyond the bandwidth, ensuring wide-frequency loop stability and avoiding high-frequency PSR roll-off.	- Loop gain: 91 dB (pre-simulation) / 83.2 dB (post-simulation) - Phase margin: 79° (pre-simulation) / 78° (post-simulation) - PSR: -81.9 dB@1 kHz
3. DC-DC Auxiliary Regulation and Multi-Stage Suppression Technology	Capacitive DC-DC Converter (VRCC) + Cascode Output Stage	(1) VRCC generates a stable Boost voltage (3.6V) to power the cascode stage; (2) NMOS cascode output stage improves output impedance for multi-stage suppression of input supply noise; (3) RC low-pass filter eliminates DC-DC switching nois	- PSNR: 45 dB (mid-frequency band) - Jitter: 30 ps RMS (quiet supply) / 42 ps RMS (600 mV@20 MHz noise) - Locking range: 110~850 MHz
4. Voltage Subtractor and Feedback Optimization Technology	NMOS Voltage Subtractor + Feedback Tracking	Integrates an NMOS pair into the power driver stage to form a voltage subtractor, enabling the error amplifier input voltage to track supply noise; cancels the noise transmission path through negative feedback, achieving $A_{p1} \rightarrow 1$ (supply gain approaches 1)	- PSR: 60 dB@10 kHz - Output voltage accuracy: ±2% (full temperature range) - Area: 0.26 mm² (single output))

5. Conclusion

Advanced system-on-chip designs require LDO regulators with ultralow noise and high power supply rejection across frequency. Conventional LDOs are limited by inherent noise from references and amplifiers, plus poor high-frequency rejection.

This study outlines key techniques to improve performance. Chopper stabilization, capacitance amplification, pre-regulation, and BJT-based references effectively reduce noise. Feedforward cancellation, cascode-based amplifiers, DC-DC assistance, and feedback subtraction enhance power supply rejection.

Combining these methods enables LDOs to achieve microvolt-level noise and high power supply rejection ratio over wide bandwidths. These advances are essential for RF transceivers, precision data converters, medical implants, and automotive systems.

Future work may extend these techniques to advanced nodes, ultra-low-power operation, and wider input voltages to support AI, quantum, and wearable applications.

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