

Circuit Techniques for Overcoming Gain-Bandwidth Limitations in Amplifiers

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Abstract. This paper provides a comprehensive review of five core amplifier architecture: Cascode, Cascade, Gain Boosting, Current Cancellation, and Bootstrapping, which aims at breaking through the limitation of Gain-Bandwidth Product in modern electrical systems. Facing the demands of 5G/6G mobile communication, radar detection and medical imaging, this study systematically analyzes the principle, structure and performance of multiple techniques, clarifying its improvement effect on aspects such as gain, bandwidth, output impedance and stability. A comparative assessment of these architectures reveals their respective advantages in different application scenarios and process conditions. Furthermore, the paper also indicates that combining these circuits with FinFET and three-dimensional heterogeneous integration, will emphasize their combined potential to significantly boost linearity, noise performance, and power efficiency. The study also addresses ongoing challenges and future directions in implementing these techniques in mass production environments. These advancements offer critical support significant potential for next-generation high-frequency and high-precision amplifier designs, paving the way for more efficient and reliable electronic systems in emerging technological domains.

Keywords: Amplifier gain; cascode; cascade; gain boosting; current cancellation; bootstrapping.

1. Introduction

Driven by the advancement of fifth generation (5G) and the transition towards sixth generation (6G) mobile communications, high-performance radar detection, and advanced medical imaging, the demand for broadband high gain amplifiers of modern electronic systems exhibits explosive growth. In communication systems, the base station RF front-end must deliver over 30dB of gain across a bandwidth exceeding 1GHz to support high-speed data links in complex environments. In phased array radars, amplifiers must simultaneously offer high gain and wide bandwidth to enable long-range detection of weak targets and multi-frequency scanning. All these applications impose stringent demands on amplifier performance.

However, traditional amplifiers are constrained by the gain-bandwidth product (GBW), making it challenging to extend bandwidth while maintaining high gain—particularly in scenarios such as millimeter-wave bands (e.g., 28 GHz) and ultra-wideband radar systems (1–18 GHz). The GBW bottleneck remains one of the key factors limiting the development of RF integrated circuits and high-performance electronic systems.

Therefore, overcoming the limitations of the existing gain-bandwidth tradeoff and developing novel amplifier architecture and design methodologies have become central topics in both academic research and engineering applications. Systematic organizing research breakthroughs in aspects such as current topology, new semiconductor technology and cross-disciplinary integration methods, have a profound impact on promoting next-generation communication, detection and biomedical imaging technology development. This study aims at providing an overview on current state of development broadband high gain amplifiers, analyzing the advantages and disadvantages of mainstream technological routes and prospecting for future development directions.

2. Principle of Amplifier Gain

Amplifier gain is the basic indicator to measure the amplification capability of the input signal of amplifiers, usually defined as ratio of input signal to output signal. According to the signal type, gain can be categorized into voltage gain, current gain and power gain, etc. In operational amplifiers (op-amp), voltage gain is the most commonly used parameters, whose expression is:

$$G = \frac{V_{out}}{V_{in}} \quad (1)$$

In this expression, G represents gain, V_{out} represents output voltage, and V_{in} is the input voltage. In practical applications, negative feedback network is often used for controlling the gain of op-amps to stabilize it within the desired range, because of extremely high open-room gain of op-amps (typically reachable values range from 10^4 to 10^6 , and may even exceed these figures).

The magnitude of the gain not only depends on the circuit structure of amplifier itself but also affected by configuration method of external components such as resistor and capacitance. For example, the gain is defined by the ratio of feedback resistance to input resistance in inverting amplifiers. While in in-phase amplifiers, the gain is related to the feedback network and the resistance ratio of the input stage.

In addition to static gain, frequency also has an influence on the gain that cannot be ignored. Amplifier gain decreases with the increase in frequency because of parasitic capacitance and inductance in it. This characteristic is usually described as Gain-Bandwidth Product (GBP), and the indicator generally remains constant within a certain frequency range. Therefore, high-gain amplifier design must balance the relationship between gain and bandwidth to avoid signal distortion in high-frequency applications.

Additionally, factors such as temperature, power supply voltage fluctuations, and load variations can also affect gain stability. Therefore, in practical circuit design, techniques like temperature compensation, power supply rejection ratio (PSRR), and common-mode rejection ratio (CMRR) are employed to enhance gain accuracy and stability.

In short, amplifier gain is one of the core metrics in amplifier gain design. Understanding and optimizing involves multiple dimensions, including circuit topology selection, frequency response analysis, and stability assessment. This forms the foundation for achieving high-performance amplifier circuits.

3. Organization of the Text

3.1 Cascode

Cascode circuits represent one of the core techniques for achieving high gain in operational amplifier design. Their principle involves significantly enhancing output impedance through the superposition of transistors, thereby yielding voltage gain far exceeding that of simple common-source or common-drain configurations [1]. The basic circuit is illustrated in Fig. 1.

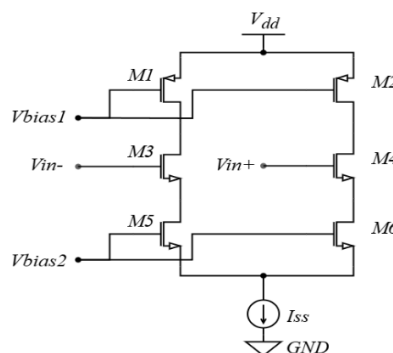


Fig 1. Basic cascode circuit.
(Picture credit: Original)

This technology is widely used in all kinds of operational amplifier architectures. For example, in Folded-Cascode operational amplifier, it not only provides high gain, but also maintains good frequency and swing of output [2]. In order to optimize frequency performance further, cascode structure is usually combined with advanced Miller compensation technique in application. For example, in fully differential two-stage op-amp, connecting compensation capacitor to common source common gate node, can change or eliminate right half plane zero point efficiently, expanding bandwidth [1]. In low voltage low power field, cascode is also vital. Research successfully achieved a gain of 40 dB, with total power dissipation only 112nW, by applying cascode current mirror as active load in 180 nm CMOS craft subthreshold op-amp [3].

In addition, cascode is indispensable in accomplishing high-precision performance indicators. In Track-to-Track input design, stable bias circuits need accurate circuit copies. High output impedance of cascode circuit mirror can ensure the bias current stable, not influenced by length modulation effect, then maintain constant transconductance (G_m) in the whole common mode range [2]. In high gain, high swing output pole design, the combination of cascode and Class-AB is proved to be an efficient scheme. One design with a 0.35 μm process achieving a gain of over 96 dB is a good example of it [4]. While in a design which pursues a very high gain-bandwidth product (GBW) and slew rate, researchers combined cascode, Adaptive Biasing and Feedback Technology, GBW of the new structure can be 9 times of traditional cascode structure according to reports [4]. Lastly, high output impedance characteristics of cascode structure benefit reducing sensitivity of the subsequent gain stage to the offset voltage, for its boosting effect decreases contribution coefficient of mismatch of threshold voltage in mirror nodes (ΔV_{th}) to general disorder, which is an important factor in optimizing precision [5].

3.2 Cascade

Cascode structure is widely applied in high performance operational amplifier design for its advantages in gain, bandwidth and output impedance enhancement. In multiple papers, cascode is applied in input pole, output pole or whole structure, to optimize comprehensive performance of amplifiers. The basic circuit is shown in Fig. 2.

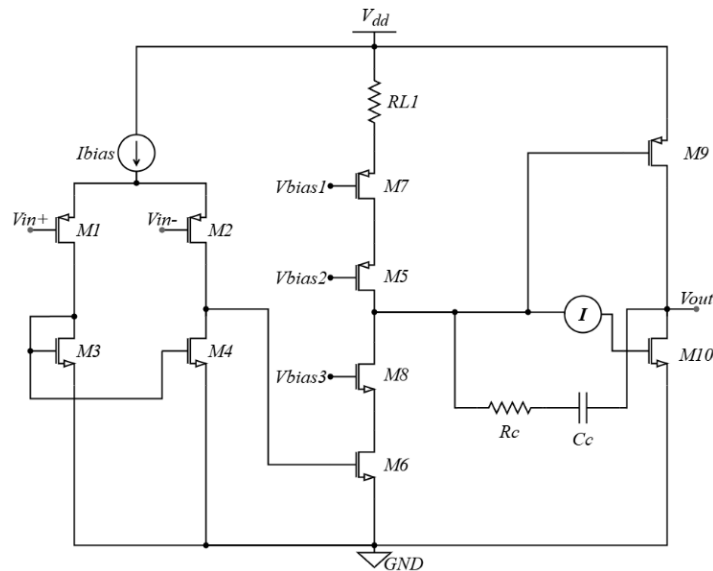


Fig 2. Basic cascode circuit.
(Picture credit: Original)

In Rail-to-Rail operational amplifier design, cascode input pole is utilized for improving transconductance (G_m), then increase DC gain, without adding the area significantly [6]. For example, a design combines PMOS input pole and cascode current mirror, realizing Common - Mode Rejection Ratio (CMRR) [7]. Another research enhanced GBW and slew rate (SR) further, by combining cascode structure and local common mode feedback (LCMFB) [8].

In output pole design, cascade structure is always combined with Class-AB output pole, in order to support greater output swing and current drive capability [7]. One high gain amplifier treats cascade common source pole as second level, coordinated with Miller compensation capacitor, realizing more than 90 dB gain and hundreds of MHz bandwidth [9]. Furthermore, cascade structure is used in increasing power supply rejection ratio (PSRR) and reducing noise, demonstrating exceptional performance, especially in low power consumption and high gain subthreshold operational amplifier design [10].

In power compensation, high impedance characteristics of cascade node are used in pole separation, combining Feed-Forward Compensation technology, expanding bandwidth further and improving phase margin [11]. One OTA design successfully boosts unity gain bandwidth to 4.5 MHz, meanwhile controls power consumption at 3.15 μW [11].

In summary, cascade structure plays a significant role in modern operational amplifier design, showing strong design flexibility especially in realizing multi-objective optimization such as high gain, high bandwidth, high stability and low power consumption.

3.3 Gain Boosting

Gain boosting is a technique that significantly enhances the open-loop gain of amplifiers through local feedback structures, widely used in high-precision analog integrated circuits. This technique achieves high gain by boosting output impedance while maintaining low power consumption.

In gain-boosted OTA structures, the gain boosting technique is applied to a continuous-time auto-zeroing amplifier (CTAZ), achieving a loop gain of 130 dB and an input offset voltage of only 2 μV through the use of a differential difference amplifier (DDA) and a gain-boosted OTA. This design, implemented in a 0.18 μm CMOS process, consumes only 27 μW under a 1.8 V supply voltage [12]. A cascode gain-boosting compensation structure proposes a two-stage operational amplifier employing a cascode gain-boosting structure. By introducing a gain stage (M6) in the feedback path of the Miller compensation capacitor, the unit gain bandwidth is significantly increased to 236 MHz, while achieving a gain of 92.5 dB and an ultra-low power consumption of 50 μW [13]. The basic circuit is shown in Fig. 3.

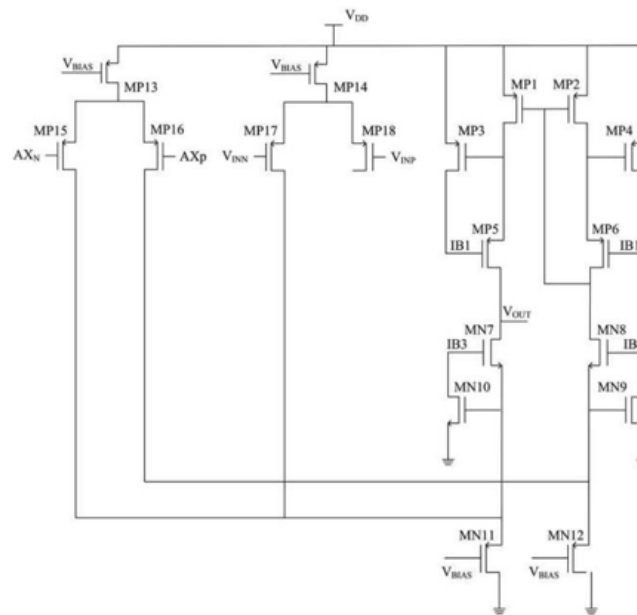


Fig 3. Differential Difference Amplifier schematic [12].

Gain boosting technology can also be combined with bulk-driven structures to overcome threshold voltage limitations in low-voltage design. In a structure combining bulk-driving with partial positive feedback, the transconductance of the bulk-driven input stage is enhanced via a partial positive feedback structure, further improving gain and common-mode rejection ratio (CMRR) [14]. Furthermore, a cross-coupled stage structure proposed in another work further enhances

transconductance and gain without increasing area. It is suitable for very low voltage (0.5 V) and ultra-low power (70 nW) applications [15].

Although gain boosting improves performance, it increases design complexity and requires careful balancing of stability and power consumption. Future research could focus on the optimization of multi-stage gain boosting structures, compatibility with advanced process nodes, and applications in biomedical and sensor systems.

3.4 Current Cancellation

This technique in CMOS operational amplifier design aims to eliminate the right-half-plane (RHP) zero introduced by Miller compensation, thereby optimizing the amplifier's frequency response characteristics.

Hurst et al. proposed embedding a cascode current buffer unit in the compensation path of a fully differential operational amplifier. This structure blocks the signal path directly coupling from the input stage to the output, transforming the original RHP zero into a left-half-plane (LHP) zero beneficial for stability, while also pushing the frequency of the secondary pole higher and increasing the unit gain bandwidth [16]. Analysis shows that this method significantly improves phase margin without altering the position of the dominant pole. The basic circuit is illustrated in Fig. 4.

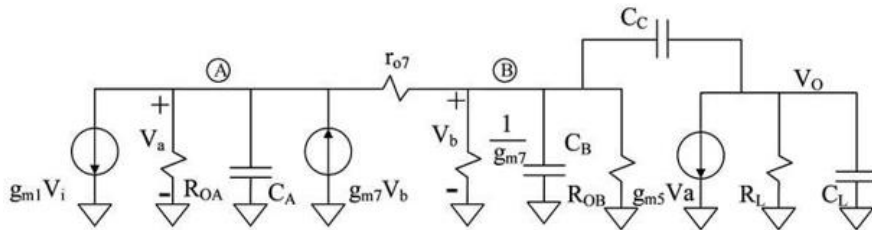


Fig 4. Small-signal differential-mode (DM) half-circuit [16].

Palumbo et al. implemented current buffering using a current mirror structure. A cross-coupled current mirror network forms the current control unit. Through precise adjustment of the current ratio, this structure can not only cancel the detrimental feedforward current but also proportionally reduce the value of the compensation capacitor, potentially saving chip area [17]. However, this scheme is more complex in handling common-mode signals and may introduce additional noise.

Other research achieved stabilization of the transconductance value through bias circuit optimization. This scheme uses a level-shifting circuit to make the operating regions of the tail currents for the complementary input pair overlap, ensuring minimal variation in the total gm across the entire input voltage range (e.g., below $\pm 4\%$), while also enhancing common-mode rejection capability and frequency response consistency [18].

In summary, cleverly designing the current path within the compensation network to cancel or steer feedforward currents is a feasible method for constructing high-performance, high-stability CMOS operational amplifiers, particularly suitable for analog and mixed-signal integrated circuits with low supply voltage and high precision requirements.

3.5 Bootstrapping

This technique extends the performance boundaries of low-voltage analog circuits by dynamically adjusting internal node potentials. It is particularly suitable for ultra-low voltage applications requiring wide input/output swing.

In a 0.4V fully differential OTA design, the Bhatkar team employed adaptive biasing technology, achieving dynamic current boosting through a cross-coupled structure. This design operates in the weak inversion region, maintains an ultra-low power consumption of 4.78 μ W, and achieves a gain of 51.15 dB and a bandwidth of 876.5 kHz [19]. Its innovation lies in achieving a near rail-to-rail input range through a bootstrapping mechanism.

The Panchal research group combined Bootstrapping with DT MOS technology to implement a variable gain amplifier under a 0.5V supply. Using a combined bulk-gate driving approach

significantly reduced the threshold voltage impact, achieving 78.35 dB open-loop gain with 8.35 μW power consumption [20]. This design approach provides a new implementation path for ultra-low voltage analog circuits. The basic circuit is shown in Fig. 5.

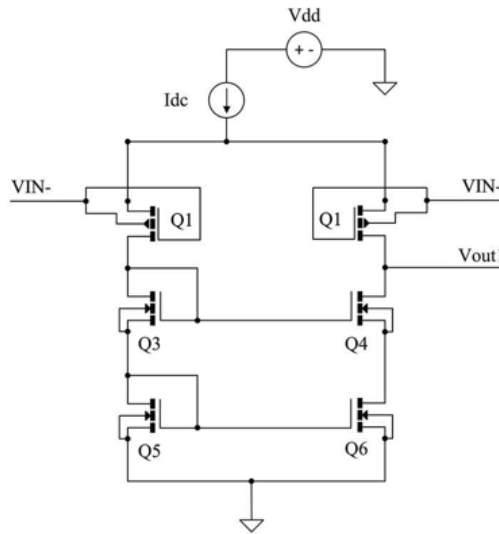


Fig 5. Dynamic Threshold Amplifier [20].

The HSMC technique proposed by Park et al. implements a super source follower function in the transient response through a dual current buffer structure. Test results show that this technique increases the slew rate to 30 V/ μs while reducing the settling time by 240%, greatly enhancing dynamic response performance under large capacitive loads.

In summary, bootstrapping technology can effectively solve design challenges in low-voltage analog circuits. Future work could further explore its combination with novel device structures to promote the development of ultra-low voltage analog integrated circuits.

4. Comprehensive Evaluation

4.1 Improved Parameters

All the five methods have advantages and disadvantages, and Table 1 lists comparison on the improved parameters of the five amplifier methods.

Table 1. Comparison of the improved parameters of different amplifier gain methods.

Parameters	[21]	[3]	[9]	[10]	[22]	[23]	[24]	[25]	[26]
Supply Voltage (V)	3.3	0.8	1.8	0.5	—	1.6-5.5	5	1	0.5
MOS Technology (μM)	0.5	0.18	0.13	0.18/0.09/0.045	0.25-0.6	0.25	0.18	0.09	0.18
DC Gain (dB)	—	40	55	74.21 (90nm)	—	—	106	54.53	78.35
Slew Rate (V/ μS)	—	0.005	38.66	0.033 (45nm)	59.7-	0.7	—	—	0.00714
UGB (MHz)	3	0.114	120	0.03162 (90nm)	266.66	1.5	43	1.7	0.355

5. Conclusion

This study systematically reviews the gain principles of five core amplifier structures: cascaded structures, gain-boosting structures, current-canceling structures, and bootstrap structures. Through in-depth analysis of topologies, application scenarios, and performance derivations of gain-doubling circuits, this research elucidates the intrinsic mechanisms for overcoming GBW limitations. Specifically: Cascade structures enhance output impedance and frequency response by optimizing topologies and reducing parasitic capacitance; Cascade structures achieve total gain multiplication

through multi-stage amplification; Gain enhancement techniques further boost gain without sacrificing bandwidth by adjusting core parameters like transconductance (Gm); Current cancellation and bootstrap techniques further optimize high-frequency performance by eliminating parasitic capacitance effects and enhancing input impedance, respectively. All these approaches not only achieve synergistic enhancement of gain and bandwidth but also provide critical insights for practical circuit design. Furthermore, integrating these circuit techniques with advanced processes like FinFET and 3D heterogeneous integration will significantly elevate overall amplifier performance, offering robust technical support and theoretical foundations for cutting-edge applications such as 5G/6G communication systems and high-performance radar detection.

Authors Contribution

All the authors contributed equally, and their names were listed in alphabetical order.

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