# Design Trade-offs in Current Mirrors: Precision and Power Efficiency

Yixun Zhang *

School of Nuclear Science and Technology, University of South China, Hengyang, China

* Corresponding Author Email: JT13550239424@outlook.com

**Abstract.** This paper systematically investigates the critical role and optimized design of current mirrors in analog and mixed-signal integrated circuits. Current mirrors replicate and scale input currents by leveraging the matching characteristics of semiconductor devices, and are widely used for functions such as biasing, active loads, and single-ended outputs. An ideal current mirror should exhibit high output impedance, high accuracy, and a wide output range; however, practical circuits face physical limitations leading to reduced impedance, mirroring errors, and limited frequency response. Based on analysis of various current mirror architectures in recent studies, this paper provides selection recommendations for different applications: low-voltage wide-dynamic-range Gm-boosted current mirrors are preferred in low-voltage scenarios for their high accuracy and impedance; for high-performance and high-swing requirements, regulated cascode current mirrors with improved voltage swing can be adopted, trading off area and power consumption for enhanced speed, output swing, and stability; tapered stacked-gate current mirrors effectively improve area, noise, and mismatch through layout optimization. Studies indicate that current mirror design requires balancing multiple constraints including precision, impedance, power consumption, and speed. Future research should integrate advancements in semiconductor technology and practical application requirements to further explore advanced architectures with higher accuracy and lower power consumption.

**Keywords:** Current mirror; transistor; impedance.

## 1. Introduction

A current mirror is a fundamental circuit structure commonly used in analog integrated circuits. Its principle involves replicating (or proportionally mirroring) the input current to generate an output current that is either equal to the input or maintains a fixed ratio with it. The current mirror primarily relies on the device matching characteristics of semiconductors. By sharing the same control voltage, it accurately copies a known reference current to one or more output branches.

Current mirrors are extensively utilized and can be found in nearly every analog and mixed-signal chip. Their primary applications include providing stable biasing, serving as active loads, and enabling single-ended output, among which supplying stable biasing represents the most widespread and core application[1].Despite its simple structure, the current mirror is a powerful and essential block in almost all analog integrated circuits and mixed-signal integrated circuits.

An ideal current mirror exhibits high output impedance, high-precision current replication, and a wide output voltage range[2]. However, practical circuits are constrained by physical device limitations and deviate from ideal behavior, manifesting issues such as finite output impedance, mirroring errors, and frequency response limitations. The optimized design of current mirrors involves understanding these theoretical principles and employing various circuit techniques to mitigate non-ideal characteristics, thereby achieving a balance among accuracy, output impedance, power consumption, and speed to meet specific application requirements. This paper surveys recent optimized designs of current mirrors and presents measured chip data to evaluate their performance.

## 2. Introduction to Different Types of Current Mirrors

### 2.1. Simple Current Mirror

The simple current mirror represents the simplest current mirror architecture. It consists of two matched transistors (BJT or MOSFET) and is designed to replicate current—generating one or more output currents $I_{out}$ that are either equal to or in a fixed ratio with a known reference current $I_{ref}$. Taking MOSFET as an example, by utilizing two NMOS transistors with identical dimensions and fabrication process, the following reference equations are obtained:

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{GS} - V_{TH})^2 \tag{1}$$

$$I_{OUT} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_{GS} - V_{TH})^2 \tag{2}$$

From Equations (1) and (2), we obtain:

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{3}$$

When receiving the paper, we assume that the corresponding authors grant us the copyright to use the paper for the book or journal in question.

When receiving the paper, we assume that the corresponding authors grant us the copyright to use the paper for the book or journal in question. When receiving the paper, we assume that the corresponding authors grant us the copyright to use.

### 2.2. Wilson Current Mirror

The Wilson current mirror is an ingenious and practical circuit architecture. Due to non-ideal characteristics, the basic current mirror exhibits limited output impedance, whereas the Wilson configuration significantly enhances output impedance, resulting in a more ideal and stable constant current source.

Typically constructed with three matched NMOS transistors [3], the Wilson current mirror operates as follows: M1 is diode-connected, through which the reference current $I_{REF}$ flows. M2 is also diode-connected and series-connected in the output branch. M3, configured as a common-source amplifier, has its drain serving as the output node from which the mirrored current $I_{OUT}$ is structure introduces a negative feedback mechanism that suppresses any tendency for the output current to increase, thereby forcing it to remain stable at the intended value. This feedback mechanism ultimately leads to a substantial increase in output impedance and improved current mirroring accuracy, while simultaneously achieving a self-biased circuit configuration.

This circuit requires both M2 and M3 to operate in the saturation region, the high output voltage requirement limits its application in low-supply-voltage scenarios. Additionally, the negative feedback introduced in the circuit results in reduced bandwidth and compromised stability, making it unsuitable for high-frequency operations.

### 2.3. Cascode Current Mirror

To address the issues of low output resistance and channel length modulation effects, a cascode transistor is added to the output branch of the basic current mirror, forming a stacked current mirror structure. This configuration exhibits extremely high output impedance, significantly enhancing the overall output resistance of the current mirror and effectively providing a highly precise and stable current source.

A standard cascode current mirror consists of four MOSFET, in which M1 and M2 serve as the core to perform current mirroring, while M3 and M4 form the cascode stage to enhance the output impedance and stabilize the voltage. By maintaining the drain-source voltages $V_{DS}$ of M1 and M2 at nearly identical levels, this structure significantly improves mirroring accuracy, effectively suppresses systematic errors, and reduces device mismatch to a certain extent.

The current cascode mirror also exhibits non-ideal characteristics. Due to its structural complexity and significant voltage headroom consumption, trade-offs and limitations remain inevitable in its operation. In contemporary applications, the standard cascode current mirror often fails to meet practical requirements, necessitating flexible adjustments based on supply voltage, required precision, bandwidth, and other performance constraints.

### 2.4. Improved Current Mirror

Most mainstream improved current mirror architectures are designed based on the three aforementioned current mirror types, aiming to address specific limitations encountered in practical applications.

The low voltage cascode current mirror represents an early improved architecture. The output node voltage requirement $V_{OUT}$ in a standard cascode current mirror is excessively high. To address this, an independent bias voltage $V_B$ is designed to precisely control the $V_B$. Compared to the standard cascode mirror, this approach significantly reduces the minimum required supply voltage, making it suitable for low-supply-voltage applications.

The wide-swing cascode current mirror represents a further optimization of the low-voltage cascode architecture, specifically designed to achieve the optimal voltage headroom. It replaces the single bias voltage in the cascode mirror with a complete bias circuit, enabling the output voltage to reach its theoretical minimum while maintaining the original high output impedance and high precision of the circuit structure.

## 3. Recent Advances in Circuit Optimization Design

### 3.1. Low-Voltage Wide-Dynamic-Range Gm-Boosted Current Mirror

This structure is a low-voltage level-shift current mirror, characterized by high output resistance and a wide input-output dynamic range[4]. The circuit architecture is illustrated in Fig. 1. Its core consists of a flipped voltage follower (FVF) unit formed by transistors M1-M4 in the input stage. In the current mirror design, the FVF module provides low input resistance and reduces the required input voltage for normal operation. To further enhance the output resistance of the output stage, a transconductance amplifier (OTA) configured in a gm-boosting topology is employed.

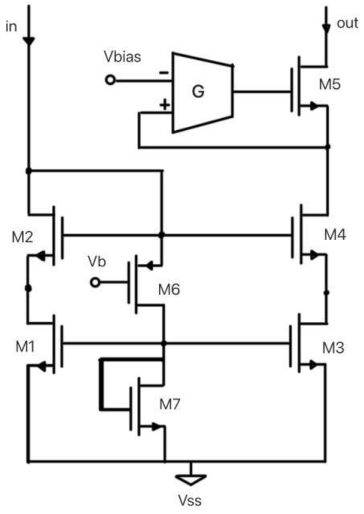

**Fig 1.** Current Mirror Simplified Design.

In Fig. 1, the gain of the gm-boosting OTA is typically controlled by its bias current $I_b$, which in turn regulates the current mirroring ratio $I_{OUT}$. The current source $I_b$ is replaced by a diode-connected transistor M7. Even with variations in transistor parameters, this feedback loop helps maintain a stable current transfer ratio[4]. The following equations represent simplified expressions derived from simulation:

$$\frac{I_{OUT}}{I_{IN}}=\frac{g_{m1}g_{m4}g_{m5}g_{m6}2(C_{gs1})g_{m5}C_{gs6}}{[s^3+s^2[\frac{g_{m6}}{C_{gs6}}+\frac{g_{m4}}{C_{gs4}}]+s(\frac{g_{m1}g_{m6}}{C_{gs1}C_{gs6}}+\frac{g_{m6}g_{m4}}{C_{gs4}C_{gs6}})+\frac{g_{m1}g_{m4}g_{m6}}{2(C_{gs1})C_{gs4}C_{gs6}}](g_{m5}+sC_{gs5})} \tag{4}$$

This design demonstrates a wide dynamic current range of up to 3 mA, providing a significant current mirroring range while minimizing the output swing to below 250 mV. By employing gm-boosting techniques, it enhances the output resistance to the giga-ohm range without compromising the output swing of the current mirror.

### 3.2.Regulated Cascode Current Mirror with Improved Voltage Swing

Due to the gradual transition between the triode and saturation regions in short-channel devices, drain voltage stabilization achieved through a source follower is insufficient. Therefore, actively regulating the VDS voltage can provide significantly enhanced stability[5].

This current mirror improves upon the cascode structure to maximize the output voltage swing across a wide range of operating conditions. The proposed circuit enables the use of short-channel devices, thereby optimizing the transient response speed of the current mirror. DC simulations were performed to validate the design, demonstrating its performance in a regulated cascode configuration with L=60 nm short-channel transistors and a 10 μA reference current.

This current mirror enables the translation of the regulated VDS voltage of the reference transistor to an optimal VDSAT value. VDSAT demonstrates excellent stability across PVT corners, allowing the structure to be employed in high-performance circuits such as nanosecond-scale laser current sources for optical communication.

### 3.3.Electrostatically Adaptive Current Mirror

The Germanium field-effect transistor adaptive current mirror is designed based on a newly proposed CMOS-compatible technology[6]. This current mirror features the capability for electrostatic compensation of inter-device variations, thereby realizing an ideal current mirror that can even switch between n-type and p-type operation.

Leveraging the electrostatic controllability of transistors, this current mirror proposes a compensated RFET-based architecture capable of establishing programmable mirroring ratios across various operating ranges through gate modulation. Compared to conventional MOSFETs with statically fixed characteristics, the reconfigurable field-effect transistor (RFET) inherently achieves adaptability, allowing not only dynamic switching between n-type and p-type operation but also drain current scaling driven by additional control voltages. The ideal behavior of this current mirror was simulated using Cadence Virtuoso under the following conditions: a supply voltage of 0.8 V, a constant VPG1 of 0.7 V, and a load resistance of 1 MΩ. Simulation results demonstrate comparable yet proportionally scaled electrostatic gate controllability.

### 3.4.High-Swing Super Wilson Current Mirror

This high-impedance current mirror utilizes a self-biasing technique in place of a conventional bias circuit. The power supply of the proposed circuit is reduced from 0.8 V to 0.5 V. This lower supply voltage results in reduced power dissipation while minimizing DC current errors[7].

In this circuit, a diode-connected transistor is employed to reduce the current mismatch between the reference and output branches by maintaining the reflection transistor in depletion mode. The design addresses issues such as low output impedance by utilizing five NMOS and three PMOS transistors. The PMOS transistors function as current sources, with the current through PM2 being replicated to PM1 and PM3. All cascode current mirrors in the structure are self-biased, exhibiting high output impedance and low systematic matching errors. Each requires an input voltage equivalent to two diode drops. Beyond the compliance voltage, each stage maintains a consistent output voltage margin equal to a diode drop. Consequently, the proposed circuit operates efficiently even at lower input voltage ranges.

### 3.5.Tapered Stacked-Gate Current Mirror

Tapered stacked-gate devices offer advantages such as area efficiency, reduced noise, and improved matching performance, making them widely applicable in various circuits. In the stacked stages of the current mirror structure, a varying number of transistors are employed, which not only reduces the number of transistors on the source side but also maintains comparable mismatch and noise characteristics[8]. Furthermore, using the same number of devices, this design achieves superior performance in simulations.

The current mirror utilizes a tapered stacked transistor structure, as illustrated in Fig. 2, which is named "tapered stacked gate" due to its geometric profile. This tapered stacked-gate configuration reduces the area occupied by the transistors on the source side. Furthermore, by employing a varying number of transistors at each stacking stage, this structure effectively functions as a source-degeneration resistance. This approach not only preserves the identical width-to-length (W/L) ratio but also minimizes the physical area while emulating the behavior of negative feedback resistors. During simulation, the total area of the current mirror was measured to be 1305 μm². Compared to conventional stacked-gate designs, the tapered stacked-gate architecture achieves a 25% reduction in oscillator area while maintaining equivalent noise performance, along with a nearly 45% decrease in noise and a 28% improvement in mismatch tolerance.

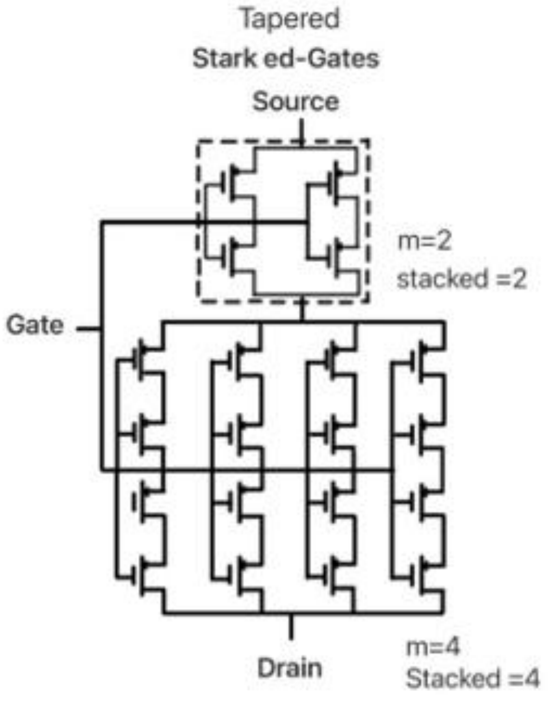

**Fig 2.** Novel Tapered Stacked Transistor Device.

## 4. Parameter Comparison

Several recent current mirror designs have been studied and statistically analyzed, with key parameters including bandwidth, DC gain, input current, power consumption, and transistor count compared in table 1.

**Table 1.** Parameter Comparison.

| | [9] | [10] | [11] | [12] | [13] |
|---|---|---|---|---|---|
| Bandwidth | - | 623MHz | 9.8KHz | 63.68MHz | - |
| DC Gain | - | - | 61.2dB | 54.07dB | 76dB |
| Input Current | -60A-60A | 10uA | 1.67mA | 750uA | 1.95nA |
| Power Consumption | 150uW | 69.55uW | - | - | 1.95nW |
| Supply Voltage | 0.75V | 1.5V | 1.8V | 1.5V | 1.3V |
| Transistor Technology | 0.18um | 0.18um | 0.18um | 0.11um | 0.18um |
| Transistor Count | 3 | 4 | 3 | 10 | 16 |

## 5. Conclusion

Based on the investigation of various current mirror architectures and the statistical analysis of their parameters, suitable current mirrors can be selected according to specific application requirements.

The preferred choice due to its high output impedance and high mirroring accuracy, making it well-suited for providing stable current sources under low supply voltages. The high-swing super Wilson current mirror also performs effectively in low-voltage conditions, though its overall performance is comparatively inferior to the former.

For applications demanding high performance and wide output swing, the regulated cascode current mirror with improved voltage swing can be employed. To mitigate short-channel effects and achieve high-speed response, this current mirror sacrifices area and power consumption in exchange for enhanced speed, output swing, and PVT stability, positioning it as a high-performance current mirror architecture.

The tapered stacked-gate current mirror is designed to address mismatch and noise issues in circuits. It significantly improves area efficiency, noise performance, and matches characteristics through optimized layout design, thereby enhancing conventional current mirror architectures.

The current mirror is a critical building block in analog integrated circuits. With advancements in modern semiconductor processes, novel current mirror architectures continue to evolve and improve. Future research on emerging current mirror designs should focus on targeted development aligned with practical application requirements, while also keeping pace with cutting-edge industry trends to achieve higher precision and lower power consumption.

## References

[1] S. Sabharwal, J. Kaur and A. Shahi, "Various Current Mirror Topologies: A Survey," 2022 2nd International Conference on Advance Computing and Innovative Technologies in Engineering (ICACITE), Greater Noida, India, 2022, pp. 504-508.

[2] Monika and P. Mittal, "Different Current Mirror Topologies at Multiple Technology Nodes: Performance Comparison and Parameters Extraction," 2021 International Conference on Simulation, Automation & Smart Manufacturing (SASM), Mathura, India, 2021, pp. 1-7.

[3] R. Bhardwaj, R. Srivastava, R. Kandari and A. Kumar, "Comparative Analysis of Wilson Current Mirror utilizing FGMOS and QFGMOS Technique," 2022 IEEE Delhi Section Conference (DELCON), New Delhi, India, 2022, pp. 1-5.

[4] A. Dadheech, N. Raj and D. Rawal, "Low Voltage, Wide Dynamic Range Gm-Boosting Current Mirror for High Performance Application," 2024 IEEE Silchar Subsection Conference (SILCON 2024), Agartala, India, 2024, pp. 1-6.

[5] V. Michal, "Regulated Cascode Current Mirror with Improved Voltage Swing," 2022 International Conference on Applied Electronics (AE), Pilsen, Czech Republic, 2022, pp. 1-4.

[6] A. Fuchsberger et al., "Electrostatically Adaptable Current Mirror based on Germanium Field-Effect Transistors," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5.

[7] P. Singla, R. Mittal, P. Sahni and P. K. Sharma, "Redesigning of High Swing Super Wilson Current Mirror Circuit," 2023 3rd Asian Conference on Innovation in Technology (ASIANCON), Ravet IN, India, 2023, pp. 1-4.

[8] C. -E. Hsia et al., "Current Mirrors with Tapered Stacked-Gates for Area Saving or Noise Improvement in 3nm FinFET Process," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2.

[9] H. Yadav and U. Bansal, "A Novel Low-Voltage Low-Power FGMOS and CMOS Resister-Based Current Mirror," 2021 International Conference on Industrial Electronics Research and Applications (ICIERA), New Delhi, India, 2021, pp. 1-4.

[10] B. Pruthwiraj, A. K. Mishra and D. Vaithiyanathan, "A Low Power CMOS Analog Multiplier using Regulated Cascode Current Mirror based on Translinear principle," 2022 IEEE 3rd Global Conference for Advancement in Technology (GCAT), Bangalore, India, 2022, pp. 1-4.

[11] A. Mezaour, M. Kadry, F. L. Goff, D. Bourke, T. Finateu and C. Posch, "A >150dB dynamic range, enhanced input swing, high precision current mirror in 180nm CMOS technology," 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5.

[12] D. Liu, T. Wei, S. Chen and N. Chen, "An Improved Recycling Folded-Cascode Amplifier with Nested Current Mirror for Front-end Readout ASIC," 2022 IEEE 2nd International Conference on Electronic Technology, Communication and Information (ICETCI), Changchun, China, 2022, pp. 281-284.

[13] K. Yu, J. Chen, S. Li and M. Huang, "A 0.011%/V LS and −76-dB PSRR Self-Biased CMOS Voltage Reference With Quasi Self-Cascode Current Mirror," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 3, pp. 1052-1056, March 2024.