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Effect of Green Logistics on Designing of Single Bit Cache Memory Architecture

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Abstract:

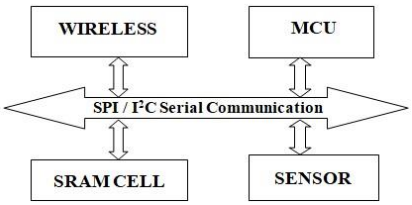
The international economy's fast expansion has made logistics more crucial in addressing shifting societal demands and has also worsened sustainability and environmental issues. With an emphasis on entering and leaving logistics, this study examines the long-term effects of green logistics practices. The paper creates a theoretical framework for examining the effects of green logistical practices on single-bit cache memory architectures' economic, social, and environmental performance. This paper proposes and implements a design analysis of a single-bit static random access memory voltage differential sense amplifier architecture. It uses a write driver circuit, a static random access memory, and different differential sense amplifiers, including voltage differential sense amplifiers, current differential sense amplifiers, and charge transfer differential sense amplifiers. How well different architectures perform in terms of total power consumption, static power consumption, transistor count, and sensing delay has been determined. The voltage differential sensing amplifier for single-bit static random-access memory cells utilizes the least power (13.16μW). Longer sensing delays (12.5ηs) are present in the single-bit static random-access memory cell charge-transfer differential sense amplifier design and the single-bit random-access memory cell current differential sense amplifier architecture. Techniques for power reduction have also been employed to optimize power.

Keywords: Internet of Things (IoT), Low Power Reduction Techniques (LPRT), Differential sense amplifier (DFSA), Complementary metal-oxide-semiconductor (CMOS), Integrated circuit (IC).

1. Introduction

With the rapid expansion of the global economy, logistics has become increasingly important in addressing the changing demands of society. However, this growth has also had several detrimental effects on the environment, society, and the long-term viability of businesses. As environmental concerns increase, businesses are being forced to evaluate the external costs of logistics, including those brought on by air pollution, climate change, noise, vibrations, and accidents. Thus, striking a long-term balance between economic, social, and environmental goals has become a business's main responsibility. Applications for semiconductors have expanded in a variety of sectors, including industry, agriculture, medicine, and the internet of things (IoT). An integrated circuit (IC) requires more power as its functional parameters expand daily. The complementary metal-oxide-semiconductor (C_{MOS}) industry has developed to the point where it can produce items like this. Because there are not

many power outlets near portable handle devices, a long-lasting battery backup system is necessary, as shown in schematic 1.



Schematic: 1 IoT Sensor Node Block Structure

The most crucial CSRAMC-based cache comprises very large-scale integrated circuit (VLSI) chips. The performance of memory and peripheral circuits can slow down speed and power. The most crucial aspect of the CSRAMC cache architecture is how to read the data. After the latching procedure, the electricity is cut off. Static electricity is absent from the differential sense amplifier (DFSA) and remains constant. As a result, the time it takes to sense and latch on is related to power loss. It occupies 90% of the chip's surface area. As a result, the on-chip loses power. Because mobile devices do not have many locations to plug in, low-power dissipation devices are crucial for technology [6]. Single-bit cache memory architecture (SBCMA) with various DFSAs is planned.

1.1 Internet of things and Cache Memory

A concept known as the Internet of Things (IoT) enables embedded devices to connect to the internet and gather and share data. It makes it possible for gadgets to collaborate and interact with one another. This group contains everyday household objects to complex industrial tools [7]. Most data delivered over the network can be cached, notwithstanding the volume and variety of data collected by the IoT. Caching can improve the performance of an IoT network. File copies are retained in a temporary storage area during the caching procedure to make them locally accessible. There are numerous methods for caching. It is necessary to choose the optimal caching method for the IoT network [8].

IoT network devices process data streams using multimedia or control signal processing hardware [9]. The primary purpose of these devices is to use batteries. Researchers are considering specialized optimization approaches for improving battery life because battery operation time has emerged as a crucial criterion for IoT devices [10]. Memory is a power-hungry component that is used by many IoT device components. The power consumption of the memory system is decreased when the cache memory is used actively.

1.2 Design of a Reliable Sensor Node Cache Memory

Transistor features continue to decrease past the sub-45ηm range as semiconductor technology develops. As silicon technology has been aggressively scaled, the effect of process variations on device parameters like channel length, oxide thickness, threshold voltage, and random positioning of dopants has grown. Extended access times, substantial power leakage, and very high temperatures might occur due to changes in crucial process parameters. Process differences substantially impact cache memory circuits because they are often built using tiny transistors. Due to process changes, cache memory cells with various properties cannot fully complete read/write operations, leading to system failure or considerable performance loss. Chip yield is one of the most critical areas for improvement due to

lowering transistor feature sizes, which have significantly increased the complexity and cost of manufacture. An adaptive design approach that considers transistor feature size downscaling and can handle cache memory variability is adopted to achieve a high chip yield. One of the most urgent problems is extending the lifespan of sensor network nodes. Various metrics, such as processing power reduction, communication message reduction, and energy-efficient protocol design, can be used to assess a network's longevity. All these techniques are software-based and targeted at increasing the network's life. In terms of efficiency, memory is one of the most critical components of software lifetime since process variation can damage the cache block of sensor node memory, leading to node failure. In a static sensor network, a crucial node, such as one close to the base station, might harm the entire sensor network, whereas frequent node damage in mobile sensor networks can shorten the network's lifespan. Sensor nodes are routinely deployed in hazardous situations, increasing the likelihood of process deviations. Developing a skill that can be applied in every circumstance is crucial.

1.3 Low Power Reduction Techniques

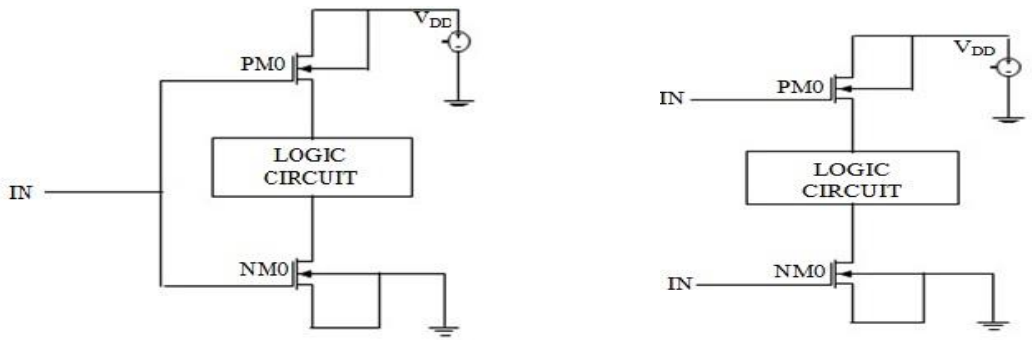
A small number of power-saving strategies are covered in this section. In this section, researchers discuss how transistors function in power reduction strategies and how power reduction techniques work in the logic circuit.

1.3.1 Low Power Sleep Transistor Technique (STT)

The sleep transistor technique switches, as shown in the schematic: 2(a). In the sleep transistor technique, PMOS0 and NMOS0 are used as a switch in a circuit. In this technique, instead of a voltage supply, $PMOS_0$ is used, and in place of ground, $NMOS_0$ is used in the logic circuit [7]. When the logic circuit is in operation, $PMOS_0$ is in the active region, and $NMOS_0$ is also in the active region; however, when the circuit is in standby mode, $PMOS_0$ is in the cut-off region, and $NMOS_0$ is also in the cut-off region, resulting in a lower power consumption [8]. Both $PMOS_0$ and $NMOS_0$ have different supply inputs.

1.3.2 Low Power Forced Stack Technique (FST)

In the forced stack technique, instead of using voltage supply, $PMOS_0$ is used, and in place of ground, N_{M0} is used in the logic circuit, as shown in schematic: 2(b). In this technique, both MOS have the same input. When $PMOS_0$ is in the active region, $NMOS_0$ is in the cut-off region [9]. Due to this, the circuit doesn't have a power supply, which helps to consume less power.

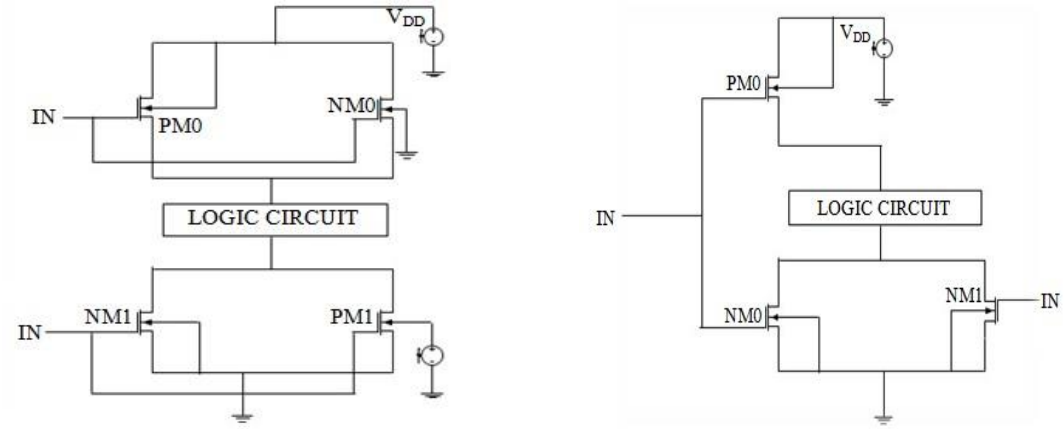


(a) **(b)**

Schematic: 2 (a) STT Structure (b) FST Structure

1.3.3 Low Power Sleepy Stack Technique (SST)

In this technique, three transistors are used $PMOS_0$, $NMOS_0$, and $NMOS_1$, as shown in Schematic: 3(a). In this technique, both $NMOS_0$ and $NMOS_1$ are connected in parallel. In place of the voltage supply, $PMOS_0$ is used, while ground, $NMOS_0$, and $NMOS_1$ are used in the logic circuit [10]. $PMOS_0$ and $NMOS_0$ have the same input in this technique, while $NMOS_1$ has different inputs. When the circuit is in working mode, $PMOS_0$ is in the active region, $NMOS_0$ is in the cut-off region, and $NMOS_1$ is in the active region. When the circuit is in standby mode, $PMOS_0$ is in the cut-off region, $NMOS_0$ is in the active region, and $NMOS_1$ is in the cut-off region. Due to this, our circuitry consumes less power [11].



(a) **(b)**

Schematic: 3 (a) SST Structure (b) DST Schematic Structure

1.3.4 Low Power Dual Sleep Technique (DST)

In this technique, four transistors are used $PMOS_0$, $PMOS_1$, $NMOS_0$, and $NMOS_1$. In this technique, $PMOS_0$ and $NMOS_0$ are connected in parallel in place of the voltage supply of circuitry, and while in place of ground, $PMOS_1$ and $NMOS_1$ are in parallel connection in the logic circuit [12]. $PMOS_0$ and $NMOS_0$ have the same input in this technique, while $PMOS_1$ and $NMOS_1$ have the same input. When the circuit is in working mode, $PMOS_0$ is in the active region, $NMOS_0$ is in the cut-off region, $NMOS_1$ is in the active region, and $PMOS_1$ is in the cut-off region. $PMOS_0$ is in the cut-off region, $NMOS_0$ is in the active region, $NMOS_1$ is in the cut-off region, and $PMOS_1$ is in the active region when the circuit is in standby mode [13]. Due to this, our circuitry consumes less power, as shown in schematic: 3(b).

After the introduction, Section 2 discusses the related work done from 2001 to 2022 by different authors, whereas section 3 describes the block structure of single-bit cache memory architecture work. Each block circuitry and the working process have been discussed in detail. There are many parts in a single-bit architecture, and this section shows how they work with a circuit diagram. Section 4 discusses the output waveforms of proposed circuits and compares them to other circuit designs. Section 5 describes the summary of the paper in the form of a conclusion with future scope.

2. Literature Review

Complementary metal-oxide-semiconductor (C_{MOS}) memory performance depends on how long and how much power sense amplifier (SA) uses. Using ultra-low-voltage $CSRAM_C$ in applications like

biomedicine, wireless sensors, and implantable devices can save a lot of power. The standard $CSRAM_C$ is used a lot. Cross-coupled types of C_{MOS} inverters are simple DFSA's, and they are the same as simple DFSA's. They work simultaneously as input lines. The memory cell or the whole $CSRAM_C$ Block is essential in this work, but the $CSRAM_C$ DFSA's don't get much attention [5]. Table:1 describes different authors' work in single-bit cache memory architecture from 2001 to 2022.

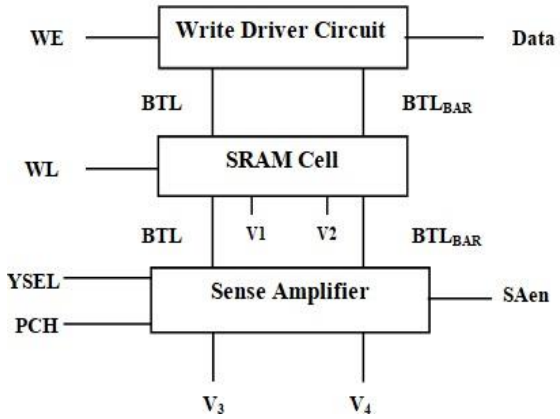
Table:1 Related work proposed in single-bit cache memory architecture between 2001 and 2022 by various authors

Year	Author	Features	C_{MOS} Technology	Supply Voltage
2001	**D. Schmitt-Landsiedel, et al. [14]**	A bit line multiplexer switches bit in the $CSRAM_C$ CDFSA.	180ηm	1.8V
2002	**F. Hamzaoglu et al. [15]**	$CSRAM_C$ with swing single-ended bit lines.	130ηm	1.3V
2003	**A. Alvandpour et al. [16]**	High-performance and low-voltage sense amplifiers	90 ηm	1.2V
2004	**D. Schmitt-Landsiedel et al. [17]**	Speed optimization of a latch-type sense amplifier	130ηm	0.7V
2005	**W. Burleson et al. [18]**	Sensing using in C_{MOS} $CSRAM_C$ with various sense amplifiers	70ηm	0.6V
2006	**H. Mahmoodi et al. [19]**	Robust sense amplifier using independent gate control	50ηm	0.5V
2007	**M. Margala et al. [20]**	Self-biased charge transfer sense amplifier	180ηm	0.6V
2008	**Y. Kiat-Seng et al. [21]**	Hybrid $CSRAM_C$ DFSA with a new transistor sizing approach	180ηm	0.9V
2009	**Z. Kong et al. [22]**	The new current mode sense amplifier	65ηm	1V
2010	**Chia-Tsung Cheng et al. [23]**	Speedy CDFSA for MRAM that sends spin torque.	180ηm	1.8V
2011	**S. Chen et al. [24]**	Content addressable memory (CAM) with efficient power and delay trade-off	65ηm	1V
2012	**Z. Kong et al. [25]**	The memory has a parity bit and is power-gated for machine learning.	65ηm	1V
2013	**S. Hamdioui et al. [26]**	Bias temperature instability impact on $CSRAM_C$ DFSA	45ηm, 65ηm, 90ηm	1V
2014	**K. Velayudhan et al. [27]**	CAM uses a small match line swing and background state machines.	65ηm	1.2V
2015	**S. Motaman et al. [28]**	Slope detection technique for robust $CSRAM_C$ sensing.	90ηm	1V
2016	**I. Agbo et al. [29]**	DFSA offset voltage decreases due to zero and runtime changes.	65ηm	1.2V

2017	**J. O. Klein et al. [30]**	Hybrid C_{MOS}/Magnetic tunnel junction logic circuit architecture	40ηm	1V
2018	**J. Park et al. [31]**	Ternary CAM using adaptive machine line discharge scheme	65ηm	1V
2019	**A. Surkar et al. [32]**	Analyze current and voltage sense amplifiers' delay and power.	180ηm	1.8V
2020	**Y. Wang et al. [33]**	Low static current sense amplifier for $CSRAM_C$	180ηm	1.4V
2021	**Chen, Jian, et al. [34]**	Reconschematicurable sense amplifier for computing $CSRAM_C$	55ηm	1.2V
2022	**Agrawal, Reeya, et al. [35]**	$CSRAM_C$ is a low-power architecture for the internet of things.	90ηm	1.2V

3. Block Structure of Single-Bit Cache Memory Architecture

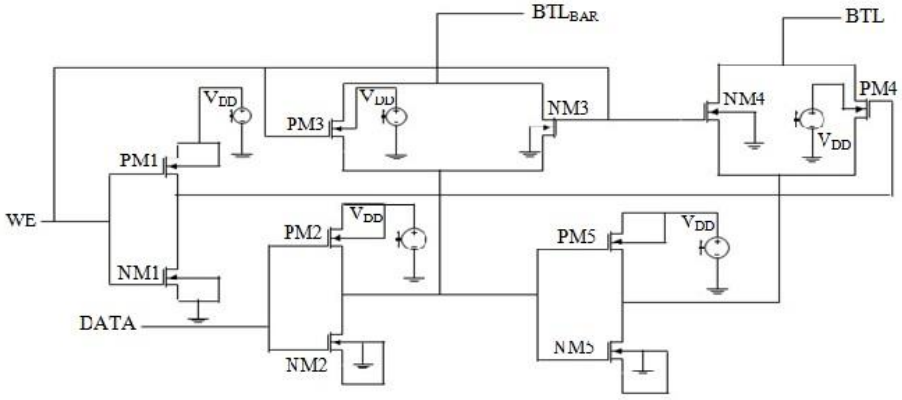
The architecture is made up of three parts, as shown in schematic:4: a circuit of write driver (CoWD), a conventional static random access memory cell ($CSRAM_C$), and a differential sense amplifier (DFSA). There are six input pins and eight output pins on this block. The CoWD has two input pins, word enable (WE) and DATA, and two output pins, BITL and BITLBAR, connected to the $CSRAM_C$ via bit lines. The $CSRAM_C$ comprises one input pin, i.e., WL, and two output pins (V_1 and V_2). Bit lines connect the DFSA to the $CSRAM_C$. The five input pins on the DFSA are YSEL, PCH, BITL, BITLBAR, and SAEN, and the two output pins are V_3 and V_4.



Schematic: 4 Block Structure of Single Bit Cache Memory Architecture

3.1 Circuit of Write Driver (CoWD)

The circuit of the write driver (CoWD) stores data in the $CSRAM_C$, and schematic: 5 shows the CoWD design. The write margin is reduced by CoWD [36]. The circuit's job is to charge or discharge the BITL and BITLBAR in the memory cell to the desired DATA. It comprises ten-transistor such as $PMOS_1$, $PMOS_2$, $PMOS_3$, $PMOS_4$, $PMOS_5$, $NMOS_0$, $NMOS_1$, $NMOS_2$, $NMOS_3$, $NMOS_4$, and $NMOS_5$ [37].



Schematic: 5 CoWD Circuit

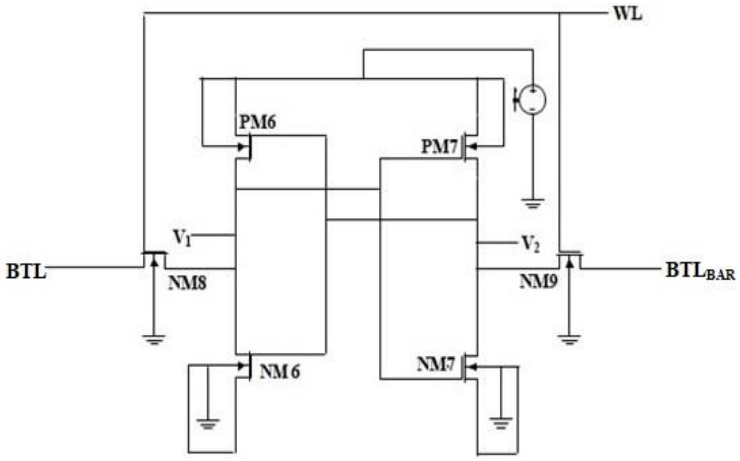
3.2 Conventional static random access memory cell (CSRAM$_C$)

A static random-access memory cell known as a conventional static random-access memory cell (CSRAM$_C$) is a type of static random-access memory cell used as cache memory in computers. It has bistable inverters for storage PMOS$_6$, PMOS$_7$, NMOS$_6$, and NMOS$_7$ are crossed-coupled inverters [38], as shown in the schematic: 6. NMOS$_8$ and NMOS$_9$ are access transistors used to access stored data for reading and writing operations and connected to BITL and BITLBAR.

$$\frac{(\frac{W}{L})_3}{(\frac{W}{L})_1} < \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}-2V_{T,n})^2}$$

$$\frac{(\frac{W}{L})_5}{(\frac{W}{L})_3} < \frac{\mu_n}{\mu_p} \cdot \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}+2V_{T,p})^2}$$

Access transistors are turned off when WL = LOW. When WL = HIGH, read or write operations have been done; access transistors are turned on, new data is applied to BITL and BITLBAR, and the data in the latch is overwritten with the new value. DFSAs read the data in BITL and BITLBAR. BITL and BITLBAR are linked to the CoWD and DFSA. DFSA, resistance, and capacitance are all linked together through bit lines.



Schematic: 6 CSRAM$_C$ Circuit

3.3 Description of Differential Sense Amplifiers (DFSA)

A differential Sense Amplifier (DFSA) is an essential circuit in $CSRAM_C$ architecture. DFSA is used for a read operation in the $CSRAM_C$. BITL = LOW, BITLBAR = HIGH, BITL = HIGH, and BITLBAR = LOW during the reading operation. This slow discharge of the bit line capacitance and access transistor is small. Due to this, a slight difference between bit lines is sensed and amplified by DFSA [42]. The total width of the transistors has been kept equal for all DFSAs.

3.3.1 Working of Voltage Differential Sense Amplifier (VDFSA)

The VDFSA has three input pins: YSEL, PCH, and SAEN, and two output pins: V3 and V4, which are connected using resistance and capacitance via BITL and BITLBAR [43].

3.3.2 Working on Current Differential Sense Amplifier (CDFSA)

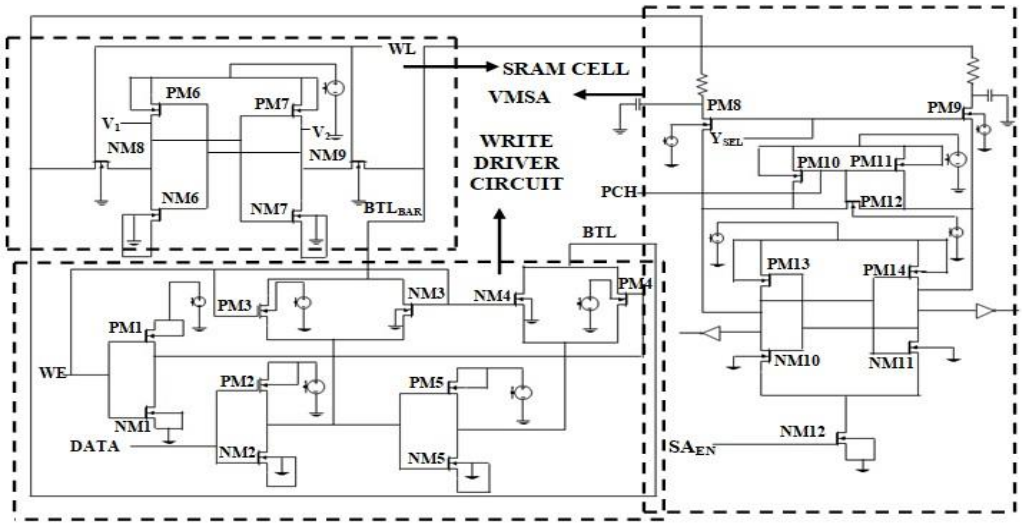
The CDFSA is divided into a) a current-transporting circuit with unity-gain current transfer characteristics and b) a current sense amplifier that senses the differential current. Four positive feedback PMOS transistors ($PMOS_8$, $PMOS_9$, $PMOS_{10}$, and $PMOS_{11}$). The internal nodes A and B are already set up with a PMOS, so each read cycle has the same delay and latching time. The second current sense amplifier is connected to the output of a circuit that moves electricity to determine how much electricity is flowing.

3.3.3 Working of Charge-Transfer Differential Sense Amplifier (CTDFSA)

The CTDFSA component detects variations in the amount of electricity flowing. Positive feedback PMOS transistors are used in this case. $PMOS_8$, $PMOS_9$, $PMOS_{10}$, and $PMOS_{11}$ are the four transistors that support positive feedback. There is no need to do anything because internal nodes A and B have already been set up to have the same delay and latching time when they are read. The second CDFSA receives the output of the circuit that moves the current.

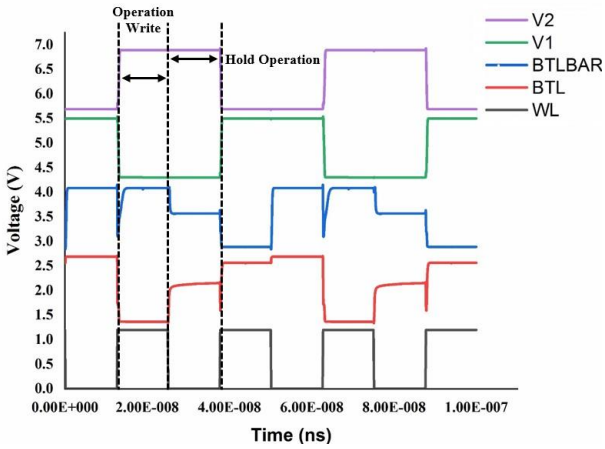
4. Discussion and Analysis of Result

Schematic:7 shows single-bit $CSRAM_C$ VDFSA architecture implemented with CoWD, $CSRAM_C$, and VDFSA as a DFSA. During the pre-charge period, the pre-charge circuit is very active.



Schematic: 7 Single-Bit $CSRAM_C$ VDFSA Architecture

YSEL = HIGH, PCH = LOW, $PMOS_{8,}$ and $PMOS_9$ are cut-off, while $PMOS_{10}$, $PMOS_{11}$, and $PMOS_{12}$ are active, and BITL and BITLBAR are PCH to the full rail swing. Because $NMOS_{12}$ is in cut-off mode, WL = LOW, indicating no read operation, and SAEN = LOW, indicating that DFSA does not detect any data. YSEL = LOW throughout evaluation, PCH = HIGH to pre-charge BITL and BITLBAR, and $PMOS_8$ and $PMOS_9$ are active. While $PMOS_{10}$, $PMOS_{11}$, and $PMOS_{12}$ are cut-off, data on the BITL and BITLBAR goes through the DFSA, WL of $CSRAM_C$ = HIGH for reading operations, i.e., access transistors are turned on BITL = LOW. BITLBAR = HIGH, i.e., voltage difference = HIGH at the output, and SAEN = HIGH for half positive cycle of WL. $NMOS_{12}$ is in active mode, DFSA detects the difference between BITL and BITLBAR, and the stored data is detected.



Schematic: 8 CoWD Waveform

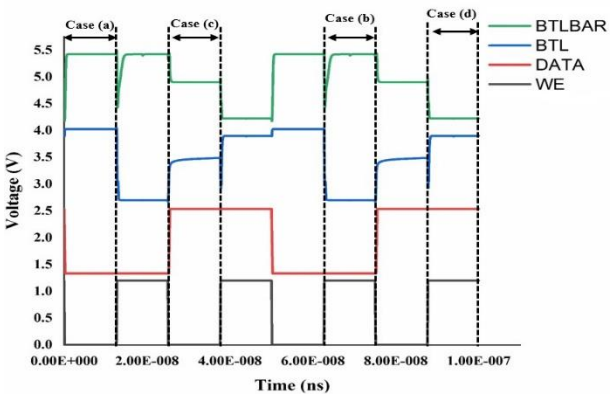
Schematic: 8 is the output waveform of CoWD, where WE and DATA are inputs, and BITL and BITLBAR are outputs described in four cases.

Case (a): $PMOS_1$, $PMOS_2$, and $PMOS_3$ = active mode, while $PMOS_4$ and $PMOS_5$ = cut-off mode, $NMOS_1$, $NMOS_2$, $NMOS_3$, and $NMOS_4$ = cut-off, while $NMOS_5$ = active mode. When WE = LOW, DATA = LOW, output pins BITLBAR = HIGH, and BITL = HIGH.

Case (b): $PMOS_2$ and $PMOS_4$ = active mode while $PMOS_1$, $PMOS_3$, and $PMOS_5$ = cut-off mode $NMOS_1$, $NMOS_3$, $NMOS_4$, and $NMOS_5$ = cut-off mode while $NMOS_2$ = active mode. When WE = HIGH, DATA = LOW, output pins BITLBAR = HIGH, and BITL = LOW.

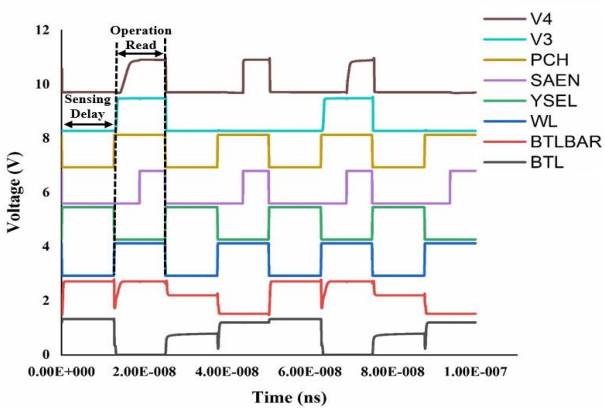
Case (c): $PMOS_1$, $PMOS_3$, and $PMOS_5$ = active mode, while $PMOS_2$ and $PMOS_4$ = cut-off mode, $NMOS_2$ = active mode, while $NMOS_1$, $NMOS_3$, $NMOS_4$, and $NMOS_5$ = cut-off mode. When WE = LOW, DATA = HIGH, output pins BITLBAR = HIGH/2, and BITL = HIGH/2.

Case (d): $PMOS_4$ and $PMOS_5$ = active mode while $PMOS_1$, $PMOS_2$, and $PMOS_3$ = cut-off mode $NMOS_1$, $NMOS_2$, $NMOS_3$, and $NMOS_4$ = active mode while $NMOS_5$ = cut-off mode. When WE = HIGH, DATA = HIGH, output pins BITLBAR = LOW, and BITL = HIGH.

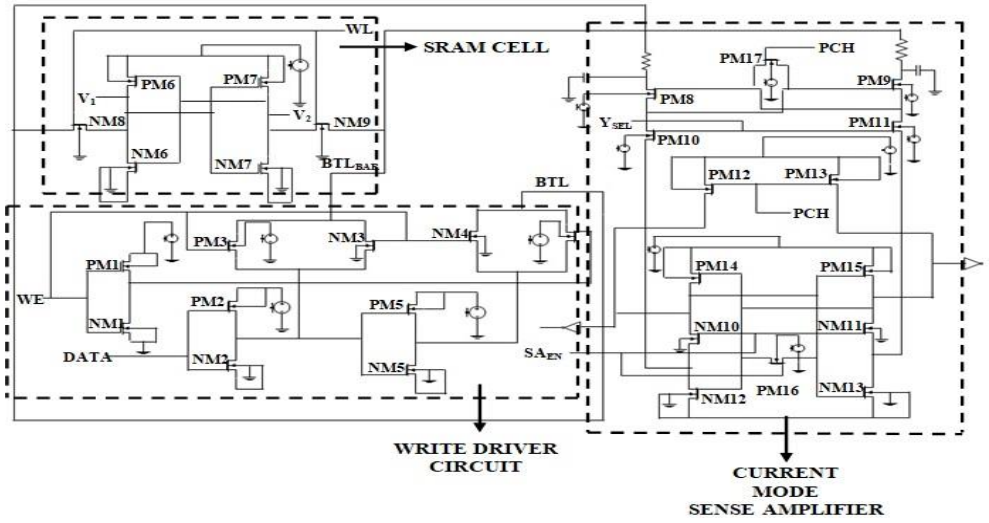


Schematic: 9 CSRAM$_C$ Waveform

The output waveform of the CSRAM$_C$ when both the write and hold operations are held is shown in the schematic: 9. PMOS$_6$ and PMOS$_7$ are pull-up transistors, and NMOS$_6$ and NMOS$_7$ are pull-down transistors, and NMOS$_8$ and NMOS$_9$ are access transistors that allow data to be stored and read by DFSA. The output waveform of a single-bit CSRAM$_C$ VDFSA architecture is shown in schematic 10.

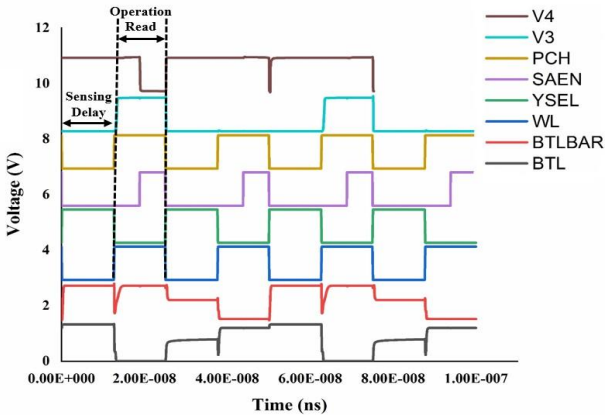


Schematic: 10 Single-bit CSRAM$_C$ VDFSA architecture output



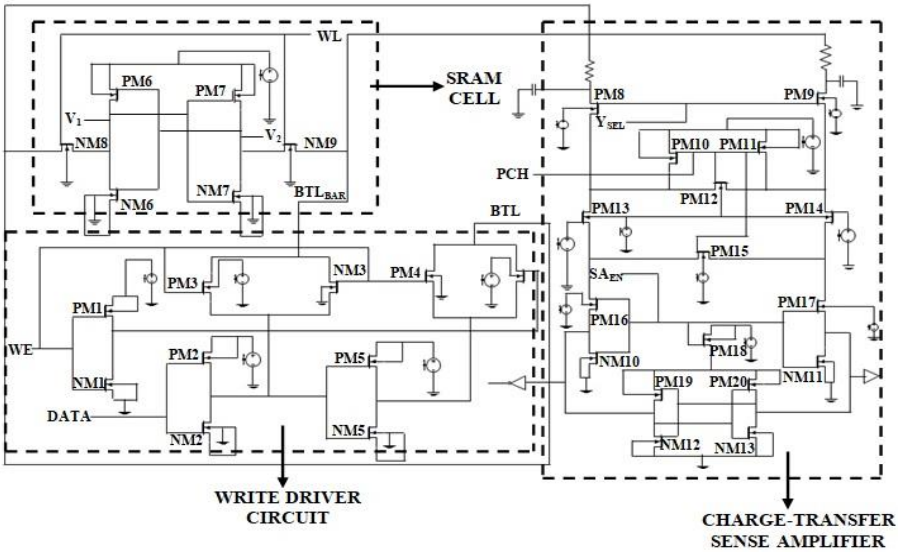
Schematic: 11 Single-Bit CSRAM$_C$ CDFSA Architecture

CoWD, $CSRAM_C$, and CDFSA are the architectural blocks for single-bit cache memory, as shown in schematic 11 [12, 13]. In schematic:12, the output waveform of a single-bit $CSRAM_C$ CDFSA architecture. The output nodes A and B, as well as the bit lines, are pre-charged. During the evaluation phase, WL = LOW, which means YSEL = LOW. PCH = HIGH to pre-charge the BITL and BITLBAR, and $PMOS_8$ and $PMOS_9$ are turned off. Data at BITL and BITLBAR in the form of current will be stopped at nodes A and B and charge the BITL and BITLBAR, which will make nodes C and D pre-discharged to LOW.



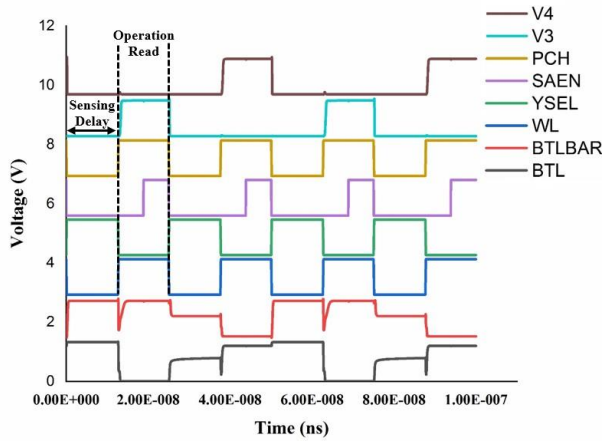
Schematic: 12 Single-bit $CSRAM_C$ CDFSA architecture output

The current on the bit-lines is passed through $PMOS_{10}$, $PMOS_{11}$ = active mode, which is stored at nodes A and B as transistors, while $PMOS_{12}$ and $PMOS_{13}$ = cut-off mode, and the current is transferred to nodes C and D through the drain of $PMOS_{10}$ and $PMOS_{11}$, WL of $CSRAM_C$ = HIGH for reading operation, i.e., access transistors are turned ON, BITL = LOW, and BITLBAR = HIGH, SAEN = HIGH (for half positive cycle of WL) at this time DFSA sense the difference between BITL and BITLBAR and the stored data has been sensed as $NMOS_{10}$ and $NMOS_{11}$ = active mode while $PMOS_{16}$ = cut-off mode due to which bias current flow through BITL and BITLBAR of DFSA while $PMOS_{16}$ keep the output equalized.



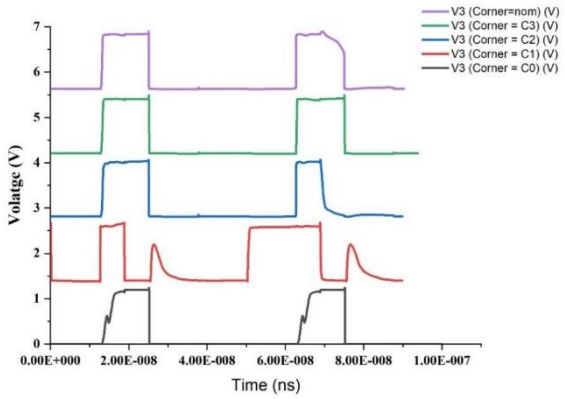
Schematic:13 Single-bit $CSRAM_C$ CTDFSA architecture

Schematic: 13 shows a single-bit $CSRAM_C$ CTDFSA architecture having CoWD, $CSRAM_C$, and CTDFSA as a sense amplifier; the working of this circuit is the same as single-bit $CSRAM_C$ VDFSA architecture and single-bit $CSRAM_C$ CDFSA architecture.



Schematic: 14 Single-bit $CSRAM_C$ CTDFSA architecture output

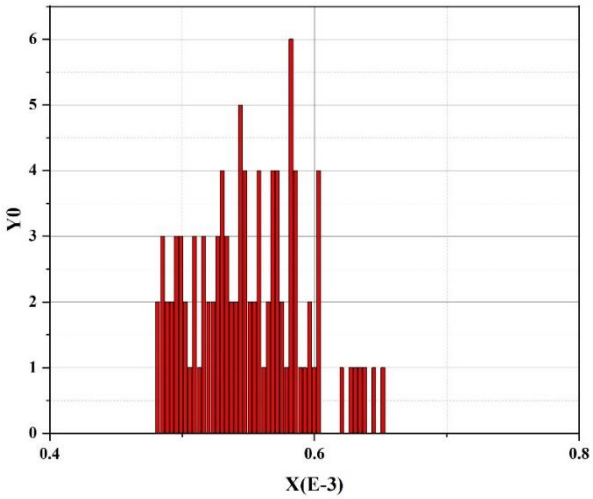
The circuit is split into two sections. $PMOS_{13}$, $PMOS_{16}$, and $NMOS_{10}$ made up the first part of the common-gate cascade $PMOS_{14}$, $PMOS_{17}$, and $NMOS_{12}$. At potential V_b, the $PMOS_{13}$ and $PMOS_{14}$ are biassed. $PMOS_{18}$, $PMOS_{19}$, $PMOS_{20}$, $NMOS_{12}$, and $NMOS_{13}$ built cross-coupled inverters to latch the output of the common-gate amplifier in the second part (A and B). DURING THE PRE-CHARGE PHASE, the BITL, BITLBAR, and all internal nodes (A, B, C, and D) = HIGH. $PMOS_8$ and $PMOS_9$ = cut-off mode, whereas $PMOS_{10}$, $PMOS_{11}$, and $PMOS_{12}$ = active, which pre-charges the BITL and BITLBAR to the HIGH. WL = LOW, indicating that no read operation is being performed. SAEN = HIGH, indicating that $PMOS_{16}$, $PMOS_{17}$, and $PMOS_{18}$ = cut-off mode while $NMOS_{10}$ and $NMOS_{11}$ = active mode, pre-charging the BITL and BITLBAR at internal nodes at E and F. YSEL = LOW during evaluation, PCH = HIGH to pre-charge the BITL and BITLBAR, and $PMOS_8$ and $PMOS_9$ = inactive. In schematic:14, the output waveform of a single-bit $CSRAM_C$ CTDFSA architecture is shown.



Schematic: 15 (a) Process Corner Variations

Schematic: 15(a) show the Process Corner Simulation of Output V_3 of SA. Five corners are shown in Schematic: 15(a). as cases are taken as; a) V_3 (Corner = C3) significant that both NMOS = SLOW, PMOS = SLOW, b) V_3 (Corner = C2) significant that NMOS is FAST, PMOS is FAST, c) V_3 (Corner

= C1) significant that NMOS = FAST, PMOS = SLOW, V_3 (Corner = C0) significant that NMOS = SLOW, PMOS = FAST, V_3 (Corner = NOMINAL) significant that both NMOS and PMOS have typical values.



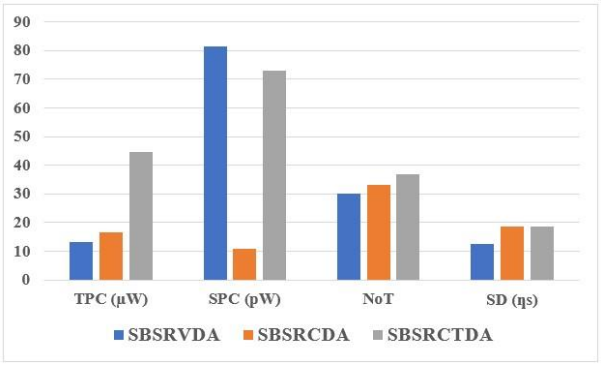
Schematic: 15 (b) Monte Carlo Simulations

In this paper, there are trade-offs between power consumption and area. Due to this region, different sense amplifiers have been analyzed to use the lowest power consumption, and different techniques are applied over $CSRAM_C$ and DFSA. Schematic: 15 (b) shows the Monte Carlo simulations of VTH _SAEN, on which the DFSA of a single-bit $CSRAM_C$ DFSA depends.

Table: 2 Various parameters of single-bit $CSRAM_C$ DFSA architecture

S.No.	Architectures	TPC (µW)	SPC (pW)	NoT	SD (ηs)
1.	**Single Bit $CSRAM_C$ VDFSA Architecture**	13.16	81.5	30	12.5
2.	**Single Bit $CSRAM_C$ CDFSA Architecture**	16.44	10.93	33	18.75
3.	**Single Bit $CSRAM_C$ CTDFSA Architecture**	44.63	72.96	37	18.75

Note: Total Power = Dynamic Power + Static Power (i.e., Total Power ≈ Dynamic Power)



Schematic: 16 Various parameters of single-bit $CSRAM_C$ DFSA architecture

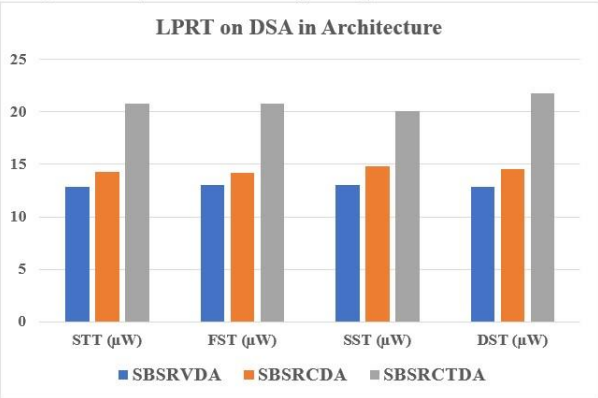
Table:2 compares sensing delay, the number of transistors, static power consumption, and total power consumption of single-bit architecture. Area increases while power decreases. Table:2 shows that using VDFSA in single-bit cache memory architecture reduces total power consumption, area, and sensing

delay. This paper focuses on total power consumption because static power consumption is in pW. Because a reduction in static power has little effect on total power, the focus is on total power consumption. Thus, power reduction techniques are used instead of leakage power reduction techniques to ensure that the design's input and output remain unchanged. Table:2 is represented graphically in the schematic: 16. In table:2 and table:3, TPC denotes total power consumption, SPC denotes static power consumption, NoT denotes the number of transistors, SD denotes sensing delay, and LPRT denotes low power reduction techniques.

In a single-bit architecture, table:2 shows how DFSA is powered down. Our circuit's working capacity increases as the total power consumption are reduced. The number of transistors increases, reducing power and increasing area, as shown in the schematic: 16, whereas the table:3 is represented graphically in the schematic: 17.

Table: 3 Analysis of TPC of single-bit CSRAM$_C$ DFSA architecture with LPRT on DFSA

S.No.	LPRT on DFSA in Architecture	STT (µW)	FST (µW)	SST (µW)	DST (µW)
1.	Single Bit CSRAM$_C$ VDFSA Architecture	12.87	13.03	13.03	12.88
2.	Single Bit CSRAM$_C$ CDFSA Architecture	14.28	14.17	14.82	14.52
3.	Single Bit CSRAM$_C$ CTDFSA Architecture	20.74	20.74	20.07	21.74

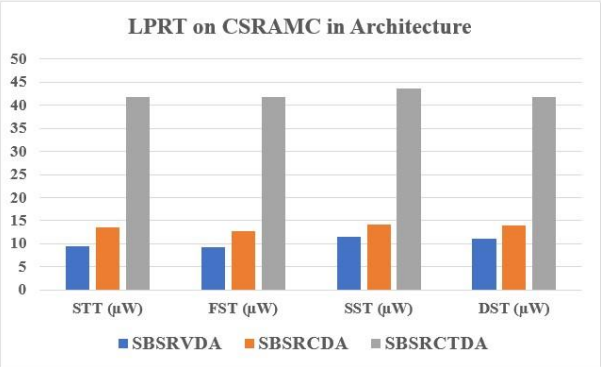


Schematic: 17 Single-bit CSRAM$_C$ DFSA architecture with LPRT on DFSA

Table: 4 Analysis of TPC of single-bit CSRAM$_C$ DFSA architecture with LPRT on CSRAM$_C$

S.No.	LPRT on CSRAM$_C$ in Architecture	STT (µW)	FST (µW)	SST (µW)	DST (µW)
1.	Single Bit CSRAM$_C$ VDFSA Architecture	9.39	9.312	11.5	11.11
2.	Single Bit CSRAM$_C$ CDFSA Architecture	13.62	12.68	14.14	13.88
3.	Single Bit CSRAM$_C$ CTDFSA Architecture	41.66	41.66	43.64	41.7

Table: 4 describes that applying LPRT over CSRAM$_C$ reduces TPC with DFSA and concludes that single-bit cache memory architecture (CSRAM$_C$ with STT using VDFSA) gives lower TPC and two transistors increases in design which increases area, i.e., ↓power consumption and ↑area.

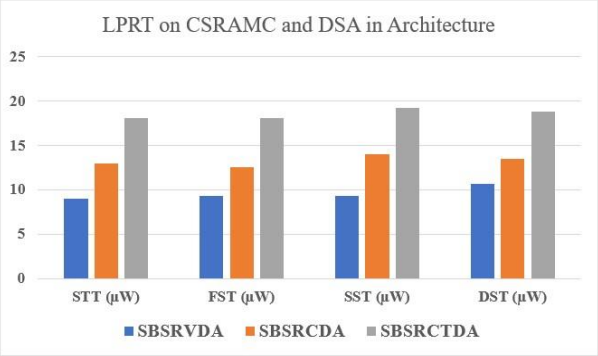


Schematic: 18 Single-bit CSRAM$_C$ DFSA architecture with LPRT on CSRAM$_C$

Table:3 and table:4 show that using VDFSA in a single-bit cache memory architecture with STT on CSRAM$_C$ and VDFSA yields the lowest TPC, as shown in table:4 and schematic:18 shows a graphical representation of table:4. Single Bit CSRAM$_C$ CTDFSA Architecture, Single Bit CSRAM$_C$ CDFSA Architecture, Single Bit CSRAM$_C$ VDFSA Architecture, LPRT stands for low power reduction technique, STT stands for sleep transistor technique, FST stands for forced stack technique, and SST stands for sleep stack technology.

Table: 5 Analysis of TPC of single-bit CSRAM$_C$ DFSA architecture with LPRT on CSRAM$_C$ and DFSA

S.No.	LPRT on CSRAM$_C$ in Architecture	STT (µW)	FST (µW)	SST (µW)	DST (µW)
1.	Single Bit CSRAM$_C$ VDFSA Architecture	8.988	9.332	9.331	10.71
2.	Single Bit CSRAM$_C$ CDFSA Architecture	12.99	12.52	14.03	13.52
3.	Single Bit CSRAM$_C$ CTDFSA Architecture	18.12	18.12	19.2	18.85



Schematic: 19 Single-bit CSRAM$_C$ DFSA architecture with LPRT on CSRAM$_C$ and DFSA

Table:5 shows that a single $CSRAM_C$ with STT VDFSA and STT architecture produces the lowest TPC, i.e., 8.988µW (a reduction of 31% in TPC). If CDFSA is used as the DFSA, then ($CSRAM_C$ and CDFSA) in a single-bit architecture with FST give the lowest TPC, i.e., reduces 23 percent TPC, and if CTDFSA is used as the DFSA in a single-bit with STT, then ($CSRAM_C$ and CTDFSA) reduces power by 59 percent, i.e., 18.12µW, whereas schematic:19 depicts the graphical representation of table 5.

5. Conclusion

With an emphasis on emerging economies, this study advances the subject of sustainable logistics by deepening our understanding of the long-term effects of green logistics methods. By explicitly differentiating between entering and departing logistics, the study provides a nuanced perspective that enables firms to better adapt their sustainability approach. This thorough analysis is essential for lawmakers and business leaders because it helps them deal with the challenging problem of reaching global sustainability standards while preserving profitability and competitiveness in a market that is changing. In the proposed work, single-bit $CSRAM_C$ DFSA architecture has been implemented with different types of DFSA, such as VDFSA, CDFSA, and CTDFSA, and compared their total power consumption, static power consumption, several transistors, and sensing delay. Furthermore, this paper also implemented CoWD, $CSRAM_{C,}$ and DFSA. Besides optimizing the power, power reduction techniques such as STT, FST, SST, and DST have been applied to different architecture blocks. Results show that SBSRVDA consumes the lowest power (8.988µW) with STT. All simulations have been done in 45nm C_{MOS} technology on the cadence virtuoso tool. Process corner simulation and Monte Carlo simulation also have been done to check the robustness of the proposed design, and there is no variation of more than three percent. This work can be extended as an array in the future.

References

[1] Abbasian, Erfan, Farzaneh Izadinasab, and Morteza Gholipour. "A reliable Low Standby Power 10T SRAM Cell with Expanded Static Noise Margins." *IEEE Transactions on Circuits and Systems I: Regular Papers* (2022).

[2] Kujur, Kanak S., Gadarapulla Rasheed, and Sriadibhatla Sridevi. "InGaAs-Si Double Pocket-Dual Gate Tunnel FET Based 7T SRAM Design." *Silicon* (2022): 1-13.

[3] Chen, Rongmei, et al. "Carbon Nanotube SRAM in 5-nm Technology Node Design, Optimization, and Performance Evaluation--Part II: CNT Interconnect Optimization." *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems* (2022).

[4] Agrawal, Reeya. "Performance Analysis of Cache Memory Architecture for Core Processor." *Control and Measurement Applications for Smart Grid*. Springer, Singapore, 2022. 479-491.

[5] Torrens, Gabriel, et al. "SRAM-Based PUF Reliability Prediction Using Cell-Imbalance Characterization in the State Space Diagram." *Electronics* 11.1 (2022): 135.

[6] Agrawal, Reeya. "Cache Memory Architecture for Core Processor." *Proceedings of International Conference on Advanced Computing Applications*. Springer, Singapore, 2022.

[7] Huang, Pei, et al. "Offset-Compensation High-Performance Sense Amplifier for Low-Voltage DRAM Based on Current Mirror and Switching Point." *IEEE Transactions on Circuits and Systems II: Express Briefs* (2022).

[8] Agrawal, Reeya. "Analysis of Cache Memory Architecture Design Using Low-Power Reduction Techniques for Microprocessors." *Recent Advances in Manufacturing, Automation, Design, and Energy Technologies*. Springer, Singapore, 2022. 495-503.

[9] Kulshrestha, Ankit, et al. "Design of High Speed and Power Efficient 16× 8 SRAM Memory Using Improved 4× 16 Decoder." *Micro and Nanoelectronics Devices, Circuits, and Systems*. Springer, Singapore, 2022. 151-160.

[10] Muthu, Bharathi Raj, et al. "Design and Analysis of Soft Error Rate in FET/CNTFET Based Radiation Hardened SRAM Cell." *Sensors* 22.1 (2022): 33.

[11] Malhotra, Akul, et al. "ADRA: Extending Digital Computing-in-Memory with Asymmetric Dual-Row-Activation." *arXiv preprint arXiv:2201.01509* (2022).

[12] Mirabella, Nunzio, et al. "An Experimental Evaluation of Resistive Defects and Different Testing Solutions in Low-Power Back-Biased SRAM Cells." *Electronics* 11.2 (2022): 203.

[13] Pal, Soumitra, et al. "A 10T Soft-Error-Immune SRAM with Multi-node Upset Recovery for Low-Power Space Applications." *IEEE Transactions on Device and Materials Reliability* (2022).

[14] B. Wicht, S. Paul and D. Schmitt-Landsiedel, "Analysis and compensation of the bitline multiplexer in SRAM current sense amplifiers," in IEEE Journal of Solid-State Circuits, vol. 36, no. 11, pp. 1745-1755, Nov. 2001, doi: 10.1109/4.962297.

[15] F. Hamzaoglu et al., "Analysis of dual-V/sub T/ SRAM cells with full-swing single-ended bit line sensing for on-chip cache," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, no. 2, pp. 91-95, April 2002, doi: 10.1109/92.994983.

[16] M. Sinha, S. Hsu, A. Alvandpour, W. Burleson, R. Krishnamurthy, and S. Borkar, "High-performance and low-voltage sense-amplifier techniques for sub-90nm SRAM," IEEE International [Systems-on-Chip] SOC Conference, 2003. Proceedings., 2003, pp. 113-116, doi: 10.1109/SOC.2003.1241474.

[17] B. Wicht, T. Nirschl and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," in IEEE Journal of Solid-State Circuits, vol. 39, no. 7, pp. 1148-1158, July 2004, doi: 10.1109/JSSC.2004.829399.

[18] Natarajan, V. Shankar, A. Maheshwari, and W. Burleson, "Sensing design issues in deep submicron CMOS SRAMs," IEEE Computer Society Annual Symposium on VLSI: New Frontiers in VLSI Design (ISVLSI'05), 2005, pp. 42-45, doi: 10.1109/ISVLSI.2005.67.

[19] S. Mukhopadhyay, H. Mahmoodi and K. Roy, "A novel high-performance and robust sense amplifier using independent gate control in sub-50-nm double-gate MOSFET," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 14, no. 2, pp. 183-192, Feb. 2006, doi: 10.1109/TVLSI.2005.863743.

[20] S. Patil, M. Wieckowski, and M. Margala, "A Self-Biased Charge-Transfer Sense Amplifier," *2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2007, pp. 3030-3033, doi: 10.1109/ISCAS.2007.377985.

[21] D. Anh-Tuan, K. Zhi-Hui, and Y. Kiat-Seng, "Hybrid-Mode SRAM Sense Amplifiers: New Approach on Transistor Sizing," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 10, pp. 986-990, Oct. 2008, doi: 10.1109/TCSII.2008.2001965.

[22] Do, Z. Kong, K. Yeo, and J. Y. S. Low, "Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 19, no. 2, pp. 196-204, Feb. 2011, doi: 10.1109/TVLSI.2009.2033110.

[23] -T. Cheng, Y. -C. Tsai and K. -H. Cheng, "A high-speed current mode sense amplifier for Spin-Torque Transfer Magnetic Random-Access Memory," *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010, pp. 181-184, doi: 10.1109/MWSCAS.2010.5548588.

[24] T. Do, S. Chen, Z. Kong, and K. S. Yeo, "A low-power CAM with efficient power and delay trade-off," *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, 2011, pp. 2573-2576, doi: 10.1109/ISCAS.2011.5938130.

[25] Do, S. Chen, Z. Kong, and K. S. Yeo, "A High-Speed Low Power CAM with a Parity Bit and Power-Gated ML Sensing," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 21, no. 1, pp. 151-156, 2012, doi: 10.1109/TVLSI.2011.2178276.

[26] Agbo, S. Khan and S. Hamdioui, "BTI impact on SRAM sense amplifier," *2013 8th IEEE Design and Test Symposium*, 2013, pp. 1-6, doi: 10.1109/IDT.2013.6727094.

[27] T. Do, C. Yin, K. Velayudhan, Z. C. Lee, K. S. Yeo, and T. T. Kim, "0.77 fJ/bit/search Content Addressable Memory Using Small Match Line Swing and Automated Background Checking Scheme for Variation Tolerance," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1487-1498, July 2014, doi: 10.1109/JSSC.2014.2316241.

[28] S. Motaman, S. Ghosh and J. P. Kulkarni, "A novel slope detection technique for robust STTRAM sensing," *2015 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2015, pp. 7-12, doi: 10.1109/ISLPED.2015.7273482.

[29] Agbo *et al*., "Quantification of Sense Amplifier Offset Voltage Degradation due to Zero-and Run-Time Variability," *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016, pp. 725-730, doi: 10.1109/ISVLSI.2016.30.

[30] D. Zhang, L. Zeng, Y. Zhang, J. O. Klein, and W. Zhao, "Reliability-Enhanced Hybrid CMOS/MTJ Logic Circuit Architecture," in *IEEE Transactions on Magnetics*, vol. 53, no. 11, pp. 1-5, Nov. 2017, Art no. 3401205, doi: 10.1109/TMAG.2017.2701407.

[31] W. Choi, K. Lee and J. Park, "Low-Cost Ternary Content Addressable Memory Using Adaptive Matchline Discharging Scheme," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1-4, doi: 10.1109/ISCAS.2018.8351461.

[32] Surkar and V. Agarwal, "Delay and Power Analysis of Current and Voltage Sense Amplifiers for SRAM at 180nm Technology," *2019 3rd International Conference on Electronics, Communication, and Aerospace Technology (ICECA)*, 2019, pp. 1371-1376, doi: 10.1109/ICECA.2019.8822122.

[33] Chen, W. Zhao, Y. Wang, and Y. Ha, "Analysis and Design of Reconschematicurable Sense Amplifier for Compute SRAM With High-Speed Compute and Normal Read Access," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 12, pp. 3503-3507, Dec. 2021, doi: 10.1109/TCSII.2021.3123512.

[34] Chen, Jian, et al. "Analysis and Design of Reconschematicurable Sense Amplifier for Compute SRAM With High-Speed Compute and Normal Read Access." *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.12 (2021): 3503-3507.

[35] Agrawal, Reeya. "Low-Power SRAM Memory Architecture for IoT Systems." *Recent Advances in Manufacturing, Automation, Design, and Energy Technologies*. Springer, Singapore, 2022. 505-512.

[36] Li, Tongde, et al. "Investigation on Transient Ionizing Radiation Effects in a 4Mb SRAM with Dual Supply Voltages." *IEEE Transactions on Nuclear Science* (2022).

[37] Abbasi, Alireza, et al. "A novel design of high performance and robust ultra-low power SRAM cell based on memcapacitor." *Nanotechnology* 33.16 (2022): 165202.

[38] Saha, Rajesh, Yogendra Pratap Pundir, and Pankaj Kumar Pal. "Comparative Analysis of STT and SOT based MRAMs for Last Level Caches." *Journal of Magnetism and Magnetic Materials* (2022): 169161.

[39] Kumar, Abhishek, Abhishek Sahu, and Shree Prakash Tiwari. "Design and Performance Evaluation of 1 KB SRAM in SCL 180 nm Technology." *Micro and Nanoelectronics Devices, Circuits, and Systems*. Springer, Singapore, 2022. 491-501.

[40] Mathur, R. et al. "Buried Interconnect for Sub-5 nm SRAM Design." *IEEE Transactions on Electron Devices* (2022).

[41] Su, Yuqi, Hyunjoon Kim, and Bongjin Kim. "CIM-Spin: A Scalable CMOS Annealing Processor With Digital In-Memory Spin Operators and Register Spins for Combinatorial Optimization Problems." *IEEE Journal of Solid-State Circuits* (2022).

[42] Vijayavelu, S. S., et al. "Design and Analysis of LK Model Based FEFET Memories." *Proceedings of International Conference on Power Electronics and Renewable Energy Systems*. Springer, Singapore, 2022.

[43] Yang, Zhi, et al. "A Novel Computing-in-Memory Platform Based on Hybrid Spintronic/CMOS Memory." *IEEE Transactions on Electron Devices* (2022).

[44] Rawat, Bhawna, and Poornima Mittal. "A reliable and Temperature Variation Tolerant 7T SRAM Cell with Single Bitline Conschematicuration for Low Voltage Application." *Circuits, Systems, and Signal Processing* (2022): 1-23.

[45] Spetalnick, Samuel, and Arijit Raychowdhury. "A Practical Design-Space Analysis of Compute-in-Memory With SRAM." IEEE Transactions on Circuits and Systems I: Regular Papers (2022).