Communications on Applied Nonlinear Analysis
ISSN: 1074-133X
Vol 32 No. 5s (2025)

Analysis of Energy Efficient Differential Fault Tolerant Adders with Minimized Nonlinearities

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Article History:

Received: *02-10-2024*

Revised: *23-11-2024*

Accepted: *02-12-2024*

Abstract:

In this paper, two 1-bit Differential fault tolerant Full Adder circuits (1b-FA)proposed focusing on reducing nonlinearities to improve performance and reliability in modern electronic systems, using Carbon Nano FETs (CNFETs).Transmission gate logic and pass transistor logic is being used in proposed adders to improve energy and fault tolerant characteristics of Full Adder. Fault detection and fault correction mechanisms are proposed in outputs of 1-bit differential full adder. The proposed fault detection can detect only single error and proposed error correction can correct it. By using Cadence Virtuoso tool, the proposed design is simulated with 32 nm CNFET technology at a supply voltage (VDD) of + 0.9V. The performance of proposed full adder designs has been comparedwithexisting designs in terms of power, delay and power-delay product (PDP). The proposed full adders supply voltage is being varied over a range and can observe the characteristics of full adder with respect to variations in supply voltage (VDD).

Keywords: Differential, CNFET, Fault Tolerant, Single error

1.Introduction

Fault Tolerant design[1-3] is vital for real time applications. This design is must for critical applications like space, defence and medical. Fault's presence in these systems can alter the functionality and which sometimes results worse condition. So, fault tolerant design is necessary for critical applications. The faults in the design are being caused due to technology advance in transistor size and high dense designs.

Adder[5-10] is the fundamental design in VLSI. Addition is the primary operation in arithmetic operationsand memory address calculations of Processors. If the adder performance [11-18] is better, this can improve the overall processor performance. Hence, researchers work on improving performance of adders by reducing the number of transistors, scaling down of transistor size and by varying device technologies[19-28].

Due to the scaling down of transistor size, there seen a change in performance parameters like speed of the device, area and power consumption. This in turn became a short come and because of this it facing non-linearities like short channel effects (SCE), Drain Induced Barrier Lowering (DIBL) and losing handleable on gate etc., These nonlinear effects can be result in malfunctioning of the device and which cannot be considered as a good design. To get benefit from scaling down of transistor, researchers were moved further to improve the device technology of transistor. In this process few device technologies like Carbon Nano Tube (CNT) Fin shaped FET (FinFET) and Gate All Around FET(GAAFET) etc., came as alternatives for MOSFET[29-30].

When compared with other device technologies CNT shows better performance requirements of low power, high speed and low area with minimal non-linearities. The scaling of CNT is flexible and hence it provides high density. The heat dissipation of CNT is better when compared to other technologies. Because of these characteristics for scaling down of transistor CNT is more preferable.

2.CNFET

The primary choice of opting CNTis carbon being profuse availability on earth and space and its raw material is cost effective. The electrical characteristics like top conductance and minimal resistancemark it as preferable.

The secondarychoice exhibiting nano and sub-nano fabrication capabilities. Graphite which is an isotope of carbon can also use as alternative for the fabrication of FETs. The s Fig.1exhibits the forms of chirality when the carbon tube is rolled. Chirality of CNT isclassified into 3, namely, Armchair, Zigzag and Chiral.[29]

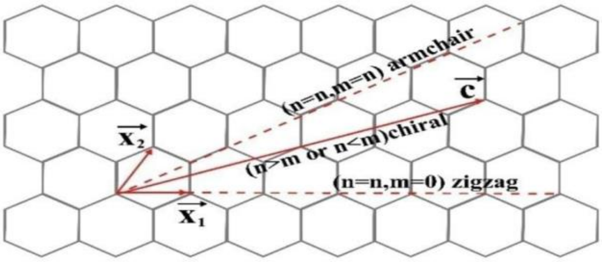

Fig.1 Various Chirality of CNT tube

Mathematically, the Chirality vector (C) is represented as

$$C = n X 1 + m X 2 \quad (1)$$

Threshold voltage of CNFET is represented as

$$V th \cong E bg / 2 e \cong 0 .436 / D CNT (nm) \quad (2)$$

And the diameter (DCNT) of CNFET is expressed as

$$DCNT = 0 .0783 \sqrt{n^2 + m^2 + nm} \quad (3)$$

Section 3 of the paper discuss the existing 1-bit full adder using CNFETs and their fault tolerant circuit design. Section 4 discuss the proposed differential 1-bit full adder using TG and PTL logic. Section 5 gives the simulation results, comparative details and at the end section 6 gives conclusion.

3.Existing Full Adder Circuit Designs and Fault Tolerant Circuit Design

The existing full adder design [4] consists of 14 transistors and has 3 transistors of delay in the critical data path. At the sum and carry outputs it has pass transistor logic, because of this the circuit provides non full output swing and having drawback of driving capability. It provides single output of sum and carry.

In the case of existing full adder design [5] consists of 12 transistors and has 3 transistors of delay in critical data path. It has pass transistor logic at sum output, due to this the existing full adder [5] having a problem of driving capability. It provides single output of sum and carry. Both the existing full adders uses Fault detection Full Adder circuit for fault detection.

This paper demonstrates the improvement in circuit performance by having differential outputs for sum and carry. Because of getting differential outputs from the full adder design, the performance of fault detection shows improvement in delay, power consumption and power-delay-product. In the proposed full adder design, care has been taken to improve driving capability of the design and to improve the circuit performance of fault tolerant design.

4.Proposed Design

4.1 Proposed CNFET Based Differential 1-Bit Full Adder Design with TG

The proposed 1-bit differential full adder design with TG as shown in fig 2. It is a transmission gate which has 3 stages. The circuit consists of 2 transmission gates in between having back-to-back connected inverters. The first stage gives XOR/XNOR signal pair. This XOR/XNOR signal is used as a control signal for remaining 2 stages of TG's. The output of second stage gives a pair of Sum and Sum bar. The output of third stage gives a pair of Carry and Carrybar.Since the full adder is differential it gives true and complementary outputs. This differential full adder uses 24 transistors.

For input B, based on the control signal input A, B bar is propagated to XNOR and XOR signal holds the complement of XNOR. This XOR/XNOR signal pair now act as control signal for remaining TG's. Based on XOR/XNOR signal pair c bar is propagated to Sbar and S is the complement of S bar. Based on XOR/XNOR signal pair either C or A bar is propagated and Cout bar and Cout are generated.

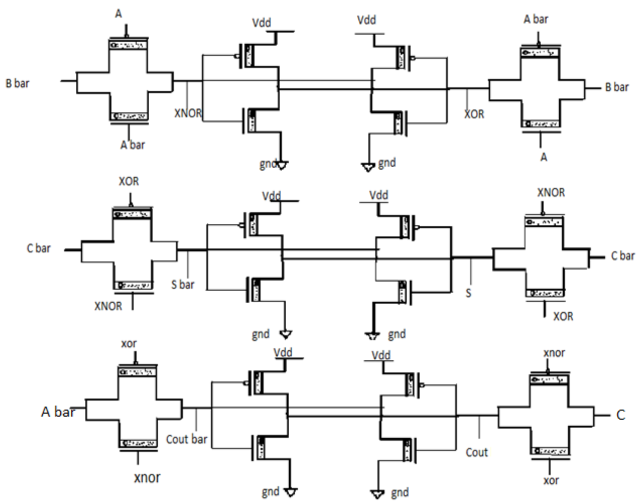

Fig 2.Schematic of Proposed CNFET Based Differential Full Adder Design with TG.

4.2 Proposed CNFET Based Differential 1-Bit Full Adder Design with PTL

The proposed 1-bit differential full adder design with PTL as shown in fig 3. It is a pass transmission logic gate which has 3 stages. The circuit consists of 2 pass transmission logic gates in between having back-to-back connected inverters. The first stage gives XOR/XNOR signal pair. This XOR/XNOR signal is used as a control signal for remaining 2 stages of PTL's. The output of second stage gives a pair of Sum and Sum bar. The output of third stage gives a pair of Carry and Carry bar. Since the full adder is differential, it gives true and complementary outputs. This differential full adder uses 18 transistors.

For input B, based on the control signal input A, B bar is propagated to XNOR and XOR signal holds the complement of XNOR. This XOR/XNOR, signal pair now act as control signal for remaining PTL's. Based on XOR/XNOR signal pair cbar is propagated to Sbar and S is the complement of Sbar. Based on XOR/XNOR signal pair either C or A bar is propagated and Cout bar and Cout are generated.

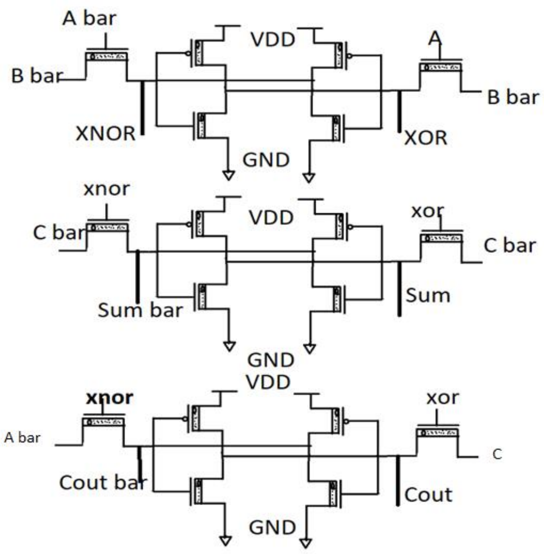

Fig 3. Schematic of Proposed CNFET Based Differential Full Adder Design with PTL.

For the proposed differential full adders performance parameters like power, speed and power delay product (PDP) are analysed.

The differential outputs i.e., Sum and Sum bar Carry and Carry bar of 1-bit full adder design are given to 2 single rail checkers. For one of the single rail checker inputs were Sum and Sum bar and to the other Carry and Carry bar were inputs. For the input combination of (1,1 and 0,0) of Sum and Sum bar the output of single rail checker is '1' which indicates faulty of the circuit and for the input combination of (0,1 and1,0) of Sum and Sum bar the output of single rail checker is '0' which indicates fault free. Similarly, based on the input combination of Carry and Carry bar either faulty or fault free is identified. Hence, by using single rail checkers, fault is detected.

Fig 4. shows the block diagram of single fault detection, where single rail checker is XOR gate.

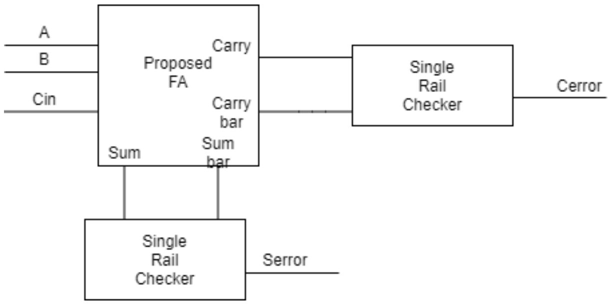

Fig4. Block Diagram of Proposed Single Error Detection

If the fault site is identified, then the Single Error Detection uses a correction design which is Fault Correction Adder (FCA) for the recovery. With this correction design the proposed full adder design can be marked as a Fault Tolerant design.

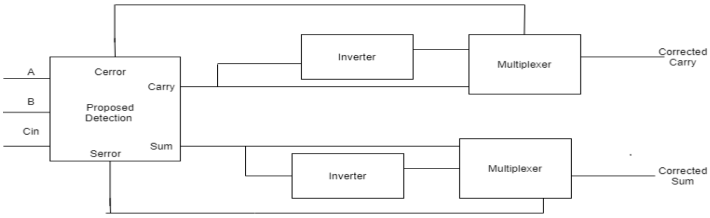

Fig5. Block Diagram of Proposed Fault Correction Adder

The mechanism of this design is as follows: If a faulty output is generated which is either Cerror is ‘0’ or Serror is ‘0, then the output Sum and Carry of full adder are transmitted through an inverter and this inverted signal is multiplexed to get Corrected Sum or Carry. For a fault free output, the Sum and Carry of full adder are as it is multiplexed for the Corrected Sum and Carry. The error signal from single error detection act as a selection signal for multiplexer, based on the selection signal either inverted Sum and Carry or non-inverted Sum and Carry are passed through multiplexer.

5.Simulation Results & Comparison

The simulation is carried out using the Cadence Virtuoso Tool. The circuit is designed with 32nm technology of 0.9 volts as supply voltage(Vdd). The waveform of the TG and PTL differential full adder circuit of inputs(A, B and C) and outputs(Sum, Sum bar, Carry and Carry bar) are shown in Fig.6 & 7.

For the proposed TG and PTL differential full adder circuit the supply voltage Vdd was altered in the range of 0.5 V to 1V and has observed circuit performances. This has tabulated in table 1.

The comparison results of existing 1-bit full adderswith proposed1-bit differential full adders are tabulated in table 2.

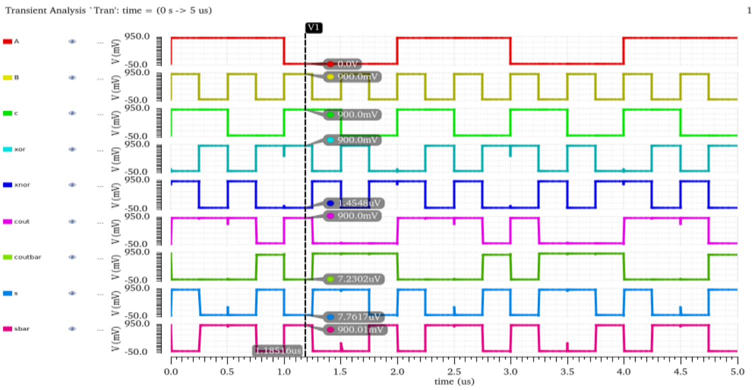

Fig6.Waveform of Proposed TG Differential Full Adder Using CNFET

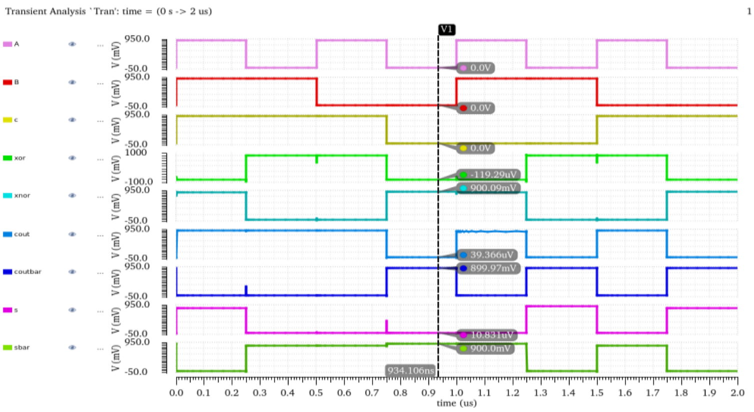

Fig7.Waveform of Proposed PTL Differential Full Adder Using CNFET

Table1: Comparison of Proposed 1-Bit FA Designs in Terms of Variation in VDD Supply

VDD Supply	Proposed with TG			Proposed with PTL		
	Power(watts)	Delay(ps)	PDP(J)	Power(watts)	Delay(ps)	PDP(J)
0.5	298.2p	47.45	14.149e-21	29.13e-9	19.99	582.3e-21
0.6	346.8p	26.22	9.094e-21	36.68e-9	15.765	578.26e-21
0.7	407.2p	18.77	7.643e-21	94.42e-9	14.06	1.327e-18
0.8	478.2p	13.87	6.632e-21	716.8e-9	11.98	8.587e-18
0.9	555.9p	11.63	6.465e-21	2.442e-6	10.086	24.63e-18
1.0	817.7p	10.298	8.42e-21	5.274e-6	8.783	46.32e-18

Table 2: Comparison of Existing and Proposed 1-Bit FA Design

Performance Parameters	Existing [4]	Existing [5]	Proposed with TG	Proposed with PTL
Transistor Count	14	12	24	18
Output Swing	NFS	NFS	FS	FS
No.of.outputs	Single	Single	Differential	Differential
Power(watts)	398.5p	388.7p	555.9p	2.442u
Delay(ps)	1.728	1.724	11.63	10.0
PDP(J)	0.687e-21	0.671e-21	6.465e-21	24.42e-18

Table 3 gives the comparison of existing and proposed full adders fault detection performance. Fig 8,9 gives the fault free and faulty of proposed full adder with TG and Fig 10,11 gives the fault free and faulty of proposed full adder with PTL.

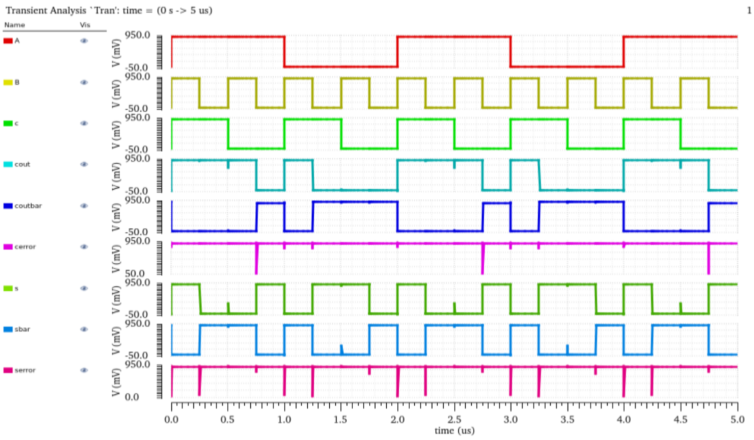

Fig8. Waveform of Fault Free Single Error Detection of Proposed with TG

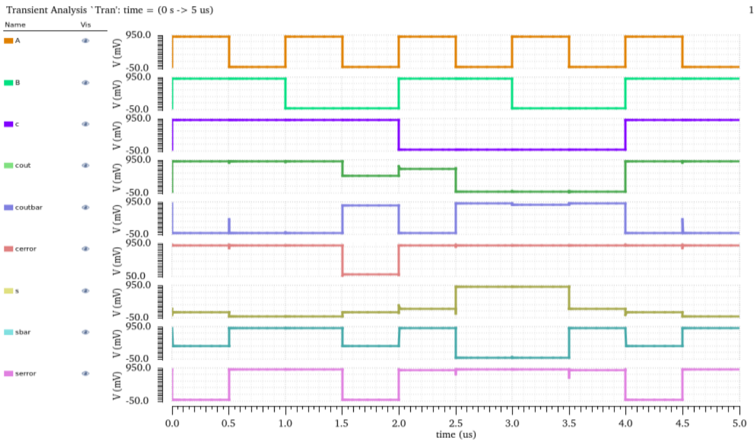

Fig9. Waveform of Faulty Single Error Detection of Proposed with TG

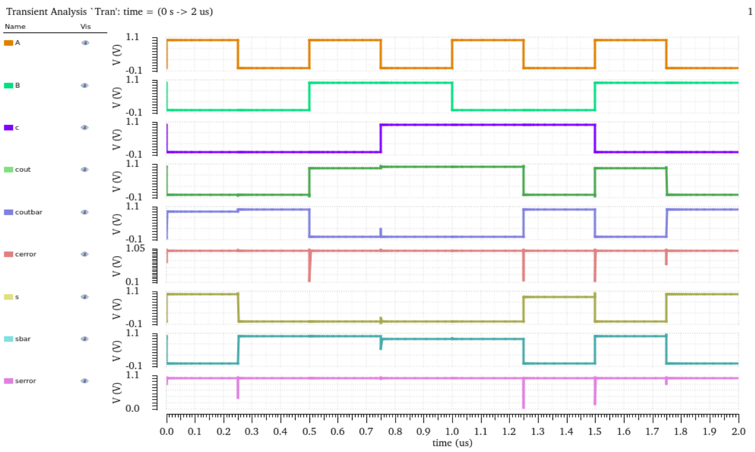

Fig10. Waveform of Fault Free Single Error Detection of Proposed with PTL

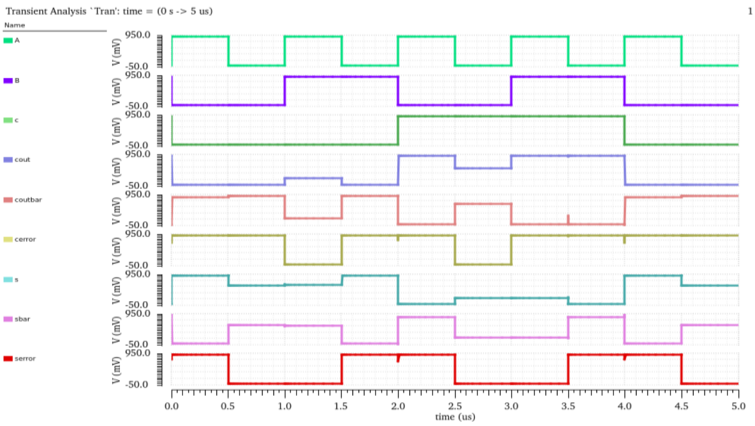

Fig11. Waveform of Faulty Single Error Detection of Proposed with PTL

Table 3: Comparison ofexisting and proposed Single Error Detection FA Design

Performance Parameters	Existing [4]	Existing [5]	Proposed with TG	Proposed with PTL
Transistor Count	50	48	30	24
Power(watts)	24.6u	24.35u	10.57u	12.78u
Delay(ps)	5.817	5.605	10.77	12.09
PDP(J)	143.1e-18	136.4e-18	113.8e-18	154.4e-18

6.Conclusion

In this paper, we have proposed two Differential Full Adders circuit based on CNFET, Single Error Detection circuit using CNFET, and Fault Correction using CNFET. The proposed Single Error Detection circuit using CNFET is optimized to consume less power, having lesser PDP and that to with less than the average number of transistors when compared with other existing designs.By addressing both energy efficiency and fault tolerance, these adders are optimized for high-performance applications, ensuring robust operation even in the presence of faults or noise.

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