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Design and Analysis of High Speed Low Power 4T-2R finFET-Memristor based SRAM

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Abstract:

Power usage management has emerged as a significant challenge in the production process due to the continued miniaturisation of CMOS technology. All standards for developing designs of non-volatile storage are going to gain through the implementation of memristors. Memristive devices have been defined by non-volatility, significant switching frequency, minimal energy consumption, and small dimensions. FinFETs may replace conventional transistors, significantly enhancing efficiency in space and power, hence improving the design. The development of a non-volatile SRAM unit using FinFET and Memristor is suggested and compared to conventional SRAMs. Compared to current CMOS 6T SRAM and finFET 6T SRAM, the proposed SRAM exhibits significantly reduced power consumption and demonstrates speed improvements of at least 87% and 54%, respectively. Furthermore, Monte Carlo calculations have been conducted for the described 6T-SRAM architecture to enhance comprehension of the device's robustness.

Keywords: SRAM, Memristor, finFET.

1. Introduction

In the last few years, metal oxide-dependent memories, including DRAM, SRAM, along with flash memory, are primarily employed to satisfy the capacity requirements of data processing units [1]. The proliferation of handheld electronics has necessitated the design of storage systems with rapid switching capabilities and extended battery life . Although SRAM remains fast, its volatile characteristics might result in data loss upon power supply removal. Furthermore, during the extremely deep submicron region, SRAM cells have significant leakage power usage [2,3]. CMOS technology has approached the basic limits of size scalability considering the enhanced short-channel impact, which significantly undermines device efficiency.

With the rise in integration along with operational speeds, power dissipation has emerged as a significant concern. In the past few years, low-power integrated circuit design has garnered interest owing to the growth of rechargeable products. The predominant technique for decreasing system power usage within memory development aims to minimise transistor dimensions. Developers of Field Effect Transistor (FET) dependent scalable CMOS devices have been making all efforts to facilitate this reduction [4,5]. As technology evolves beyond 90 nm nodes into sub-nanometers, leakage becomes a major issue. After MOS devices encountered scaling limits, the semiconductor industry launched the FinFET, the main next-generation semiconductor. Many semiconductor firms invest in FinFET technology to support Moore's Law. FinFETs have an undoped or mildly doped totally depleted silicon sheet (body).

SRAM can be utilised as a part of memories because of its enhanced operational speed and superior functionality. Using SRAM, data retention is crucial as data is lost whenever power has been

discontinued. Traditional SRAM structures, such as the primary memories or cache, have significantly prolonged starting times due to their unreliability. Nonvolatile storage may reduce startup duration and consumption of energy. A CMOS Memristor-based SRAM cell might serve as an efficient circuit component, enabling ordinary memory cells to retain data even when power is removed[6,7].

The memristor had been found by Leon Chua during the beginning of the 1970s, establishing the relationship between magnetic flux (Φm) and electric charge (q), and capable of retaining its resistive condition regardless of when the power source is removed. The internal state of the variable (xm) functions as the memristance (M) for the memristors, that is, $x_m \equiv M$ [8]. The condition associated with the memristor can be determined by the subsequent formula.

$i(t) = x_m - (v(t))$ ……..1

The memristor comprises a two-terminal device, once regarded as the subsequent passive component following the inductor (L), capacitor (C), as well as resistor (R) [9]. The memristor employs a non-linear switch method which facilitates the formation of conductivity filaments via oxide layers that are situated across metal terminals, therefore attaining both low-resistance along with high-resistance states of the component . The magnitudes associated with various resistance levels might vary. The supplied external voltage dictates the resistance levels of the component. Furthermore, the employing of memristors has been shown to result in reduced power consumption and increased package density. Memristors have applications in several domains, including the development of chaotic circuitry [10,11], analogue circuits [12], logic arrays [13], along with flip-flops [14].

A research group at UC Berkeley designed FinFET to define quasi dual-gated transistors on a silicon-on-insulator substrate. Given the growing interconnection, FinFET technology has evolved. Moore's Law states that the number of transistors in a silicon area doubles every two years. The attractiveness of FinFETs arises from their reduced leakage current, improved efficiency, and diverse implementation methodologies, notably the incorporation of Tunnel FETs along with Junctionless Tunnel FETs throughout SRAM design as documented in the research literature [15,16]. As stated by Moore's rule, scaling down enhances integrating density upon the chip and facilitates the mitigation associated with the short channel impacts. The minimal power usage of FinFETs facilitates substantial integration levels due to their reduced threshold voltage, allowing them to operate at lower voltages. The reduced threshold enables their functioning at a pace 30 percent faster compared non-FinFET devices. The FinFET has been defined because of its conductivity channel, composed of silicon referred to as the "fin," that serves as the device's body.

Figure 1 illustrates a conventional FinFET architecture. The functional channel width (electrical width) Weff associated with a single-fin FinFET, as per the design, must be double the fin height [17]. The use of several fins allows an increased device width. Increasing the fin height and therefore the channel width could improve the driving current within the FinFET. The construction of several parallel fins yields greater driving current densities per unit area.

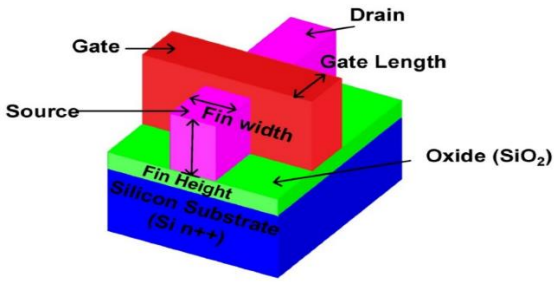

Figure 1. 3D representation of Silicon substrate-dependent FinFET. [17]

A new SRAM with higher energy efficiency, noise immunity, and lower writing and reading latency than the typical 6T SRAM cell design is proposed in this study. This paper highlights the benefits of symmetric SRAM, including improved idle power utilisation and static noise margin compared to standard 6T SRAM cells. Additionally, using a memristor ensures non-volatility. This article covers the following topics: Section 2 discussexisting literature. Section 3 details the suggested symmetric SRAM cell architecture's functioning in multiple operating modes. Section 4 compares simulation results to contemporary CMOS 6T SRAM memory cells and the recommended cell. The conclusion is derived in section 5.

2. Literature Survey:

Figure 2 illustrates the 8T2R-dependent NVSRAM. RRAMs were accessible by applying a CTRL1 command to two devices, M7 & M8, that facilitate the SET and RESET operations, correspondingly [18]. Upon receipt of the SET command, CTRL1 gets switched to a higher state, whereas CTRL2 remains grounded. SRAM cell data indicates that R1 or R2 is set for low-level reading and writing. CTRL2 is VDD during RESET, whereas R1 or R2 is HRS depending on SRAM cell data. The F-MOSFET's driving performance has been improved for NVSRAM applications, although writing and power-down phases increase power consumption.

Figure 3 shows the 7T1R SRAM cell design [19]. The transistor cell has 7 devices and a single RRAM with six TSRAM cells and one T1R. The STORE operation is controlled by transistor M7 in the RRAM device and memory node Q, which stores "0" and "1". Due to a single RRAM device, the BL starts the FORMING phase at storage start.The power-down phase disables all voltage sources. Depending on resistivity, CTRL2's current passes the RRAM unit during RESTORE. The RRAM's Low Resistance State (LRS) keeps Q at "1," and Qb discharges via M2. When CTRL1 and WL are high during READ, the voltage differential between the RRAM devices' upper and lower terminals determines current flow. Node Q checks the storage cell's status using BL. This design reduces energy consumption and can save and execute numerous FPGA configurations.

Figure 4 shows 7T2R [20] with RRAMs R1 and R2. R1 is connected to M7, whereas R2 relates to M3 and M4's shared beginnings. The M5 controls STORE/RESTORE. One BL will produce R1. If the CTRL1 signal stays high, RRAM resistance switches between LRS and HRS and LRS during STORE operation, depending on Q and Qb node voltages. WL and CTRL1 stay increased while reading. Nodes Q encode "0" and "1" writing commands. BL rises to SET R1 during STORE and falls to RESET. The RRAM device keeps "1" at Node Q during RESTORE in LRS mode and "0" in HRS mode. While stability was improved, energy loss increased tenfold with every 100 K temperature rise in this model.

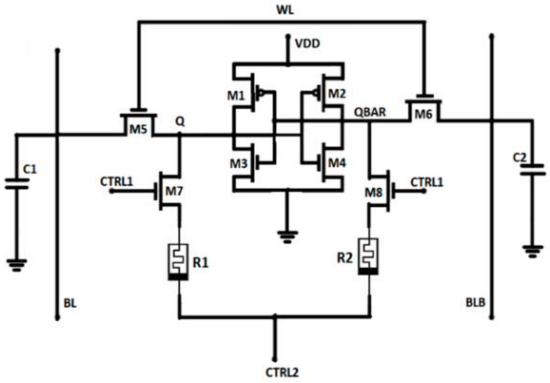

Figure 2: Existing 8T2R Mermistor based SRAM [18]

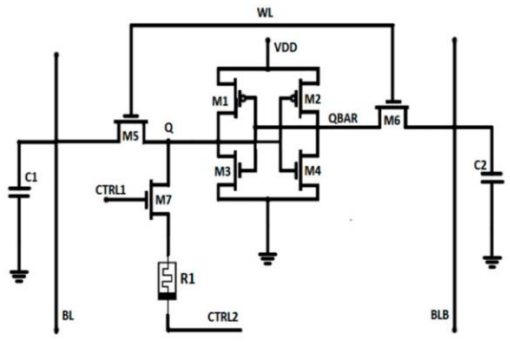

Figure 3: Existing 7T2R Mermistor based SRAM [19]

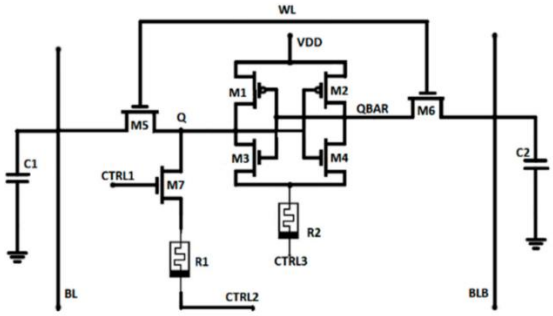

Figure 4: Existing 7T2R Mermistor based SRAM[20]

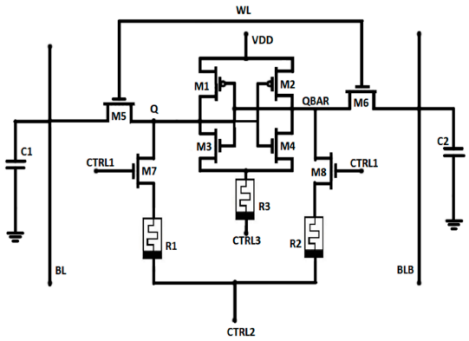

Figure 5: Existing 7T2R Mermistor based SRAM[21]

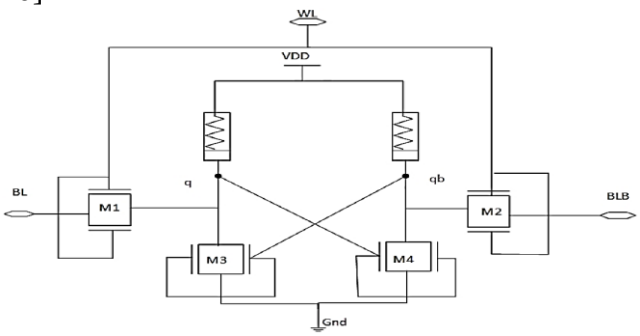

Figure 6: Existing 7T2R Mermistor based SRAM[22]

Figure 5 depicts a symmetric 8T3R NVSRAM cell[21]. A memristor component stores data in its resistance state, making RRAM non-volatile. This cell retains data after power-off and has fast power-on/power-off. The proposed symmetric 8T3R NVSRAM cell outperforms existing NVSRAMs in instant-on performance across technology levels. Simulations show that the RAM-based 8T3R SRAM cell consumes less power in sleep mode and switches more efficiently during power on/off transitions. Its reading and writing stability and noise tolerance are better than ordinary asymmetric 6T SRAM with extra NVSRAM cells. Multiple technology nodes have assessed power dissipation.

Figure 6 depicts a symmetric SRAM cell [22].Silicon substrate-dependent FinFET and Metal Insulator Metal (MIM) Memristor are used to construct a non-volatile SRAM cell and compare it to traditional SRAMs. Power consumption of the hybrid architecture is 91.8% higher than the Silicon substrate FinFET design. Proposed design latency is 1.989 ps, considerably shorter. The inclusion of high-K insulation at the metal area interface makes the recommended architecture more realistic for a low-power, high-speed memory system. To further understand device stability, Monte Carlo (MC) simulations were performed on the published 6T-SRAM designs.

3. Proposed Memristor based SRAM

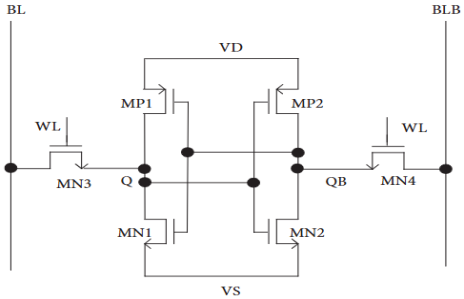

Figure 7: A traditional 6T SRAM

SRAM storage cells are mostly made up of SRAM along with non-volatile units. SRAM functions according to the conventional 6T SRAM architecture, as seen in Figure 7. Together, the transistors MP1 & MN1 develop a left side inverter, whereas the transistors MP2 & MN2 constitute a right side inverter. For the purpose of data storage, both of these inverters remain cross-coupled. There are two types of access transistors known as MN3 & MN4. Accessing transistors have been employed to establish connections between the storage nodes Q & QB, both of which are respectively linked to BL & BLB. The gate controlled signal for accessing transistors has been designated by the symbol WL. Memory is capable of being accessed and written to whenever the WL has been turned on while it is active.The 7T1R & 8T2R components make up the majority of the preceding SRAM memory cell. For the purpose of preventing the loss of data within the event that the system fails, the data are immediately saved in RRAM.

Figure 8 illustrates the recommended 4T2R SRAM cell. It comprises 2 memristors along with 4 transistors, with NM2 & NM3 functioning as accessing transistors that link the bit lines to both the Q & Qb nodes. Two memristors function as storage elements. The configuration allows for parallel connection with the opposite orientation throughout the writing cycle, however throughout the reading cycle, the connection switches to series. A typical version has an inverter containing NMOS transistors, which have a memristor connected to the drain terminals of the respective transistors (NM1 & NM0). Consequently, the architecture becomes 2R-4T, that will exhibit reduced area as well as power usage.

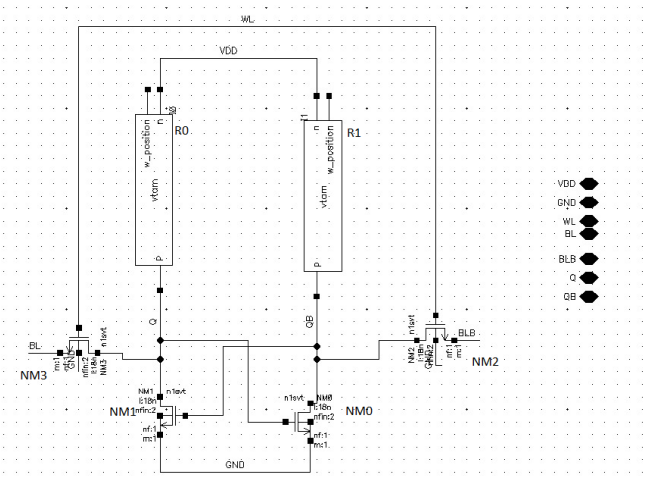

Figure 8: Proposed 4T2R SRAM Cell

SRAM cells operate in three forms: Writing, reading , and holding modes. In Writing mode, the SRAM cell might receive additional bit values instead of the original. When powered, the SRAM unit can store or maintain data forever. In "Reading" mode, an SRAM cell may communicate its data. The holdmode does not change the data.

The SRAM circuitry operates effectively using CMOS logic; nonetheless, it consumes substantial power and requires considerable space. Figure 8 illustrates the use of a FinFET along with Memristor to facilitate the realisation of a 6T-SRAM circuit, aimed at minimising power consumption and spatial dimension. Inverters employing cross-coupled FINFET as well as memristor technology have been employed to construct the memory circuitry. Static CMOS accessing transistors have been substituted with FinFET technological advancement.

Throughout pre-charging onto VDD, both the Bit Lines have been set higher for the reading activity. When the pull-down fin device turns on, the resultant bit on the node of “Inverter 1,” designed with a Memristor, will be set as “0.” Subsequently, whenever the bit line (BL) discharges from the supply

voltage (VDD), the differential bit- line sensing amplifier activates. FinFET-memristor-dependent storage cells can additionally be set for writing operations. Two FinFETs, NM2 & NM3, may perform this based on the storage cell's bit that needs to be written. Applying VDD to BL will record a bit "1" within the cell. This is accomplished by setting NM2's gate controlled input (WL) to a higher state. When the initial input BL becomes higher, the FinFET (NM2) result (Q) stabilises at "1" and QB at "0". Concurrent writing enabled line and increased WL activation starts this. Disengaging the BLB line at 0 V feeds "0" into the specific SRAM cell. This causes WL to disconnect both Memristor inverters, allowing node Q to store "0" with the extra accessing FinFET (NM3).

4. Simulation Results:

The rest of this part presents the findings of the recommended SRAM design, including the following sections that examine the study of SRAM in connection with a variety of factors.

The necessities for a suggested SRAM memory component has been formulated, and the 18nm production process of Cadence Virtuoso facilitated the computed outcomes. The presented SRAM cell was compared to comparable designs employing an 18 nm manufacturing node. The power utilisation delay, process fluctuation sensitivity, parameters, and stability features were evaluated. 0.7 V maintains room temperature at 27 °C.

Table 1 presents the frequently used computational attributes. The study covers process characteristics such temperature swings from -50 °C to 75 °C and supply voltage variations from 0.6 to 0.9 V. The next sections compared the proposed SRAM module's operational properties to current ones. The transient simulation research waveforms for writing and reading are shown in Figures 9 and 10.

Table 2: Simulation Set-up

Parameter to be set	Corresponding Value
Transistor used	finFET
Technology (nm)	45
Transistor Sizes	2/1
Temperature (^{0}C)	27

Power Utilization

This section evaluates and examines the power consumption of the proposed design for both writing and reading, in comparison to current SRAMs. Due to bit-line capacitance throughout the process of reading and writing, dynamic power accounts for a large portion of power consumption.

Consequently, as seen in equation (1), it may be used in the calculation of dynamic power.

$$P_{dyn} = \propto_{BL} C_{effective} V_{DD}^2 f_{write/read} \quad (1)$$

$\propto_{BL}$ – bitline switching activity

$\propto_{BL}$ shows the bit-line's switching frequency and the probability of its changing throughout a clock period.

$C_{effective}$ The capacitance efficiency within the SRAM

Assessing capacitance necessitates consideration of the length and quantity of the connections to the bit-line. Subsequently, the unit capacitance for each connection must be applied.

$f_{write/read}$ −Frequency of reading or writing operations

$V_{DD} - supply\ voltage$

Delay:

Reading delay serves as a metric employed to assess the reading performance of SRAM cells. The reading-delay represents the interval between 50% excitation of the word line (WL) as well as a 10% variation within the pre-charged value of the bit line.
Write access time (TWA), also known as write delay, measures how fast an SRAM can transmit data within its storage node during a write operation.

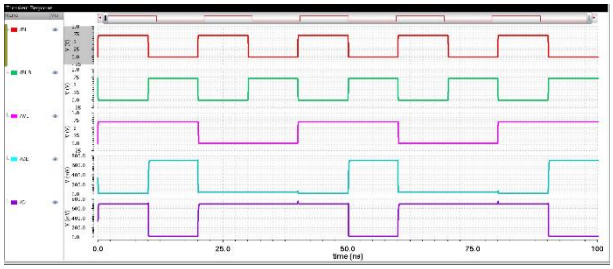

Figure 9: Transient simulation analysis waveforms of proposed SRAM during writing mode of operation

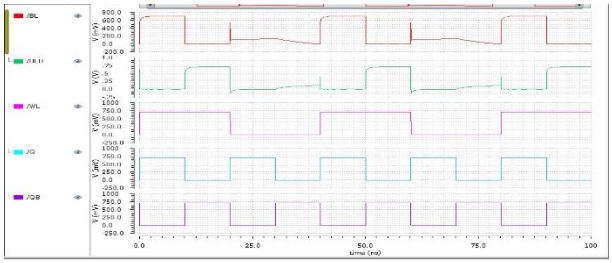

Figure 10: Transient simulation analysis waveforms of proposed SRAM during reading mode of operation

Table 2 shows how the suggested designs compare to current topologies for efficiency and power. The use of less transistors that are activated just when required, significantly reduces power consumption. This demonstrates the rapid functionality of the intended SRAM. The specified design exhibits a power consumption of 4.8 µW and a delay of 10.1 ns.In comparison to existing CMOS 6T SRAM and finFET 6T SRAM, the suggested SRAM has much lower power consumption and displays speed enhancements of at least 87% and 54%, respectively.

Table 2: Performance Comparison analysis of proposed SRAM

SRAM Design	Power Utilization (uW)	Delay(nS)
Static 6T CMOS SRAM[23]	75.3	40
finFET 6T SRAM	34.2	21.8
Proposed SRAM	4.8	10.1

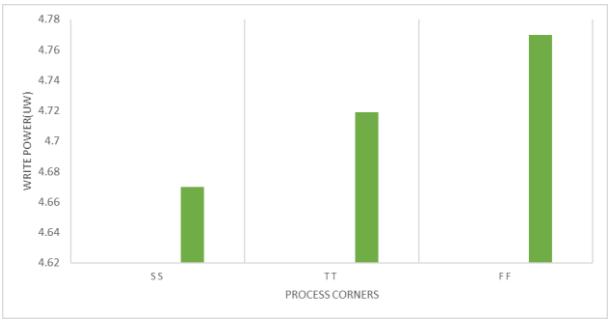

Figure 11: Power Usage during writing mode of operation across various process corners.

The calculated power usage at various process locations during both the writing and reading activities is depicted in Figures 11–12. Performance, stability, and power are all ultimately impacted by changes in the threshold potential that are a direct consequence of variations in the die. Taking into account all process modifications, the proposed SRAM storage cell demonstrates superior efficiency compared to traditional cells, hence enhancing the reliability of both write and read operations.

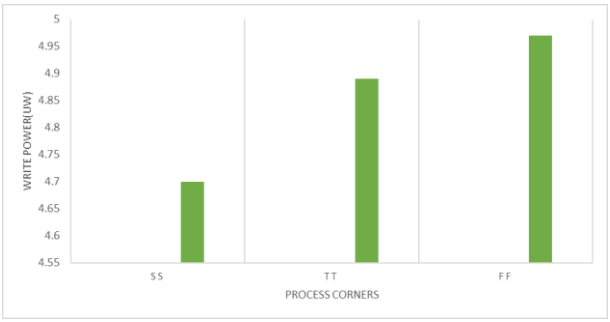

Figure 12: Power Usage during reading mode of operation across various process corners.

A voltage increment from 0.7V to 0.9V was implemented to assess its impact on power usage throughout writing and reading operations. Figures 13 and 14 illustrate the variations in power usage throughout writing and reading operations for different source voltages.

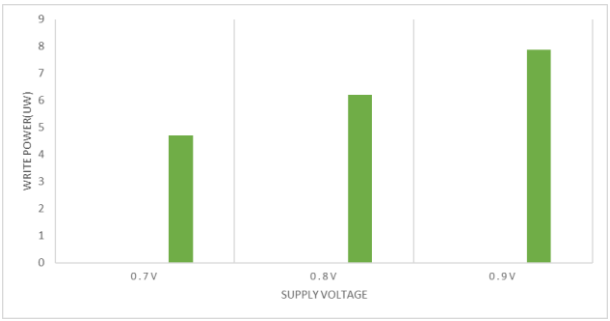

Figure 13: Power consumption throughout the writing mode w.r.t Supply voltage

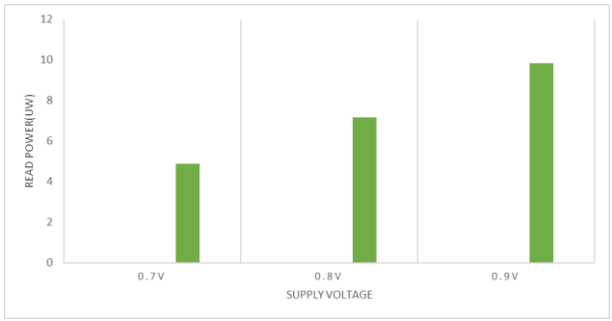

Figure 14: Power consumption throughout the writing mode w.r.t Supply voltage

The recommended SRAM cell has been subjected to calculations to ascertain the effects of temperature fluctuations. The temperature range that was evaluated spans from -50°C to 75°C. The variance in power consumption for writing and reading tasks as a function of source voltage is illustrated in Figures 15 and 16. Regardless of the temperature, the SRAM circuit that has been recommended demonstrates optimal power efficiency during writing operations and minimal power consumption during reading activities. The proposed SRAM cell has been subjected to calculations to ascertain the effects of temperature fluctuations. The temperature range under investigation is from -50°C to 75°C.

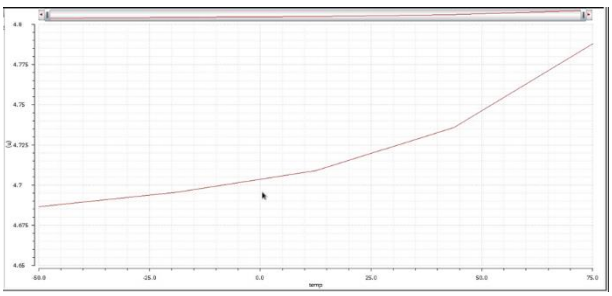

Figure 15: Power consumption during the writing mode w.r.t temperature

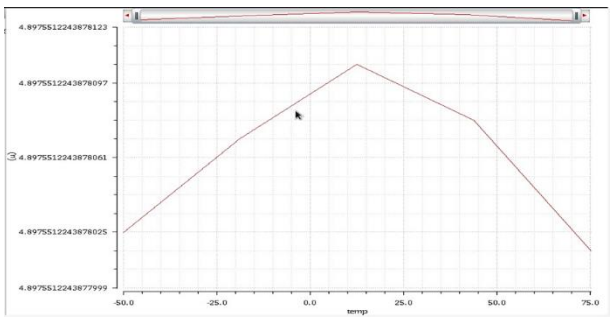

Figure 16: Power consumption during the reading mode w.r.t temperature

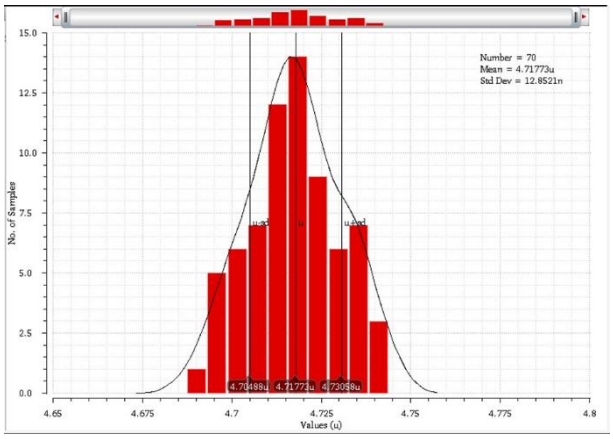

Figure 17: Performance a Monte Carlo calculation to evaluate the writing power of proposed SRAM

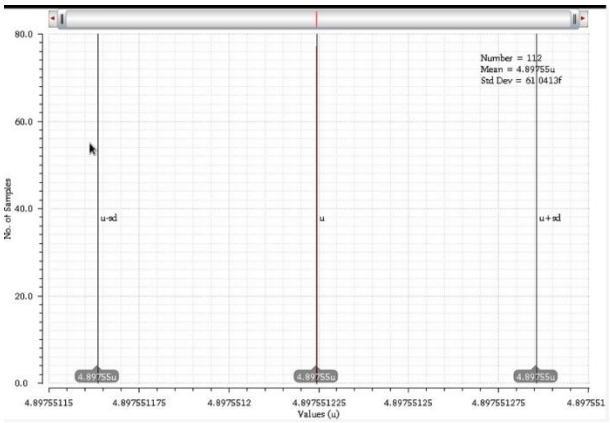

Figure 18: Performance a Monte Carlo calculation to evaluate the reading power of proposed SRAM

Natural variations in characteristics, such as random doping agent alterations, line boundary flaws, and oxide coating modifications, significantly impact the device's efficiency and performance. The impact on the SRAM chip was simulated using a Monte Carlo computation. The SRAM cells were statistically assessed by a Monte Carlo simulation method, utilising two hundred samples. The simulation's mathematical foundation employs a sigma value of three. The results of a Monte Carlo calculation addressing power consumption throughout the write and read processes are illustrated in Figures 17 and 18. The power consumption of the suggested SRAM cell fluctuates by about 10% during reading and writing activities.

An study was done on the proposed SRAM to evaluate its adaptability, since delay time is crucial in determining its effectiveness and efficiency. Figure 18 illustrates the impact of delay time across several process corners. Among all the alternatives in the FF corner, the recommended SRAM exhibits the lowest delay values. Fluctuating voltages may undermine the precision of monitoring delay time, especially at low voltage levels. The read and write latencies have been calculated for various process corners. The delay is expected to be more significant in the Slow Process corner and less significant in the Fast Fast process corner, as seen in Figure 19. Figure 20 illustrates the ramifications of changing the voltage between 0.7 V and 0.9 V.

The temporal delay resulting from temperature fluctuations is illustrated in Figures 21 and 22. The results indicate that the proposed SRAM cells meet the PVT standards for both write and read durations.

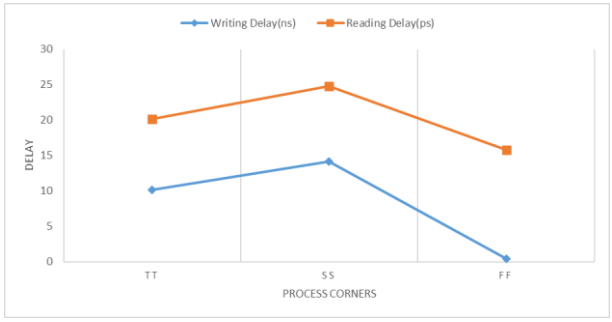

Figure 19: Delay analysis of the proposed across various process corners

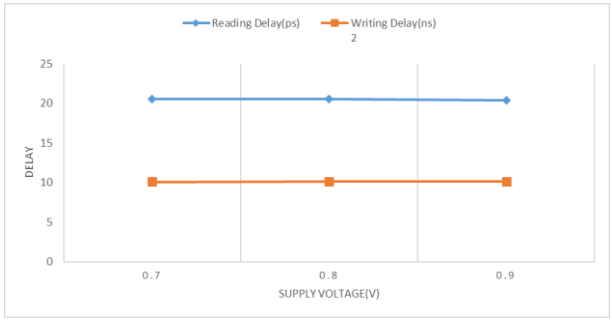

Figure 20: Delay analysis of the proposed 8T SRAM w.r.t source voltage

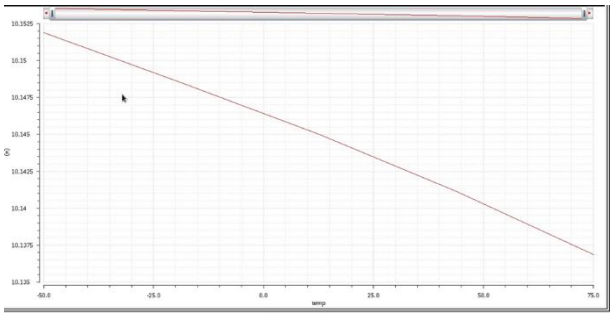

Figure 21: Delay during the writing mode w.r.t temperature

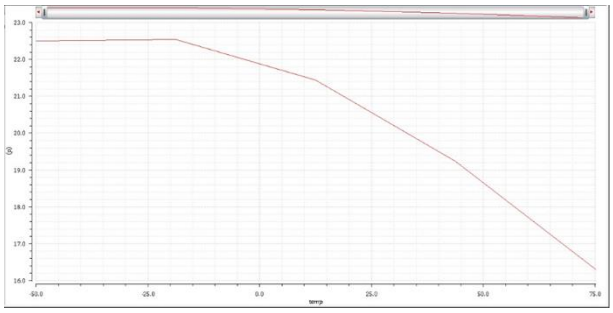

Figure 22: Delay during the read mode w.r.t temperature

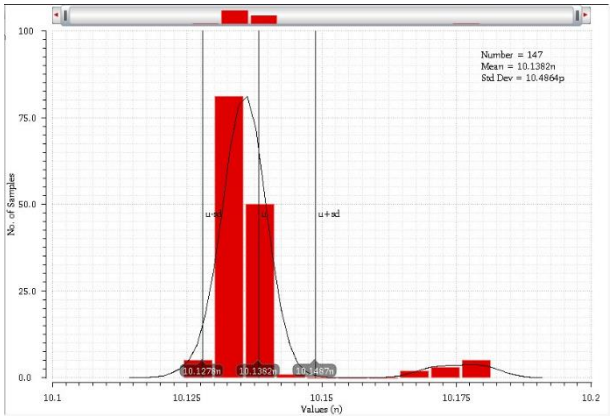

Figure 23: Performance a Monte Carlo analysis of writing delay in proposed SRAM

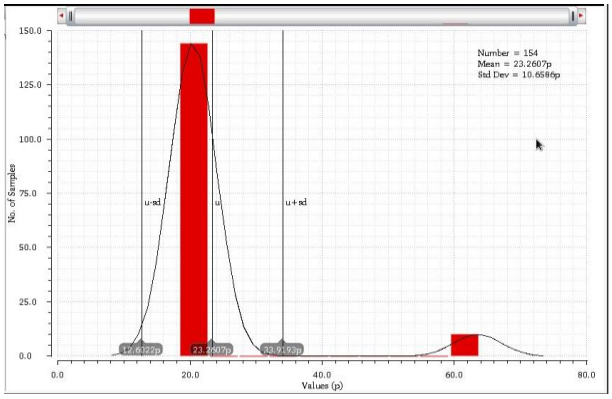

Figure 24: Performance a Monte Carlo analysis of reading delay in proposed SRAM

The efficiency of devices is considerably influenced by variations in intrinsic characteristics and alterations in the oxide layer. A Monte Carlo simulation was performed to assess the effects on the SRAM chip. The SRAM cells underwent statistical analysis using the Monte Carlo modelling method. The model included 200 samples, each with a sigma coefficient of 3. Figures 22 and 23 illustrate the results of a Monte Carlo simulation that quantifies the time delay encountered during write and read operations. Reliability tests and comparisons reveal that the suggested SRAM cell has a ±10% fluctuation in latency during read and write operations.

5. Conclusion

The current paper demonstrates the design and analysis of a 4T-2R SRAM device made utilising finFET 18nm semiconductor technology. After a comprehensive investigation of every element, it became evident that there had been a considerable variance in the power use of the 4T-2R SRAM storage during reading and writing activities. The memory array runs on a 0.7-volt power supply . The architecture is compared with traditional CMOS 6T SRAM, as well as FinFET enabled 6T SRAM. The assessment is conducted in relation to latency and power. It is evident that the hybrid SRAM which has been recommended consumes less power and has minimal latency. The Monte-Carlo investigation has additionally verified the reliability of the proposed device, and the results suggest that the suggested architecture's variability is superior to the performance of CMOS SRAM.

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