

A Dependable Multistage Interconnection Network Topology and Fault-Tolerance

Dr.D.Deepakraj¹,L.R.Aravind Babu²,Dr. V. Kavitha³, C Navaneetha⁴, Dr K Sreeramamurthy⁵

¹Assistant Professor/ Programmer, Dept. of Computer and Information Science, Annamalai University.
deepakraj0708@gmail.com

²Department of Computer and Information Science, Annamalai University, Annamalai Nagar, Tamilnadu, India.
er.arvee@rediffmail.com

³Associate Professor, Department of Computer Science and Engineering, Rajiv Gandhi College of Engineering and Technology, Puducherry. kavitha.ck13@gmail.com

⁴Assistant Professor, Panimalar Engineering College, Chennai, Tamilnadu. navaneetha27@gmail.com

⁵Professor, Department of Computer science Engineering, KoneruLakshmaiah Education Foundation, Bowrampet, Hyderabad-500043, Telangana, India.sreeram1203@gmail.com

Article History:

Received: 27-10-2024

Revised: 04-11-2024

Accepted: 13-12-2024

Abstract:

Interconnecting networks will become more and more popular as computer networks spread. To facilitate communication across processes in various networks, this paper examines the challenges associated with connecting heterogeneous computer networks. The course includes a thorough overview of pertinent literature. The degree of network interconnectedness, global addressing and routing strategies, and the roles played by interfaces and gateways between networks are covered. Developing larger supercomputers and more dependable parallel computing systems has garnered significant attention and effort. Multistage interconnection networks (MINs) are frequently utilized as interconnection mediums in supercomputer environments because of their fault tolerance, low cost, minimal transmission delay, and self-routing capabilities, enhanced by the growing number of nodes in the system. In distributed and parallel systems intended to provide quick and effective communication amongst high-capacity processors, MINs are frequently employed as switching fabrics.

Keywords: Path sets, multistage interconnection networks (MINs), computer network reliability;

1. Introduction

A multistage interconnection network (MIN) is an alternate and intermediate indirect network that connects big multiprocessor systems' common bus and crossbar. Compared to the crossbar network, they offer cheaper switching costs and superior performance over the shared bus. In networks-on-chips, broadband communications, decentralized and parallel structures, and huge scale integration (VLSI) designs, MINSs with $\log_2 N$ (N being the number of input and output nodes) shifting stages are often utilized technologies. These networks link N components, mostly processors, to N outputs, which can be memory modules or processing units [1]. An essential element in any workable, large-scale computer system is adequate fault tolerance. The wiring designs for Multistage Interconnection

Networks (MINs) that provide the highest fault tolerance and performance for a fixed quantity of components are the main topic of this study.

We study multipath networks with and without interconnections. Each routing component's redundant outputs are connected to physically separate components in the network's subsequent level via an interworked network. We employ random fault generation in conjunction with the straightforward fault metric of wholeness to assess fault tolerance by probabilistically quantifying the maximum number of defects that a network can withstand. For a network to be considered complete, there must be every pair of network endpoints via a non-faulty path. If the system can withstand network partitioning or endpoint isolation, then this measure is conservative [2]. However, it offers a straightforward decision test to compare the outcomes of errors in different networks.

We assess the effective aggregate bandwidth of faulty and non-faulty networks in the presence of faults by simulating message traffic over both networks for our performance evaluations. We simulate processor synchronization and message distributions to model a number of shared memory applications.

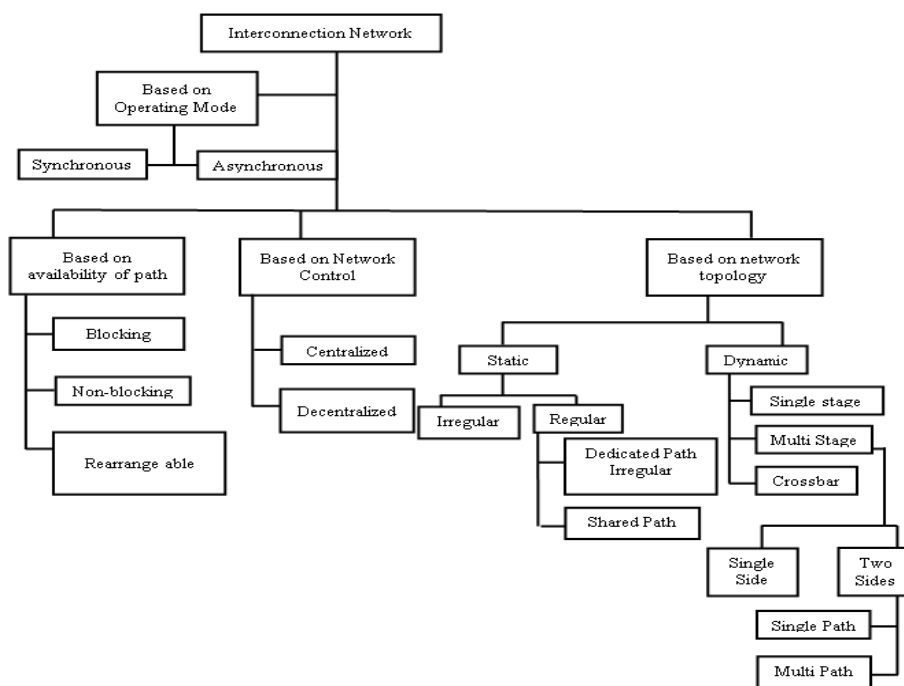


Figure 1.1 Multistage Interconnection Networks

Compared to crossbar networks, they offer cheaper switching costs and better performance than shared buses. MINs with $\log_2 N$ (N is the number of input and output terminals) shifting stages are frequently utilized in networks-on-chips, broadband communications, parallel and distributed systems, and the development of very large-scale integration. MIN provides communication between input and output by connecting layers of switching elements (SEs) in a predetermined architecture in Figure 1.1. MIN is classified as an indirect network.

With the advent of buffered switches, multistage interconnection networks have become widely employed in circuit switching and packet switching networks. MIN is an interconnecting system that enables communication between processor and memory modules by arranging several layers of

interconnected SEs in a predetermined architecture [3]. It has been implemented in numerous domains, primarily in multiprocessor environments, computer networks, and telephone networks. MINs are economical, fault-tolerant, and offer low transmission latency by utilizing multistage shifting fabric pathways to carry out several communication functions at once.

This is how this article is organized. Section 2 talks about this system's associated works. Section 3 describes how to apply the recommended methodology. Section 4 presents the results and discussions of the experiment. Section 5 presents the system's conclusion and future scope.

2. Literature Review

Reducing processor and/or memory unit losses at the expense of routing overhead is an alternative tactic [4]. Therefore, allowing numerous passes through the network can lessen the impact of a network link failure on the system when a multistage network is utilized for processor-to-processor connections. If every processor in the system may interact with every other processor in a limited number of network passes, passing the data through intermediary PEs if needed, the network is said to have dynamic full access (DFA) capabilities. While a single component failure eliminates the Omega network's full access capabilities, numerous problems do not eliminate the DFA capability. Therefore, assuming the faults do not impair the DFA property of the network, rebuilding without the loss of any processing is conceivable by creating a routing mechanism that permits routing through intermediate processors.

Over the past few decades, several MIN topologies have been proposed. The majority of these topologies are multipath or unique path networks. Since diameter is the longest path between any two nodes, multistage interconnecting networks aim to lower both the cost and the diameter [5]. Benes networks act as less resilient networks and offer various paths in the beginning, but just one path in the end after the intermediate stages. Additionally, the Clos network does not block MIN. The Clos network is more fault-tolerant than the majority of other MINs, which is one of its appealing features. Nevertheless, these networks are not a workable option due to two primary issues. Non-blocking MINs are typically more costly and difficult to manage than other MINs. Because it can handle errors by rerouting requests over alternate pathways, MIN with redundant routes is therefore preferred because it improves dependability.

The dependability and performance features of the networks connecting processors to processing and processors to stores are gaining more attention as multiprocessor systems become more widely accepted and used. There is a quick overview of interconnection networks as well as an examination of multistage interconnection networks' fault-tolerant features. We investigate the dependability features of multistage interconnection networks (MINs) in this research [6]. The uniquepath shuffle-exchange multistage interconnection network (SEN) and its variation, known as the SEN+, will be our specific areas of interest. An extra stage in the SEN+ network is utilized to boost the standard SEN's dependability. A number of studies discuss dependability concerns related to MINs. Furthermore, a number of academics have documented the application of multiple-path MINs to enhance dependability and fault tolerance.

In light of that approach, a novel Gamma minus Network has been presented in this study, which offers a disjoint minimal path set, high reliability, and fault tolerance capabilities while also lowering

the hardware complexity of the Gamma Network. Because Gamma Minus Network has one stage less than Gamma Network and offers multiple path features for every source-destination pair, including when the source and destination are the same, it has all of these benefits over Gamma Network, involving low cost, low hardware intricacy, high reliability, and fault tolerance [7]. Terminal reliability has been examined in order to assess the dependability of two networks.

Creating duplicate routes between each source-destination pair is the primary method for enhancing MINs' fault-tolerance [8]. One of the main concepts for adding redundancy to MINs' pathways is to increase the number of stages. What effects do adding more stages have on reliability, then, is the question that emerges here? Prior analyses have demonstrated that an additional stage improves MIN reliability. These investigations demonstrate that it is inefficient and unreliable to add more than one switching stage to MINs. The primary cause of this is the addition of multiple stages, which increases network complexity. Consequently, it was determined that increasing the number of switching steps can increase MIN dependability. However, this enhancement is constrained and might not adapt to systems with a larger scale. Therefore, in order to increase the fault-tolerance and reliability of MINs, we must search for advanced solutions.

The requirement for stochastic scenarios to handle the unpredictable and dynamic character of future demand and generation is acknowledged in the research on multi-stage planning models for distribution systems. The two-stage architecture, however, ignores the possibility of changing the network framework at the planning level in response to gradually revealed load development, even while it takes operational-level loads and uncertainties in distributed power sources into account [9]. Some studies have used Markov decision processes (MDP) to model the random procedure and roughly dynamic programming algorithms (ADP) to mitigate the "curse of dimension" issue in order to address the challenge of the large number of state and decision factors in multistage planning.

Buffers in MINs have been shown to greatly improve MIN performance, particularly in cases when traffic is irregular. Additionally, they guard against packet loss in the event of a path conflict. A packet can only exit its buffer when the destination buffer at the next step is able to accept it, if buffers are placed in each switch node and the back pressure method is used. Analytical performance evaluation is essential for different MIN deployments, whether buffered or unbuffered [10], in order to support the design's value under diverse operating circumstances. The performance model must also be straightforward and simple to extrapolate.

3. Methods and Materials

3.1 Motivation

The MIN architectures currently in use are either single or double fault tolerant. Less redundant and discontinuous pathways are offered by them. The design's limited fault tolerance leads to low terminal dependability. Self-routing capabilities are present in certain networks, but their rout ability is lacking. There are several complicated hardware architectures with extra intra-stage supplemental links, multiplexing devices, multiplexers, and extremely expensive layouts.

MINs can be created from a variety of angles. Reliability and fault tolerance are crucial factors in the design of interconnecting networks for huge networks when considering real-world circumstances. Important components for creating a MIN will need to be:

Fault tolerance MIN capability will be enhanced by the quantity of redundant and disconnected paths, routing, and dynamic rerouting behaviour [11][19].

Strong rerouting is provided via dynamic rerouting in the event of a switch failure. The design of MIN with variable rerouting property has been the focus of recent studies. Multiple switch breakdowns should be tolerated by MINs. Because the remaining processors can continue to communicate without any disruption in the event of a processor failure, this component is essential to MIN fault tolerance capacity. MINs should be able to handle several switch failures. This component is crucial to MIN fault tolerant capacity since, in the event of a CPU breakdown; the additional computers can still communicate without any interruption. By offering several redundant and discontinuous pathways, this study suggests a MIN that effectively meets a high dependable low-cost layout with dynamic redirecting ability.

3.1 Fault tolerant connection network (FTIN) design proposal

A fault-tolerant reliable multipath IN that offers several disjoint pathways between any S-D node pair is called a fault-tolerant interconnection network (FTIN) (see Figure 3.1) [12][18]. Having redundant pathways and the capacity to dynamically reroute transmissions can help achieve failure tolerance.

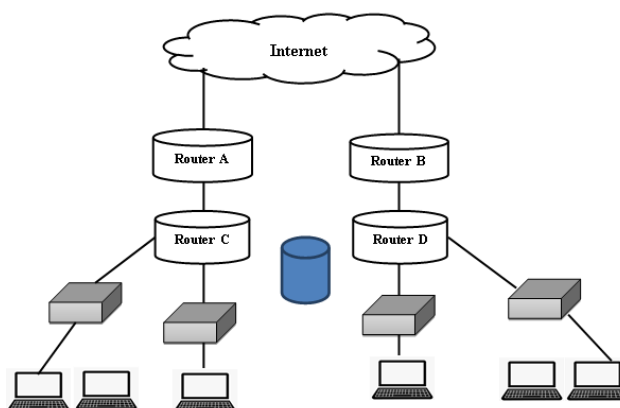


Figure 3.1 Fault Tolerant Interconnection Network Design

Through a detailed determination of the parameters and type of network parts, the network architecture depicts the network topology and its physical realization. Switches are typically used to connect the local components of such a network[20][21]. In nature, MINs combine different kinds of multiprocessor connectivity networks with crossbar and shared bus networks. MINs make an effort to shorten the journey and lower the cost. Prior academics have suggested a variety of techniques to improve the network's dependability. To handle failure in a SEN environment, several strategies have been put forth, such as implementing a multilayer network and lowering a network stage [13][22]. The SEN is a self-routing network that routes messages from any source to a specified destination based on the destination address's binary form.

In the event of network problems or conflicts with other connections, multipath MINs enable the selection of an alternate path. As the network grows in size, the blocking-induced performance loss and the fault tolerance-resulting reliability loss become more severe. Because alternate paths can be employed to lessen the impact of blocking in a random access environment, multiple path MINs perform better than unique path MINs. The majority of MINs suggested in the research are typically built with 2×2 bar switches and feature $n = \log_2 N$ stages, with $N/2$ SEs in each stage.

An entire interconnection network is not what a shuffling network is. A shuffle network can be transformed into a full connectivity structure by adding exchange iteration.

3.3 The basic topology of networks

The configuration of the links and nodes in a network connection is known as the network's topology. Each network may have the same topology even while the distances between its nodes, connections, transmissions, and signals vary. The images demonstrate the various kinds of basic topologies.

3.3.1 Network Shuffle-Exchange

The size of their SEs and ease of configuration have led to SENs being often regarded as offering handy connection systems [14]. By correctly assigning each SE to a straight or cross relationship, a distinct path can be created from any source to the intended destination. Since there are typically $(\log_2 N)$ stages between specific inputs and outputs in this network, the failure of any SE will have an impact on the entire network. From a given source to a particular destination, the message is routed according to the target address. Within this network, the address moves one bit to the left in a cyclical fashion within the link. SENs usually connect multiple inputs to N outputs, or $N \times N$. The network's size is indicated by the parameter N .

3.3.2 Enhanced Shuffle-Exchange System

Links between switching of the same stage are a characteristic of the ASEN, a standard multipath MIN. By cutting one network stage, the SEN can be modified to create the ASEN. ASEN has $(N/2)$ SEs and $[(\log_2 N) - 1]$ stages [15]. The ASEN is simpler to maintain and fix because loops are implemented as modules. By employing extra links to build loops, the ASEN generates numerous paths based on joining the switches that belong to a complementary population.

ASEN is a network that routes itself. It only has one fault tolerance; for example, if the source or target switches both malfunction, they are cut off from the remainder of the network.

4. Implementation and Experimental Results

4.1 Dependability of the terminal

Reliability is often defined as a system's capacity to operate and continue to do so under both normal and unanticipated conditions. Consequently, many researchers have been persuaded that it is the most immediate criteria for each effective network in the field of interconnection networks.

From the perspective of reliability, lifeline networks, including electrical and gas networks, wireless mobile ad hoc networks (MANETs), wireless mesh networks, wireless sensor networks with nano-

sensors based on nano-wired networks, social platforms, stochastic-flow manufacturing networks (SMNs), and interaction networks, are referred to as complex network systems.

Based on published studies, simulation or analytical approaches can be used to investigate the reliability of complex networks. The efficacy of simulation-based techniques is limited, despite their ease of implementation. For example, there should be a sufficient number of simulations run in order to provide a thorough analysis, which can take a lot of time. Additionally, compared to analytical methods, simulation yields a narrow range of outcomes. It is evident that the ease of use of simulation has trumped the intricacy of analytical methodologies. It is evident that the ease of use of simulation has trumped the complexity of analytical methodologies. Analytical techniques have been developed to provide an exact solution for calculating a system's reliability using reliability equations. Consequently, the lengthy computations and the simulation methodology's non-repeatability problem has to be fixed. Given a system's reliability equation, additional system evaluations can be carried out, including calculating the system's MTTF and precise reliability and failure rate values at particular times. Furthermore, design improvement initiatives can be supported by the application of reliability optimization strategies. As a result, the reliability block diagram (RBD) approach will be utilized in this work as a precise analytical technique for assessing the dependability of complex

Three factors can be used to evaluate MINs' dependability: network, broadcast, and terminal reliability. This study will examine terminal reliability, which is the likelihood of at least one fault-free path connecting a source and destination pair and indicates the reliability between them. The terminal's reliability on a specified basic path will be determined here.

The components of a system and their relationships are shown graphically in a reliability block diagram (RBD), which is used to assess the overall dependability of the system. RBDs can be shown in simultaneous or serial forms. The remainder

Two basic themes are combined to create one template. Figure 4.1 displays Series RBD.



Figure 4.1 RBD Series

Lastly, the routing method can be looked at to make sure the Pars network is designed correctly. The Pars network's routing method is made to be built for a variety of network sizes. Therefore, we can make sure that the right connection pattern is employed between stages by evaluating the routing method across the network in Table 1.

Table 1 Switch correspondence in the 8x8 and 16x16 Pars networks

Switches in stage 1 of 8x8 Par	Corresponding switches in stage 1 of 16x16 Pars	Switches in stage 2 of 8x8 Pars	Corresponding switches in stage 2 of 16x16 Pars
$SE_{1,1}$	$(SE_{1,1}, SE_{2,1})$	$SE_{1,2}$ $SE_{1,2}$	$(SE_{1,2}, SE_{2,2})$
$SE_{2,1}$	$(SE_{3,1}, SE_{4,1})$	$SE_{2,2}$ $SE_{2,2}$	$(SE_{3,2}, SE_{4,2})$

$SE_{3,1}$	$(SE_{5,1}, SE_{6,1})$	$SE_{3,2}$	$(SE_{5,2}, SE_{6,2})$
$SE_{4,1}$	$(SE_{7,1}, SE_{8,1})$	$SE_{4,2}$	$(SE_{7,2}, SE_{8,2})$
$SE_{5,1}$	$(SE_{9,1}, SE_{10,1})$	$SE_{5,2}$	$(SE_{9,2}, SE_{10,2})$
$SE_{6,1}$	$(SE_{11,1}, SE_{12,1})$	$SE_{6,2}$	$(SE_{11,2}, SE_{12,2})$

Investigating the networks' dependability in large-scale networks is important, even if Figure 4.2 offers useful information for network evaluation. IEGN, ABN, ASEN, EGN, and Pars network terminal reliability analysis findings as a function of network size.

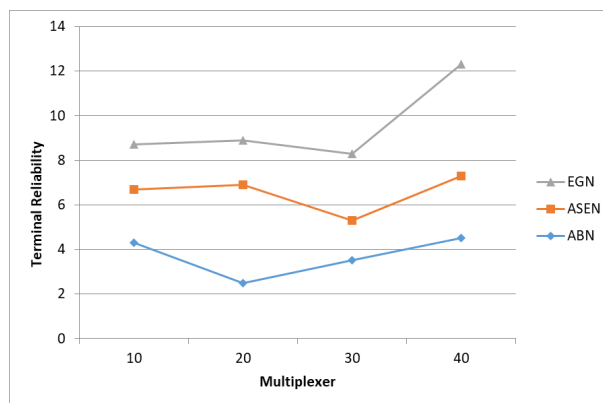


Figure 4.2 Reliability of a 2x1 multiplexer (or a 1x2 demultiplexer) versus terminal reliability in each fundamental path (r)

Table 2 presents the terminal reliability findings for the five 16x16 networks of Pars, ABN, ASEN, EGN, and IEGN.

Table 2 Comparison of 16x16 ABN, ASEN, EGN, IEGN, and Pars network' terminal reliability

r	$R_t(Pars)$	$R_t(ABN)$	$R_t(EGN)$	$R_t(ASEN)$	$R_t(IEGN)$
0.89	0.980650	0.954740	0.922944	0.902831	0.906937
0.88	0.883779	0.8459688	0.850363	0.815316	0.817197
0.87	0.826620	0.808751	0.783543	0.7242412	0.729882
0.86	0.772357	0.7443628	0.721689	0.644628	0.649913
0.85	0.720139	0.683545	0.663390	0.571461	0.575003
0.84	0.690070	0.6267892	0.609529	0.502736	0.505549
0.83	0.622426	0.572695	0.5595432	0.444338	0.44757
0.82	0.5761256	0.52175123	0.513619	0.389692	0.386272
0.81	0.5333874	0.472029	0.470452	0.344758	0.33466
0.80	0.492261	0.426535	0.4304367	0.257062	0.283223

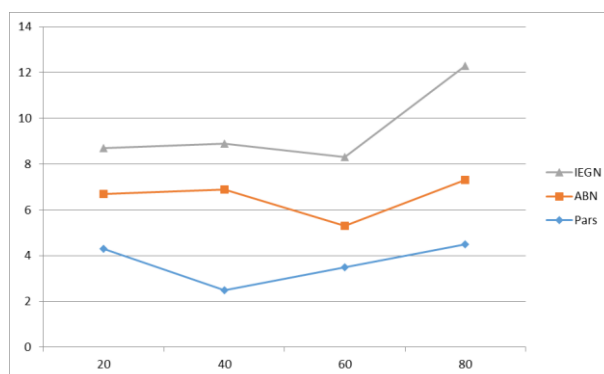


Figure 4.3 Among the three networks, ABN performs better

In other words, even while ABN outperforms the other three networks in terms of response time, this does not necessarily mean that ABN is better when taken into account together with its subpar performance in terms of arrival rate in Figure 4.3, expenditure, and consistency.

The Pars network works well in terms of response time in addition to providing adequate performance in terms of cost and arrival rate. Among other things, the Pars network outperforms ABN in terms of response time.

5. Conclusion

A novel fault-tolerant multistage connection network is suggested in this paper. Any pair of S-D nodes, they offers four disjoint pathways. By employing dynamic rerouting capability to efficiently exploit the multiple redundant channels, intermediate stages switch faults are tolerated.

The reliability assessment of several current MIN architectures was also examined in this study, and the suggested FTIN's reliability outperforms that of other MINs, making it an ideal option for multiprocessor interconnection networking.

Creating effective networks of connections is essential to the development of multiprocessor systems. Cost and performance are two crucial factors that essentially influence the striking design. In this research, we introduced the Pars network, a fault-tolerant MIN that is inexpensive because of its small switching elements (2x2). Additionally, it offers several routes between every source-destination pair, making the network resilient to errors. In terms of cost, fault-tolerance, terminal reliability, MTTF, and permutations capability, the Pars network performs better than the well-known regular MINs, specifically ABN, ASEN, EGN, and IEGN, according to the findings of a thorough performance analysis.

Furthermore, Pars' self-routing technique makes it straightforward but efficient. The Pars network is therefore a strong contender for usage in multiprocessor systems, according to the results obtained. However, it is thought that by merging the Pars network with other contemporary design techniques, it will be possible to show ever-better performance in the future. Recent studies, for example, indicate that multilayer MINs perform better and should be investigated further to produce the best designs.

References

- [1] Rajkumar, S., &Goyal, N. K. (2016). Review of multistage interconnection networks reliability and fault-tolerance. *IETE Technical Review*, 33(3), 223-230.
- [2] Chong, F., Egozy, E., &DeHon, A. (1992, March). Fault tolerance and performance of multipath multistage interconnection networks. In *Advanced Research in VLSI and Parallel Systems* (pp. 227-242).
- [3] Mun, Y., &Youn, H. Y. (1994). Performance analysis of finite buffered multistage interconnection networks. *IEEE Transactions on Computers*, 43(2), 153-162.
- [4] Varma, A., &Raghavendra, C. S. (1989). Fault-tolerant routing in multistage interconnection networks. *IEEE Transactions on Computers*, 38(3), 385-393.
- [5] Rajkumar, S., &Goyal, N. K. (2016). Reliable multistage interconnection network design. *Peer-to-Peer Networking and Applications*, 9, 979-990.
- [6] Blake, J. T., & Trivedi, K. S. (1989). Multistage interconnection network reliability. *IEEE Transactions on Computers*, 38(11), 1600-1604.
- [7] Gupta, S., &Pahuja, G. L. (2015). Terminal reliability assessment for a new gamma minus multistage interconnection networks. *Procedia Computer Science*, 70, 476-482.
- [8] Jahanshahi, M., &Bistouni, F. (2014). A new approach to improve reliability of the multistage interconnection networks. *Computers & electrical engineering*, 40(8), 348-374.
- [9] Wu, Z., Li, A., Sun, Q., Zheng, S., Zhao, J., Liu, P., &Gu, W. (2024). Multistage reliability-constrained stochastic planning of diamond distribution network: An approximate dynamic programming approach. *International Journal of Electrical Power & Energy Systems*, 156, 109701.
- [10] Salameh, Anas A., and Othman Mohamed. "Design and Performance Analysis of Adiabatic Logic Circuits Using FinFET Technology." *Journal of VLSI Circuits and Systems* 6.2 (2024): 84-90.
- [11] Rajkumar, S., &Goyal, N. K. (2016). Fault tolerant interconnection network design. *IETE Technical Review*, 33(4), 396-404.
- [12] Kruskal, &Snir. (1983). The performance of multistage interconnection networks for multiprocessors. *IEEE transactions on computers*, 100(12), 1091-1098.
- [13] Kruskal, &Snir. (1983). The performance of multistage interconnection networks for multiprocessors. *IEEE transactions on computers*, 100(12), 1091-1098.
- [14] Padmanabhan, &Lawrie. (1983). A class of redundant path multistage interconnection networks. *IEEE Transactions on Computers*, 100(12), 1099-1108.
- [15] Sharma, V., Ansari, A. Q., & Mishra, R. (2021). A novel design layout of three disjoint paths multistage interconnection network & its reliability analysis. *International Journal of Pervasive Computing and Communications*, 17(4), 390-403.
- [16] Soh, Hodges, and Nranžén Keljovic. "Development of Highly Reconfigurable Antennas for Control of Operating Frequency, Polarization, and Radiation Characteristics for 5g and 6g Systems." *National Journal of Antennas and Propagation* 6.1 (2024): 31-39.
- [17] Madugalla, A. K., & Perera, M. (2025). Innovative uses of medical embedded systems in healthcare. *Progress in Electronics and Communication Engineering*, 2(1), 48–59. <https://doi.org/10.31838/ECE/02.01.05>
- [18] Suma, P. B., M. E. Shobha, and Santhosh George. "On the convergence of the sixth order Homeier like method in Banach spaces." *Results in Nonlinear Analysis* 5.4 (2022): 452-458.
- [19] Velliangiri, A. "Security Challenges and Solutions in IoT-Based Wireless Sensor Networks." *Journal of Wireless Sensor Networks and IoT* 1.1 (2024): 6-9.
- [20] Prasath, C. Arun. "Cutting-Edge Developments in Artificial Intelligence for Autonomous Systems." *Innovative Reviews in Engineering and Science* 1.1 (2024): 11-15.
- [21] Rahim, Robbi. "Adaptive Algorithms for Power Management in Battery-Powered Embedded Systems." *SCCTS Journal of Embedded Systems Design and Applications* 1.1 (2024): 20-24.
- [22] Iqbal Ahmad, Iqbal, et al. "Fractals as Julia Sets of $a\exp[d\sin(z^n)]-bz + c$ via Jungck Four-Step Iterative Method with s-Convexity as Well as Four-Step Iterative Method." *Results in Nonlinear Analysis*, vol. 7, no. 3, 2024, pp. 1–18.