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Comparative Analysis of 3-2 Adder Compressor for High-Speed Applications

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Abstract— Adder compressors (ACs) are essential components in high-performance computing applications, including multipliers, machine learning, discrete transforms, and filters, due to their ability to perform efficient multi-operand addition in parallel data paths. This paper investigates the robustness of the 3-2 adder compressor designed using predictive 18nm FinFET technology, focusing on the impact of voltage scaling. The study highlights the advantages of FinFET technology in reducing power dissipation and improving speed compared to traditional MOSFET technology. Simulation results demonstrate that FinFET-based adder compressors exhibit a significant reduction in power-delay product (PDP) (95-99%) and a greater decrease in sum delay (54.68%) compared to MOSFETs (17.70%). However, FinFET's carry delay shows an increase (66.75%) compared to MOSFET's more consistent reduction (11.50%), indicating that the choice between FinFET and MOSFET may depend on specific application requirements.

Keywords: Adder Compressor, MOSFET, FinFET Technology, Voltage Scaling, PDP.

1.Introduction

In the fast changing semiconductor technology landscape, achieving great performance while reducing power consumption is a major issue. The most efficient way to accomplish multi operand addition is using N-2 adder compressors (ACs), which compress the N operands to just two [1]. The 3-2 adder compressor is an essential component in digital circuits, notably multipliers and signal processing applications. Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have long been fundamental to digital electronics, yet they encounter considerable difficulties at technology nodes smaller than 28nm. FinFET technology is now used extensively in advanced semiconductor production, particularly for high-performance computers and mobile devices. Furthermore, Carbon Nanotube Field-Effect Transistors (CNTFETs) represent a huge step forward in transistor technology. CNTFETs, which use carbon nano tubes as the channel material, have outstanding electrical features. They can function at lower voltages and faster switching rates than MOSFETs and FinFETs, while also being less prone to short- channel effects, making them promise for future scalability beyond existing silicon-based technology. Although still in the research phase, CNTFETs have the potential to be used in high- speed digital circuits, low-power devices, and

flexible electronics. The transition from traditional MOSFETs to FinFETs, as well as ongoing research into CNTFETs, exemplifies semiconductor technology's ongoing evolution, fueled by the need for digital circuits that are high-performing, energy-saving, and compact in a swiftly evolving technological landscape. Each technology has advantages and disadvantages, and their continued advancement will be critical in shaping the future of electronics and computer systems. ACs have been utilized in various significant computing kernels, including multipliers, multiply-accumulate (MAC) systolic arrays for machine learning [2], digital filters [3], discrete transforms [4], [5], [6], and video processing [7], [8], [9].

1.1 3-2 Adder Compressor and Its Importance:

Because they allow for quick multi-operand addition, adder compressors (ACs) are crucial in parallel data pathways [10]. Since it can merge three operands into two without the need for immediate carry propagation, the 3-2 adder compressor is very well-liked. 3-2 adder compressors are very helpful in a range of computing applications, including multipliers, digital filters, discrete transformations, and video processing systems, because of this property, which not only decreases circuit size but also boosts critical path latency and decreases power consumption. The kind of transistor used— conventional MOSFETs, FinFETs, or emerging CNTFETs—has a significant impact on the design and functionality of these adder compressors as semiconductor technology develops. Conventional field effect of metal-oxide-semiconductor For many years, transistors have served as the cornerstone of digital circuit design because they provide a reliable and affordable means of carrying out logic operations. However, MOSFETs face problems including higher leakage currents, short-channel effects, and greater power dissipation as technology advances to lower nodes, especially those below 28nm, which can reduce efficiency and performance. However, because of its three-dimensional structure, which enhances electrostatic control over the channel, FinFETs have emerged as a remedy to these limitations. This design enhances performance and energy efficiency by significantly minimizing short-channel effects and leakage currents, while also allowing for increased driving currents. The industry standard for sophisticated semiconductor manufacturing is FinFET technology, particularly in high-performance computers and mobile devices where low power consumption and fast speed are essential.

One possible advancement in transistor technology is the CNTFETs Carbon nanotubes are used as the channel material in CNTFETs, which have remarkable electrical properties such as high carrier mobility and low power consumption[]. Moreover, CNTFETs are more suitable for future scalability than what current silicon-based technologies can manage since they are less. The integration of adder compressors, particularly the 3-2 adder compressor, into new transistor technologies will be essential as the semiconductor industry develops to meet the growing need for digital circuits that are small, high-performance, and energy-efficient. Additionally, as process technology advances, the influence of process variability rises, particularly in circuits based on FinFETs. Because variations in power dissipation, signal delay, and overall circuit stability can be caused by sources of variability such as Metal Grain Growth (MGG) and Line Edge Roughness (LER) [14], [15]. To increase the efficiency and dependability of adder compressors and other crucial parts of today's computer systems, it will be crucial to comprehend these issues and make use of MOSFETs, FinFETs, and CNTFETs.

S = Sum + Carry << 1

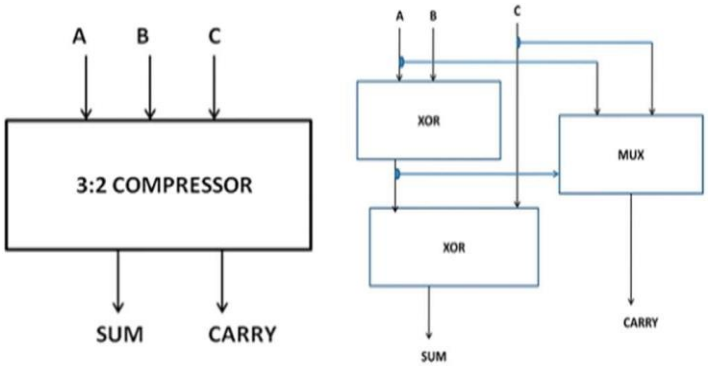

Figure 1: (a) Block diagram of 3-2 adder compressor

(b) Traditional implementation of 3-2 adder compressor.

1.2 Challenges in Various Transistor Technologies

1.2.1 MOSFETs:

Traditional MOSFETs have been fundamental in digital circuit design, but they confront considerable hurdles as technology advances to smaller nodes. Key concerns include increased leakage currents, short-channel effects, and greater power dissipation, which can degrade performance and complicate thermal management. Furthermore, the intricacy of circuit designs at lower nodes exacerbates power consumption and signal integrity difficulties, making high-density integrated circuits inefficient.

1.2.2FinFETs (Fin Field-Effect Transistors):

FinFETs overcome MOSFET limits by utilizing a 3D fin structure that improves gate control, reduces leakage, and enables scalability to sub-10nm nodes. They do, however, provide issues in terms of process unpredictability. Line Edge Roughness (LER) causes fin width changes, whereas Metal Grain Growth (MGG) modifies gate work functions, resulting in threshold voltage oscillations. These variations cause irregular power dissipation, signal delays, and reliability issues. FinFET-based circuits require robust design methodologies (e.g., statistical timing analysis) and modern manufacturing procedures to assure stability [12].

1.2.3 CNTFETs:

High-speed performance and ultra-low power operation are made possible by the exceptional carrier mobility of carbon nanotubes in CNTFETs [13]. However, its use is hampered by manufacturing problems. Creating homogenous semiconducting CNTs with consistent chirality and diameter is difficult.

1.3 Existing Research on Adder Compressors:

Several research have looked into several forms of adder compressors, such as 4-2, 6-2, and 8-2, to improve power efficiency and reduce silicon area [5], [7], [8]. Research has demonstrated that using

adder compressors in systems such as discrete transformations and video encoding can result in significant energy savings. While the performance advantages of adder compressors are widely known, little study has been undertaken on their resistance to Process, Voltage, and Temperature (PVT) fluctuations. Most previous research has focused on increasing efficiency rather than investigating how these compressors function under real- world variable conditions.

1.4 Simulation Tool:

1.4.1 Cadence Design Systems is a leading EDA (Electronic Design Automation) software provider for integrated circuit and system design. It offers a comprehensive suite of tools for custom IC design, digital design, verification, PCB design, and system analysis. Popular tools include Virtuoso (custom IC design), Innovus (digital implementation), and Spectre (circuit simulation). Cadence supports advanced node technologies like FinFET and provides solutions for analog, mixed-signal, and RF design. Its tools enable end-to-end design flow, from concept to manufacturing, ensuring high accuracy and efficiency. Cadence is widely used in industries for designing cutting-edge chips, including CPUs, GPUs, and IoT devices. It also offers AI-driven optimization and cloud-based design solutions for scalability and collaboration. Cadence is a critical tool for semiconductor companies, enabling faster time-to- market and innovation

2. Methodology

2.1Design Framework and Process Design Kits (PDKs):

The technique starts with picking the proper PDKs for each technology. MOSFETs use a typical CMOS PDK (such as 28nm or 45nm), whereas FinFETs use the ASAP7 PDK, which replicates 7nm technology with actual process parameters [18], [19]. CNTFETs use a specialized PDK to accommodate for carbon nanotube properties including chirality and alignment. Regular threshold voltage (RVT) transistors are used in all technologies to improve performance and power efficiency, with consistent transistor sizing to increase layout density[20].

2.1 Circuit Design and Simulation:

Cadence Virtuoso was used for circuit design and simulation of the 3-2 adder compressor, including schematic development, layout design, and symbolic representation. MOSFETs are designed using planar rules, whereas FinFETs require 3D designs and particular metal track spacing. To solve carbon nanotube alignment and contamination issues, CNTFETs require certain layout considerations.

2.2 Verification and Parasitic Extraction:

All technologies undergo Design Rule Check (DRC) and Layout Versus Schematic (LVS) verifications to ensure compliance with fabrication requirements. After verification, parasitic extraction (PEX) is used to simulate resistance and capacitance effects in Cadence Spectre, resulting in SPICE netlists for post-layout simulations. This procedure allows for an accurate assessment of power, latency, and signal integrity under real-world situations.

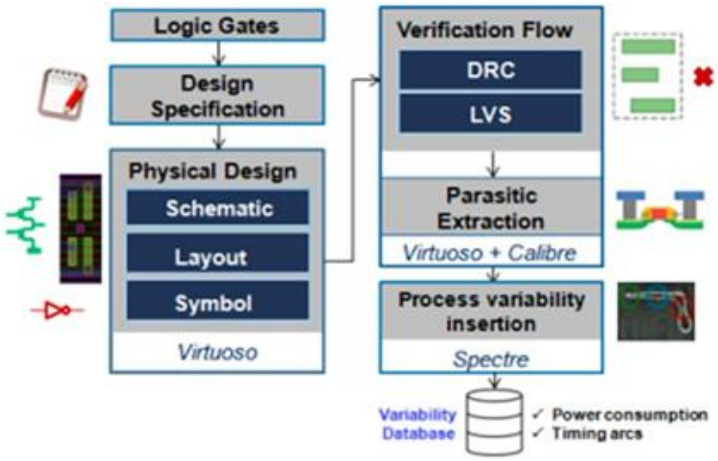

Figure 2: Flow chart of 3-2 AC

This unified methodology enables a comparative analysis of the 3-2 adder compressor across MOSFET, FinFET, and CNTFET technologies. By addressing technology-specific challenges—such as MOSFET leakage, FinFET process variability, and CNTFET fabrication complexity—the study identifies design optimizations for power, performance, and reliability.

3. Proposed Method

The study investigates the reliability of a 3-2 adder compressor (AC) developed in 18nm FinFET technology, with a focus on its resistance to PVT fluctuations. The work uses the 18nm FinFET process design kit (PDK) from ARM to assure realistic lithography and manufacturing restrictions. The 3-2 AC, which is required for multi-operand addition in applications like as multipliers and machine learning accelerators, uses three-fin transistors in both PFET and NFET devices to improve mobility and threshold voltage while resolving layout density concerns. The circuit is built with the Cadence Virtuoso tool, which includes schematic design, layout generation, and symbolic representation. The design method focuses on optimizing the logical structure to reduce latency and power consumption while following the 18nm FinFET design requirements for manufacturability. A concise symbolic representation makes integration into bigger computing platforms easier. Design Rule Check (DRC) verification ensures conformity with production restrictions, while Layout Versus Schematic (LVS) verification confirms the layout fits the intended design. The circuit's resistance to PVT fluctuations is assessed using Monte Carlo simulations with the Cadence Spectre tool, which includes 2,000 simulations that model process variability [11]. A Gaussian distribution is used to approximate work function fluctuations, while voltage variability is measured by adjusting the supply voltage by ±10%5. According to the study, power consumption can vary by up to 20%, latency can increase by 11-15%, and the power-delay product (PDP) can shift by around 10% as a result of these changes.

The results show that process fluctuations are the most important factor influencing the performance and reliability of the 3-2 adder compressor, particularly in near-threshold operation. This highlights the importance of rigorous design techniques in advanced FinFET technologies. Future research will concentrate on the resilience of higher-order adder compressors and the effects of radiation-induced transient faults, as well as circuit and layout-level solutions to reduce the influence of PVT changes

and improve the reliability of FinFET-powered devices [13].

4. Simulation results

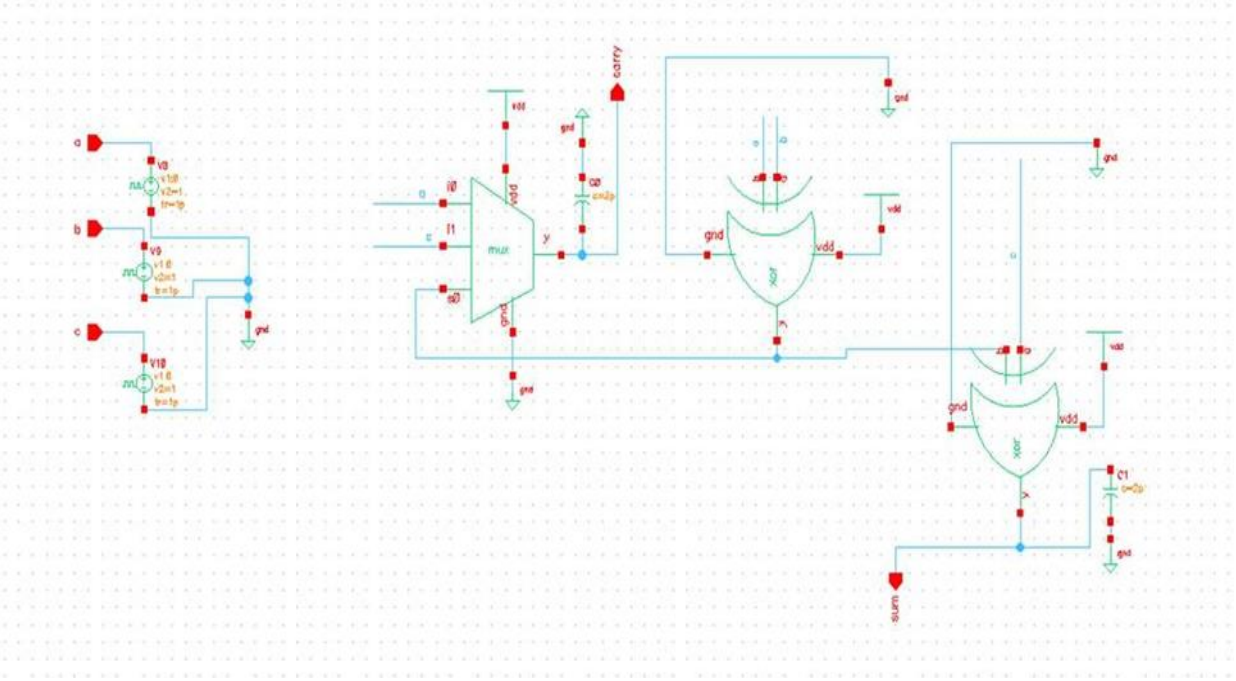

Figure 3: Schematic of 3-2 AC using FinFET in Cadence

Figure 4: Sum and Carry Delay Trends in FinFET Adder Design

From Figure : 4 The FinFET technology's delay measurements at various voltages (0.6V to 1V) are expressed in nanoseconds (ns). While the "carry" operation's delay rises from 9.608 ns at 0.6V to 16.02 ns at 1V, the "sum" operation's delay falls from 79.06 ns at 0.6V to 35.82 ns at 1V.2.

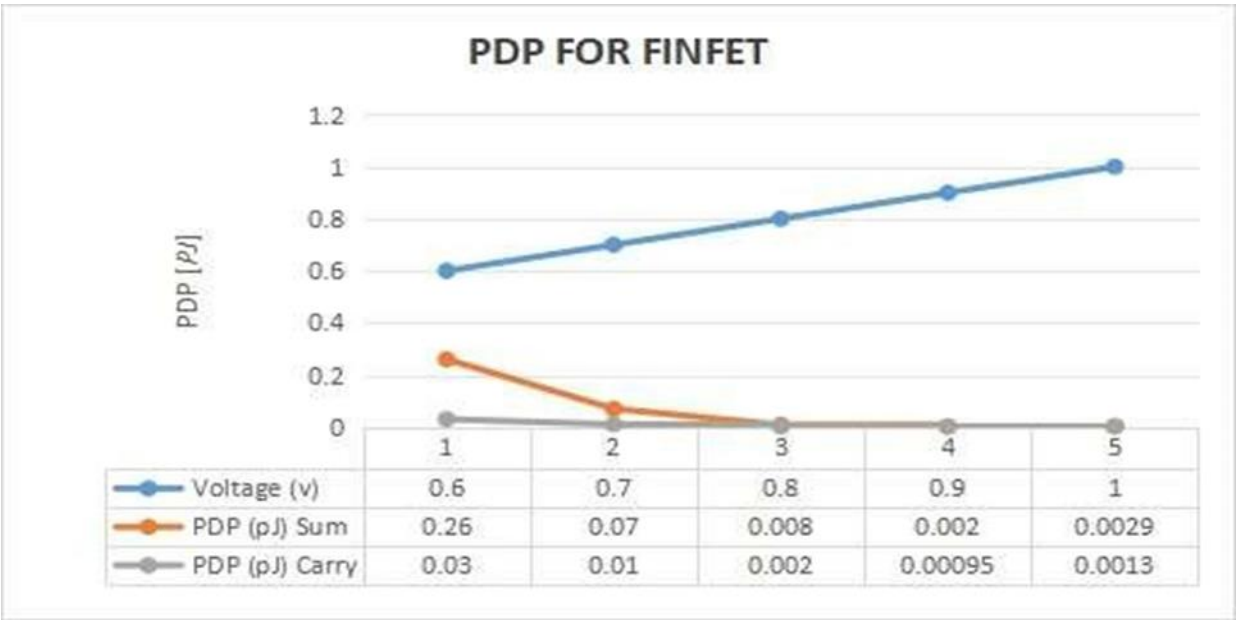

Figure 5: Effect of Supply Voltage Changes on PDP of 3-2 AC

From Figure : 5 For both "sum" and "carry" operations, the Power- Delay Product (PDP) is expressed in picojoules (pJ). From 0.26 pJ at 0.6V to 0.0029 pJ at 1V, the PDP for the "sum" operation and the "carry" operation both drastically drop from 0.03 pJ at 0.6V to 0.0013 pJ at 1V.

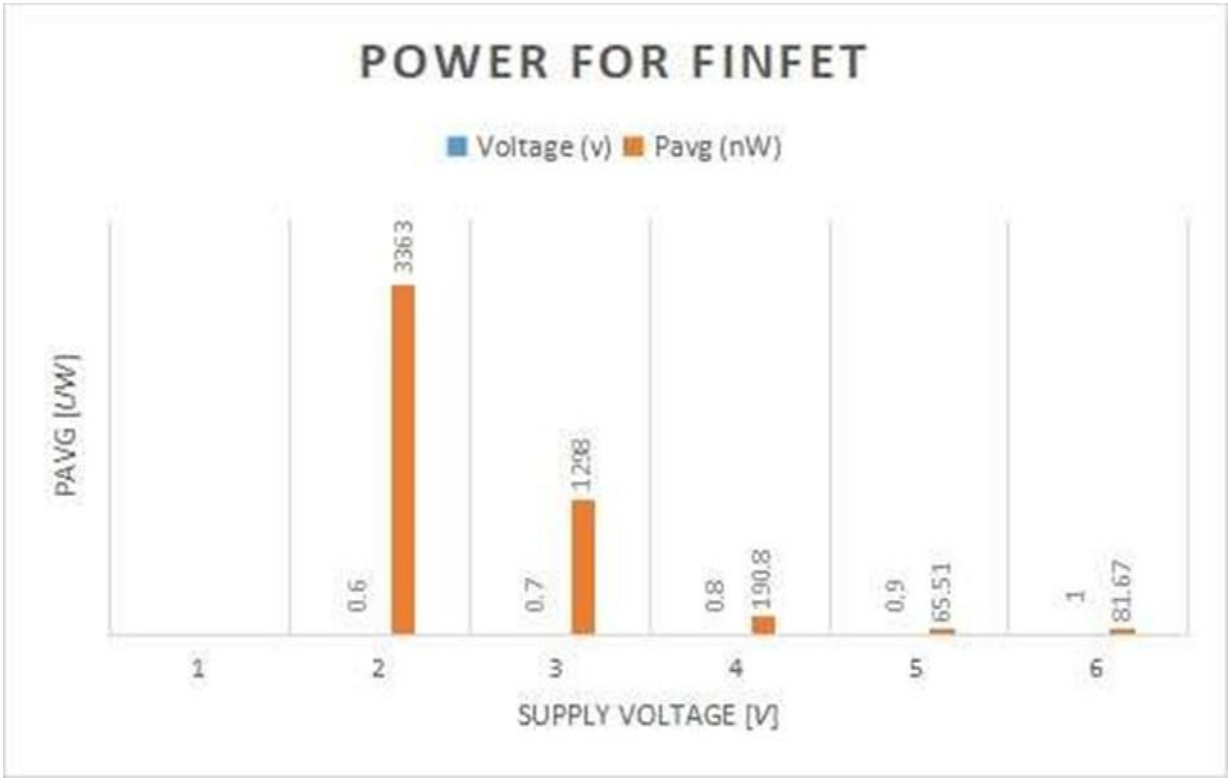

Figure 6: Impact of Power and voltage of the 3-2 AC.

From Figure : 6 Power measurements for FinFET at various supply voltages are included in nanowatts (nw)

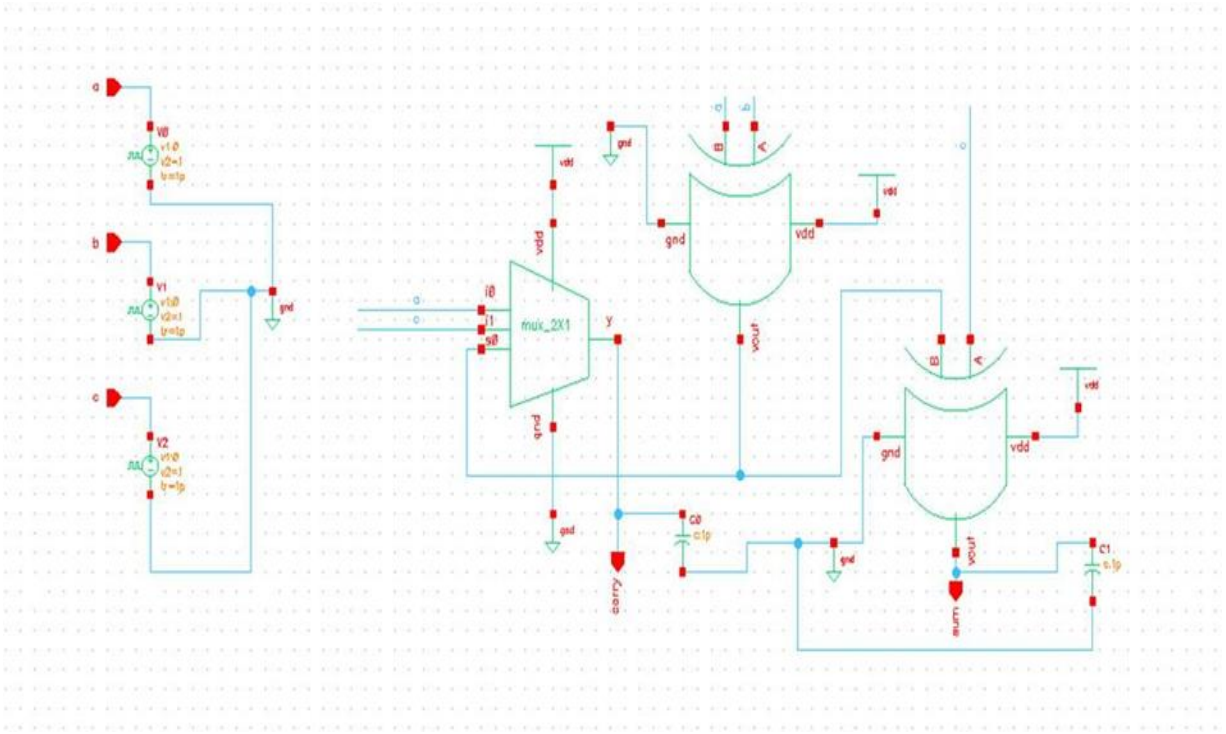

Figure 7: Schematic of 3-2 AC using MOSFET in Cadence

	1	2	3	4	5
Voltage (v)	0.6	0.7	0.8	0.9	1
Delay (ns) sum	14.87	14.07	13.33	12.71	12.24
Delay (ns) carry	9.14	8.85	9.42	9.32	8.09

Figure 9: Effect of Supply Voltage Changes on PDP of 3-2 AC

From Figure : 8 the report gives MOSFET technology delay measurements in nanoseconds (ns) at various voltages (0.6V to 1V). While the "carry" operation's delay varies somewhat, from 9.14 ns at 0.6V to 8.09 ns at 1V, the "sum" operation's time drops from 14.87 ns at 0.6V to 12.24 ns at 1V. 2.

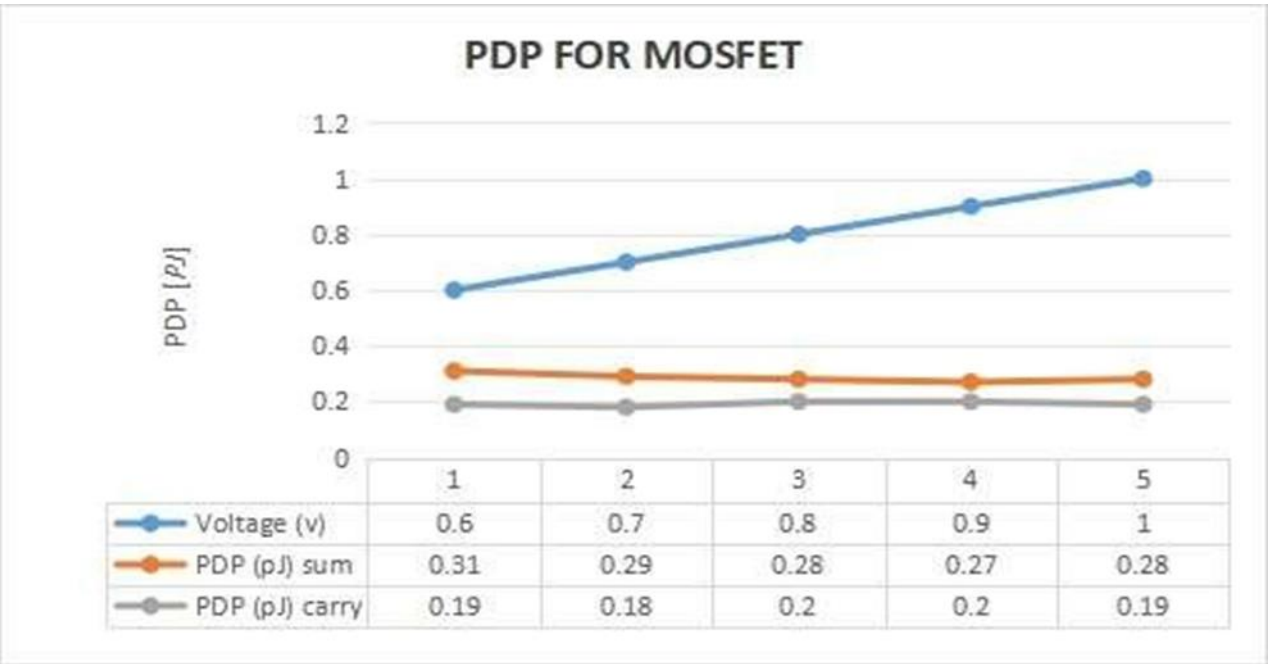

Figure 8: Sum and Carry Delay Trends in MOSFET Adder Design

From Figure : 9 for both "sum" and "carry" operations, the Power- Delay Product (PDP) is expressed in picojoules (pJ). While the PDP for the "carry" operation also exhibits some variations, ranging from 0.19 pJ at 0.6V to 0.2 pJ at 0.8V and 0.9V, the PDP for the "sum" operation is comparatively constant, ranging from 0.31 pJ at 0.6V to 0.28 pJ at 1V.

Figure10: Impact of Power and voltage of the 3-2 AC.

From Figure : 10 Power measurements for MOSFET at various supply voltages are included in the document in nanowatts (nW).

TABLE : 1 POWER, DELAY AND PDP OF 3-2 AC of FinFET

Voltage (*v*)		0.6	0.7	0.8	0.9	1
Pavg (*nW*)		3363	1298	190.8	65.51	81.67
Delay (ns)	**sum**	79.06	56.68	45.27	39.44	35.82
	carry	9.608	12.32	12.39	14.58	16.02
PDP (*pJ*)	**sum**	0.26	0.07	0.008	0.002	0.0029
	carry	0.03	0.01	0.002	0.00095	0.0013

Table : 1 Represents the data on voltage, power, delay, and Power-Delay Product (PDP) for various components (sum and carry) are included in the table. the typical power usage for various voltages, expressed in nanowatts (nW). For instance, the power is 3363 nW at 0.6V and falls with increasing voltage.The total component's delay at various voltages, measured in nanoseconds (ns). The delay drops from 79.06 ns at 0.6V to 35.82 ns at 1V as the voltage rises. The total component's power-delay product, expressed in picojoules (pJ). This statistic provides an estimate of energy efficiency by combining power and delay. As the voltage rises, the PDP dramatically drops, going from 0.26 pJ at 0.6V to 0.0029 pJ at 1V.In practice, the dynamic power dominates over static power at higher frequencies, while static power becomes more significant at low frequencies.

TABLE : 2 POWER, DELAY AND PDP OF 3-2 AC of MOSFET

Voltage (*v*)		0.6	0.7	0.8	0.9	1
Pavg (*uW*)		21.36	21.27	21.39	21.69	23.68
Delay (ns)	**Sum**	14.87	14.07	13.33	12.71	12.24
	carry	9.14	8.85	9.42	9.32	8.09
PDP (*pJ*)	**sum**	0.31	0.29	0.28	0.27	0.28
	carry	0.19	0.18	0.2	0.2	0.19

Table : 2 Represents the Data on voltage, power, delay, and Power-Delay Product (PDP) for various components (sum and carry) are included in the table. Microwatts (uW) of average power consumption for various voltages. As the voltage rises from 0.6V to 1V, the power stays comparatively constant at 21–23 uW. 2. The sum component's delay in nanoseconds (ns) at various

voltages. As the voltage rises, the delay somewhat decreases, going from 14.87 ns at 0.6V to 12.24 ns at 1V. The total component's power-delay product, expressed in picojoules (pJ). Throughout the voltage range, the PDP for the sum component stays comparatively constant, ranging from 0.27 pJ to 0.31 Pj.

5. Conclusion

This work tested the power, delay, and PDP performance of the 3-2 adder compressor using FinFET and MOSFET technologies. The results indicate that several variability sources affect the performance of the circuit, modifying its expected behavior. FinFET is more power-efficient since its PDP significantly reduces (95-99%), while MOSFET's PDP is comparatively fixed. FinFET reduces sum delay by higher percentage (54.68%) than MOSFET (17.70%), so it is suitable for high-speed computations. MOSFT's carry delay is more consistent (reduces 11.50%), while FinFET's carry delay increases (66.75%), which could be a disadvantage in some applications. Overall, FinFET is superior in reducing power consumption and improving performance, making it the better choice for modern high-speed, low-power applications. In the future, further research needs to study the robustness of new adder compressor architectures, including 4-2 and 5-2 topologies.

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