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Design and Optimization of Reversible Quaternary Scalable Multiplexers and De-multiplexers

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Abstract: Minimizing information loss in digital systems is important because it helps in saving power. Quaternary reversible circuits, which use four levels of logic instead of the usual two, are becoming popular because they can be more energy-efficient. This paper introduces a new and scalable design for key circuits in computing, specifically 4 × 1 Multiplexers and 1 × 4 Demultiplexers, and also n x 1 multiplexers and 1 x n Demultiplexers using special gates designed for quaternary logic. This paper proposes, a general method for building larger versions of these circuits. Compared to existing designs, proposed circuits will be more efficient because they use fewer resources and produce less waste, which will improve the performance of processors in digital systems. In circuit analysis, multiplexers and demultiplexers are essential components of the Arithmetic Logic Unit (ALU). The performance of the processor is greatly impacted by their effective design. This work realized by using EDA tools and performance of proposed techniques is analyzed in terms of quantitative outcomes and calculating Power, Delay and Power Delay Product (PDP) in Nano meter technology.

Keywords: Reversible Quaternary Logic circuits, Multiplexers, Demultiplexers and Nano meter technology

1. Introduction

The limits future circuit design to high power consumption. As early as in 1961, In circuit design, Landauer showed that irreversible gates cause energy loss [1]. Zhirnov et al. pointed out that CMOS technology won't be efficiently cooled because of power dissipation [2]. Bennett's work shown that using reversible gates in circuit design does not result in power dissipation [3]. Input vectors can be obtained from the vectors that are generated and vice versa since reversible gates have an equal number of inputs and outputs [4, 5, 6]. Fan-out and feedback must also be excluded from these circuits [6]. Reversible circuits are regarded as a major facilitator for the development of quantum computing technology because of their intrinsic reversibility [7], [8].

Compared to classical computing, quantum computing has the ability to greatly decrease computational complexity and perform more efficiently. For example, a search in an unprocessed database can be completed by quantum algorithms in roughly √(N) steps, while classical algorithms need N steps to accomplish the same task [9], [10]. Since binary logic is predicted to encounter major difficulties because of serious reliability and thermal concerns, multiple-valued logic has attracted a lot of interest [12]. Reversible multiple-valued logic is more efficient in quantum processing of data and provides greater safety in quantum encryption [14] as compared with reversible binary logic. It also has increased tolerance for errors in quantum calculations and lower connectivity complexity as well as lower power consumption. Ternary logic is one of the most effective types of multiple- valued logic among the others operates in this domain.

A disadvantage is that standard binary logic circuits can be a very difficult to symbolized in ternary logic. Two bits can express binary logic functions in quaternary logic by being a group of quaternary values. Quantum quaternary logic The memory unit uses qudit, which can be appear in the following categories: |0⟩ |1⟩, |2⟩, and |3⟩. The 4x1 vector equation is used to represent the corresponding states (1).

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} |1\rangle = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} |2\rangle = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} |3\rangle = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$$

Key circuits such Decoders, half subtractors, full adders, parallel adders, and comparators have been developed as a result of recent developments in quaternary reversible logic [15]–[17]. Circuits for multiplexers and demultiplexers are essential parts of desktops, storage systems, communication systems, converters, and arithmetic logic units [17]. With an emphasis on developing more effective quantum quaternary circuits, this study introduces novel designs for quaternary reversible multiplexers and demultiplexers [17]–[23]. Quantum cost, consistent inputs, and trash outputs are used to evaluate the suggested circuits. With an emphasis on reducing this . The quantum cost is the sum of the 2-qudit Muthukrishnan-Stroud gates and quaternary bidirectional 1-qudit shift gates used in the circuit [17], [26]. Information loss is minimized by lowering the number of repetitive outputs needed for reversibility, which is indicated by the garbage output count [17], [25]. Th

standardized quantities (0, 1, 2, or 3) required for logic circuit synthesis are represented by the number of steady inputs; a greater count improves circuit effectiveness [17], [24].

The main features are reduced while creating quantum quaternary logic circuits for increased efficiency. The suggested quaternary circuits have better garbage output counts, constant input counts, quantum costs and its truth tables for addition, multiplication and its unitary quaternary transform matrices than current designs [17], [19], and [23]. The format of this document is as follows: The basics of quadraple reversible gates and quaternary Galois fields are covered in Section II. Extensible quadruple bidirectional multiplexer and demultiplexer design is shown in Section III.Conclusion, discussed in Section IV examines the assessment and valuation of the proposed networks.

2. Fundamental Principles

Quaternary Galois fields and quaternary bidirectional gates are introduced in Section I and are discussed in more detail in the following sections.

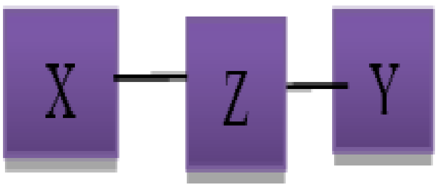


Figure 1. A graphic representation of the quaternary 1-qudit shift gates is shown.

A.Galois Field Quaternary Logic

The values Q = {0, 1, 2, 3} and the addition and multiplication processes that characterize the algebraic framework of the Galois Field (GF4) in quaternary logic. According to [27], these have multiplication features and are both associative and additive.

B. First-Quantit Shift Gates

In bidirectional logic, quaternary 1-qudit shift gates function as 4x4 unitary matrices that use a Z transform to translate input X to output Y[27].

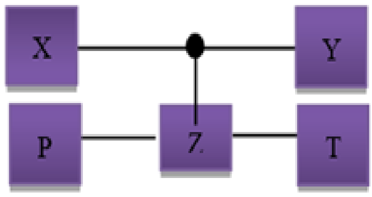


Figure 2. The quaternary 2-qudit Muthukrishnan- Stroud gate is shown symbolicall

C. Second-Quantative Muthukrishnan-Stroud Gates

A family of 2-qudit gates for liquid ion- trap quantum computation was presented by Muthukrishnan and Stroud [28]. The outputs under go particular changes where the control input X=3 is equal to 3 then,

IV= (X, P)

OV == (Y=X, Q=Z transform (1-qudit transform) .The inputs of the quadraple Muthukrishnan-Stroud (M-S) gate are X and P, and the outputs are Y and Q. When X = 3, Y = X, and Q is subjected to a 1-qudit transform of input B, X = P. Otherwise, Q equals P. This gate, which has a quantum cost of 1, is shown in Figure 2.

D.Quaternary 3-Qudit Managed Feynman Gate

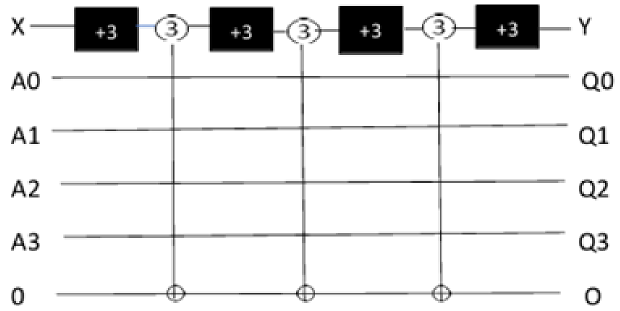
The quaternary controllable Feynman gate is a three-entry, three-endt gate that, when N= 3 X=3, maps (X, P, R) (X,P,R) to $(Y = X, T = P, S = P \oplus R)$ (Y=X, T=P, S=P⊕R); otherwise, R stays constant [29]. And can be removed with a quantum cost of 6

3. Proposed quaternary Reversible Circuits

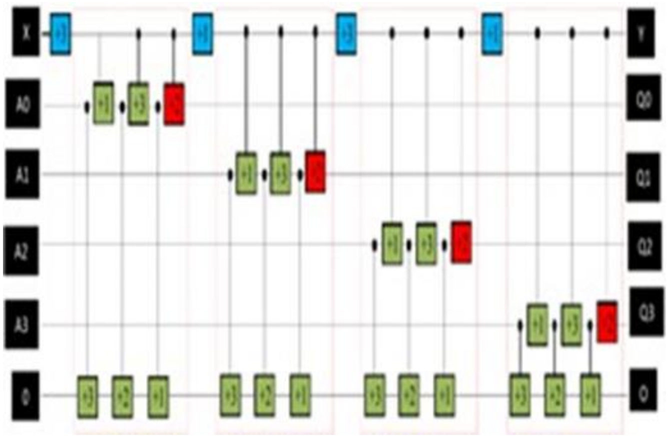
A scalable 4×1 reversible multiplexer is used to create quaternary bidirectional 16×1 and n×1 multiplexers. As same as to th emultiplexer.In order to reduce garbage outputs, constant inputs, and quantum cost, the design makes use of 3-qudit Coordinated Feynman gates and 1- qudit Shift gates.

A. Proposed Quaternary Reversible Multiplexer Circuit

An input is chosen by a quaternary 4 × 1 multiplexer using a selection line A, which may have values of 0, 1, 2, or 3.When A = 0, 1, 2, or 3, and A = 0, 1, 2, or 3, the equivalent output is either A0, A1, A2, or A3.



(a)



(b)

Figure 3. a) Symbolic depiction of the suggested quaternary reversible 4 × 1 multiplexer circuit. b) M-S and shift gates are used in the implementation.

The suggested quaternary reversible 4 × 1 multiplexer circuit, which makes use of four quadraple 1-qudit Shift gates and four quaternary 3-qudit Controlled

Feynman gates, is shown in Figure 3a. Together with a constant input of 0, the main inputs are A0 to A3. The output O is determined by selector X, whereas trash outputs are represented by Y, Q0, Q3, and Q3. The inputs A0 to A3 correspond to the outputs Q0 to Q3, and Y makes sense in relation to selection X. The initial Managed Feynman gate (control value 3) sets O=A0 when X=0. The 2nd Controlled Feynman gate, which similarly has control value 3, sets O=A1 if X=1.

Figure 6a displays the logical layout of the suggested quaternary 16 × 1 multiplexer, which was constructed using 4×1 multiplexers. There are five 4 × 1 quaternary multiplexers in this configuration. The 1st row multiplexers pick their second inputs when $B = 1$ B=1, and they trigger their first inputs when $P = 0$ P=0. Likewise, for P=2 and P=3, respectively, the third and fourth inputs are activated. The second, third, and fourth multiplexers route their outputs to O when X=1,2, or 3, but the primary multiplexer routes its output to O when X=0.With red boxes denoting the recommended 4 × 1 design, Figure 6b shows how to create a quaternary bidirectional 16 × 1 multiplexer utilizes a 4×1 multiplexer.Five steady inputs (0), sixteen major inputs (T0 to T15), selectors A and B, the major output O, and trash outcomes (T0 to T15), as well as the main inputs (T0 to T15) make up the circuit. With a quantum cost of 140.

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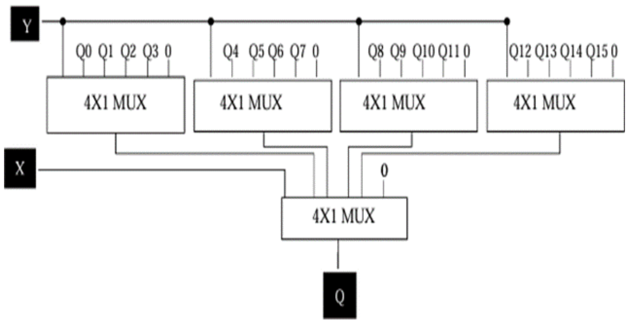
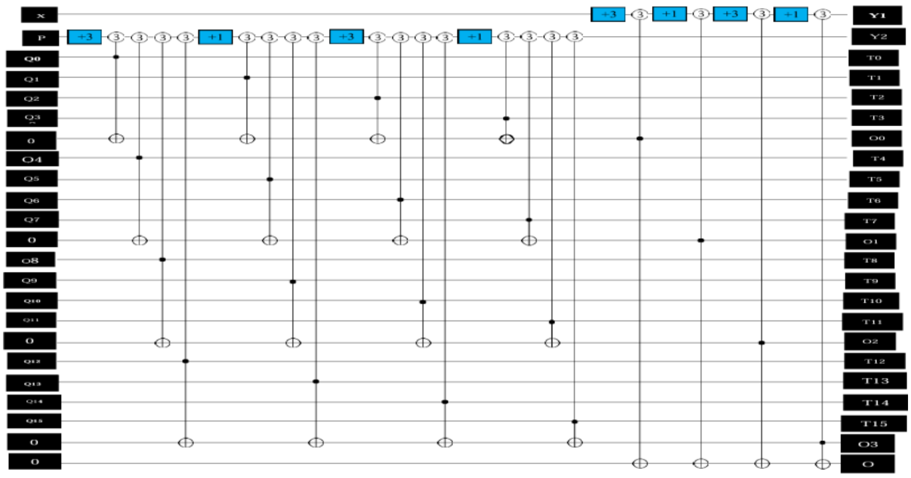
However, by removing unnecessary outputs (T0 and T15), a second version lowers the quantum cost to 120.By employing eight quaternary Shift gates and twenty quadruple manageable Feynman gates, this construction lowers quantum cost and produces a more effective multiplexer network.

An enhanced design achieves a lower quantum cost of 108, which is much lower than the initial realization, by employing 100 quaternary Muthukrishnan-Stroud gates, eight quaternary Shift gates, and Feynman gates. Five constant inputs and 22 trash outputs are maintained in both implementations. A quaternary reversible n×1 multiplexer circuit that is generalized, which builds upon the original 4×1 reversible multiplexer architecture, is further depicted in Figure 4 as given below.

The circuit needs m rows of 4×1 multiplexer, with There are 4 m−1 multiplexers in the 1st row, 4 m−2 multiplexers in the second row, and one multiplexer in the last row. Geometric series formulas can be used to calculate the total number of 4×1 multiplexers utilized to a build the n×1 multiplexer, as represented by Y in equation (2).



(a)



(b)

Figure 4. The suggested circuit for a quaternary bidirectional 16 × 1 mux. a) The rational framework b) The optimal implementation.

$$Y = \sum_{i=0}^{m-1} 4^i = \frac{4^m-1}{3} = \frac{n-1}{3} \quad .... (2)$$

The formula for the quantum value of a quaternary bidirectional n×1 multiplexer is $24\times(n-1)/3$.It generates $(3m+4n-4)/3$ trash outputs and requires $(n-1)/3$ .The previously described method can be used to merge the first quant-shift gate on every row in order to optimize the architecture. This results in four 1-qudit Shift gates per row. Furthermore, there are 4m−1 manageable Feynman gates in the first row and 4 m−2 Controlled Feynman gates in the second row.

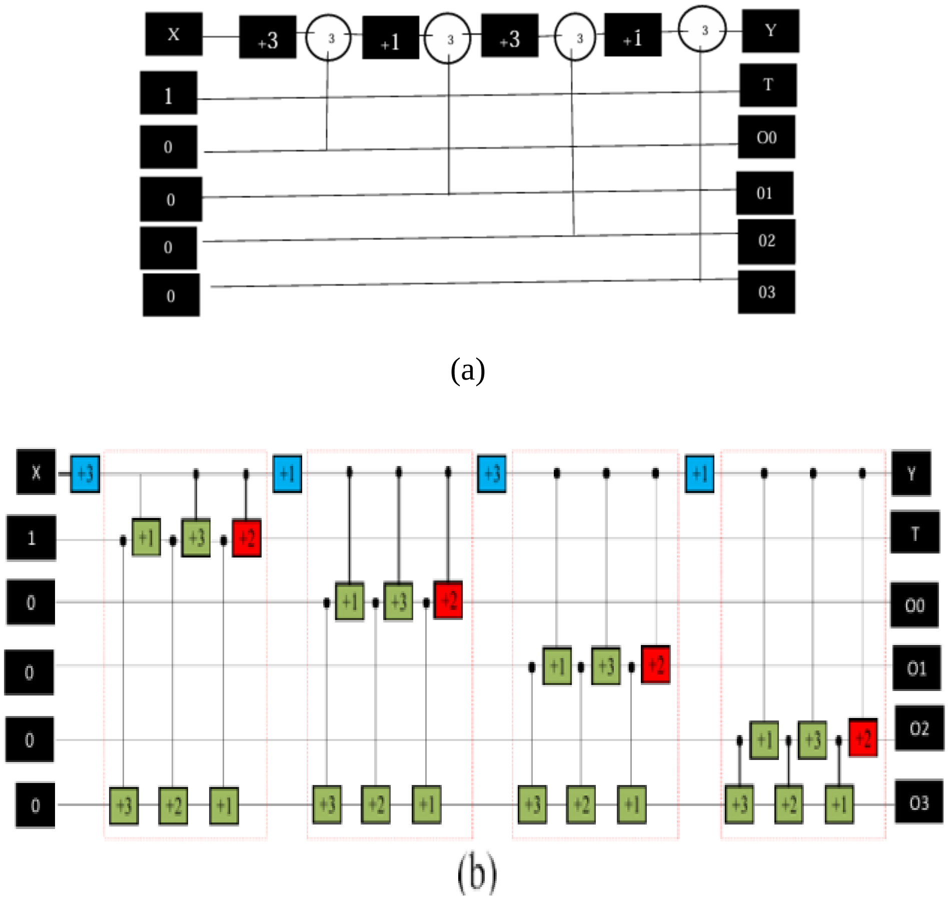


Figure 5. The suggested circuit for a quaternary bidirectional 1×4 demultiplexer. a) The sign; b)The implementation with shift gates and M-S

The improved circuit's overall quantum cost, using the 2nd version of the Controlled Feynman gate, is 20×(n−1)/3+4.

B. Proposed Quaternary Reversible Demultiplexer Circuit

A 1×16 demultiplexer can be designed by extending our suggested quaternary 1×4 demultiplexer. Two selectors, sixteen outputs, and a single input are needed for this circuit. As shown in Figure 5a, the suggested quaternary reversible 1×16 demultiplexer is constructed utilizing 1×4 demultiplexers. Five quaternary 1x4 demultiplexers are needed for this setup.

The quaternary reversible 1×4 demultiplexer circuits are indicated by the red boxes. Twenty constant inputs set to 0 are needed for the principal input, I. The output is determined by the selectors X and P, which route the signal to one of the outputs through O15. The circuit generates seven garbage outputs, designated "Y1," " Y2," "I," and "S0" to "S3," where "Y1" and "Y2" respectively stand for the selectors "X" and "P.". Twenty Shift gates in the Quaternary and 100 quaternary M-S gates make up the final design, which has a quantum cost of 120.

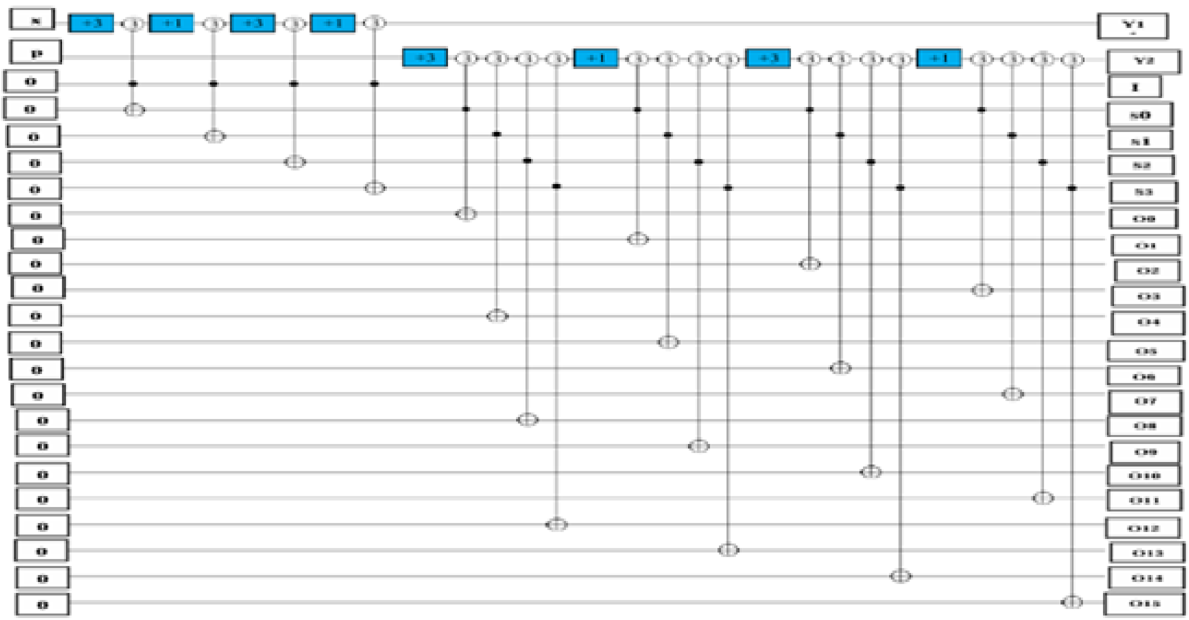
A more efficient quaternary bidirectional 1×16 demultiplexer with a lesser quantum cost is created by implementing additional gate modifications. Eight one-qudit shift gates and twenty quaternary controlled Feynman gates are included in the modified circuit, as seen in Figure 9c.

Single input, m selectors lines, and $n = 4^m$ lines of output make up this circuit. To build the circuit, m rows of 1×4 demultiplexers are typically required. Demultiplexers are arranged as follows: one in the first row, four in the second, and four in the last. The necessary number of demultiplexers, denoted as Q, can be calculated by using Equation (3). The recommended quaternary reversible 1×n demultiplexer network gives (n+3m−1)/3 trash outcomes and needs a total of 4((n−1)/3) constant inputs. This circuit's quantum cost can be computed as 24((n−1)/3). The proposed design surpasses the existing design mentioned in [23] since its values for this parameter.

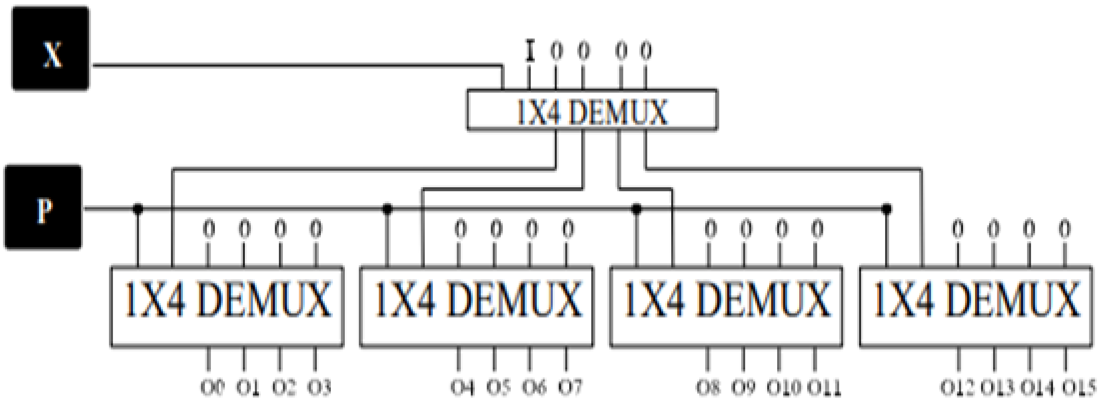
$$Q = \sum_{i=0}^{m-1} 4^i = \frac{4^m - 1}{3} = \frac{n-1}{3} \quad (3)$$

4. Results and Evaluations

The effectiveness of our suggested quaternary bidirectional multiplexer and demultiplexer circuits is assessed in this section by contrasting them with those of previous designs in [17], [19], and [23]. Quantum cost, unwanted outputs, and stable inputs are important performance parameters that are essential to the design of reversible circuits. Higher efficiency is indicated by fewer values in these metrics. Both suggested methods accomplish comparable functionality for the quaternary reversible 4x1 multiplexer, however one shows notable gains over previous designs in terms of constant inputs, garbage outputs, and quantum cost. This implies that compared to its competitors, our suggested 16x1 multiplexer is more efficient. Quaternary reversible 1x4 demultiplexer is compared to the design in [23] in Table 2. Our approach has a quantum cost of 24, which is substantially less than the 58 stated in [23], even though both uses four steady entries and produce two trash outputs. Our suggested circuits improve reversible computing efficiency by reducing quantum cost.



(a)



(b)

Figure 6: The circuit for the suggested quaternary reversible 1x16 demultiplexer. a) The representation in logic. b) The main and most efficient realization.

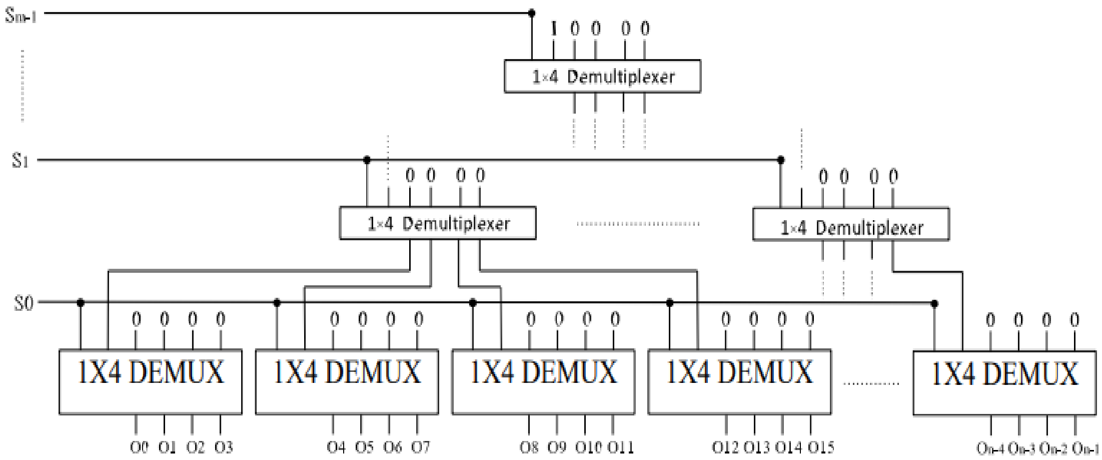


Figure 7: The proposed 1xn Demultiplexer's logical design

In this proposed system we have implemented the following parameters like Delay, Power, Total Delay Product respectively by using three different FPGA's as Spartan-6, Kintex-7, Artix-7 to get efficient values as follows from Table 1, Table 2, Table 3.

From the Table.1, the proposed technique enhances Mux and DeMux efficiency with notable improvements as Speed: Achieves 70% to 90% delay reduction for faster performance, Power Efficiency: Reduces power consumption by 20% to 65%, Resource Optimization: Cuts FPGA resource usage by up to 75%, PDP Enhancement: Boosts efficiency by up to 94.5%. These advancements demonstrate superior performance compared to existing designs.

From Table.2, The proposed method has been provided lower latency, power consumption, and the Power-latency Product (PDP).For 4×1 Mux: Produces a small power savings while reducing delays by 24% and improving PDP by 24.6%, 1×4 DeMux: Notable improvements in PDP of 60.7% and latency reduction of 59.5%, as well as lower power usage. Moderate 3.8-3.9% delay reduction, 14.3% power savings, and 8.6-17.6% PDP improvement are achieved using 16×1 Mux and 1×16 DeMux. Up to 36% PDP improvement, up to 34.7% power savings, and 31.2% latency improvement are achieved with 32×1 Mux & 1×32 DeMux. Moreover, up to 68.9% power savings and 69.5% PDP improvement, 64×1 Mux & 1×64 DeMux offer the most improvements and are therefore very effective for power sensitive FPGA applications.

From the Table.3, The proposed method from Table 3 optimizes delay, power, PDP, and resource utilization, which greatly enhances Mux/DeMux performance on Artix-7 FPGA.

Table 1: Compares various Mux/DeMux techniques on the Spartan-6 FPGA based on LUT/FF usage, delay, power consumption, and Power-Delay Product (PDP).

Spartan-6						
Size of the Mux	Technique	LUT	FF	Total Delay(ns)	Total Power (mW)	PDP(ns*mW)
4X1 Mux	[23]	4	4	9.082	40.55	368.27
	[19]	4	4	8.112	35.06	284.4
	Proposed	6	6	1.042	27.88	29.05
1X4 DeMux	[23]	16	16	9.867	36.97	364.78
	[19]	16	16	8.067	30.26	244.1
	Proposed	4	4	1.325	27.77	36.79
16X1 Mux	[23]	16	16	9.179	62.35	572.31
	[19]	16	16	8.194	62.62	513.1
	Proposed	4	4	1.869	35.66	66.64
1X16 DeMux	[23]	64	64	9.343	38.91	363.53
	[19]	64	64	9.257	39.31	363.81
	Proposed	16	16	2.735	30.86	84.4
32X1 Mux	[23]	40	40	10.908	216.79	2364.74
	[19]	40	40	13.469	118.17	1591.63
	Proposed	10	10	2.246	98.24	220.64
1X32 DeMux	[23]	128	128	9.827	130.49	1282.32
	[19]	64	64	9.406	103.9	977.28
	Proposed	32	32	1.894	88.76	168.11
64X1 Mux	[23]	84	84	12.738	337.78	4302.64
	[19]	4	4	8.112	88.82	720.5
	Proposed	21	21	2.032	116.24	236.19
1X64 DeMux	[23]	264	264	10.78	134.03	1444.84
	[19]	32	32	8.547	86.46	738.97
	Proposed	68	68	1.761	89.36	157.36

Principal Improvements: Delay: Up to 49.3% quicker, Power: Up to 78% dynamic power reduction, PDP: Down as much as 53.7%, Resource Usage: 74-75% reduction in LUTs and FFs Gains in Performance

4×1 Mux: 47.6% better PDP, 12% lower power, and 46% quicker,1×4 DeMux: 75% fewer LUTs/FFs, 64.3% power reduction, and 49.3% speed.16×1 Mux & 1×16 DeMux: 13.9–28.7% PDP gain, 75%

power savings.32×1 Mux & 1×32 DeMux: 24-43% PDP gain, 76.4-78% power savings.64×1 Mux & 1×64 DeMux: 74-75% fewer LUTs/FFs, 76.4% power cut, and the best PDP increase (53.7%).

Table 2: Compares various Mux/DeMux techniques on the Kintex-7 FPGA based on LUT/FF usage, delay, power consumption, and Power-Delay Product (PDP).

Kintex-7						
Size of the Mux	Technique	LUT	FF	Total Delay(ns)	Total Power (mW)	PDP(ns*mW)
4X1 Mux	[23]	4	4	1.601	167.44	268.07
	[19]	4	4	1.217	166.17	202.22
	Proposed	4	4	1.217	166.08	202.11
1X4 DeMux	[23]	16	16	2.879	161.8	468.73
	[19]	16	16	1.096	167.39	185.65
	Proposed	4	4	1.166	158.13	184.37
16X1 Mux	[23]	16	16	1.735	195.29	338.82
	[19]	16	16	1.735	195.35	338.93
	Proposed	4	4	1.668	167.36	279.15
1X16 DeMux	[23]	64	64	1.322	168.64	222.94
	[19]	64	64	1.322	167.37	221.26
	Proposed	16	16	1.27	160.42	203.73
32X1 Mux	[23]	40	40	2.313	270.16	624.88
	[19]	40	40	3.234	197.34	638.19
	Proposed	10	10	2.223	176.27	399.84
1X32 DeMux	[23]	128	128	1.348	220.47	297.19
	[19]	64	64	1.336	177.2	236.73
	Proposed	32	32	1.33	164.96	219.39
64X1 Mux	[23]	84	84	2.774	535.9	1486.58
	[19]	4	4	1.343	191.76	257.53
	Proposed	21	21	2.722	166.57	453
1X64 DeMux	[23]	264	264	2.027	223.12	452.26
	[19]	128	128	1.348	200.88	270.78
	Proposed	68	68	1.467	165.37	242.59

5. Conclusion

In order to minimize power, delay, and PDP, the study optimizes quaternary reversible Mux (4×1, 16×1, 32×1, 64×1) and DeMux (1×4, 1×16, 1×32, 1×64) on Artix-7 and Kintex-7 FPGAs. The suggested designs are effective for low-power digital circuits, ALUs, and quantum computing because they employ less LUTs, FFs, and PDP values.

Table 3: Compares various Mux/DeMux techniques on the Artix-7 FPGA based on LUT/FFusage, delay, power consumption, and Power-Delay Product (PDP).

Artix-7						
Size of the Mux	Technique	LUT	FF			PDP(ns*mW)
				Total	Total	
4X1 Mux	[23]	4	4	2.233	94.5	211.01
	[19]	4	4	1.207	91.66	110.63
	Proposed	4	4	1.207	91.61	110.57
1X4 DeMux	[23]	16	16	2.019	88.24	178.15
	[19]	16	16	1.092	85.89	93.79
	Proposed	4	4	1.025	83.7	85.79
16X1 Mux	[23]	16	16	1.771	125.44	222.15
	[19]	16	16	1.771	125.96	223.07
	Proposed	4	4	1.704	92.85	158.21
1X16 DeMux	[23]	64	64	1.316	95.86	126.15
	[19]	64	64	1.316	95.99	126.32
	Proposed	16	16	1.264	85.94	108.62
32X1 Mux	[23]	40	40	2.312	172.41	398.61
	[19]	40	40	3.241	128.39	114.11
	Proposed	10	10	2.222	101.86	226.86
1X32 DeMux	[23]	128	128	1.338	117.4	157.08
	[19]	64	64	1.326	106.16	140.76
	Proposed	32	32	1.32	90.41	119.34
64X1 Mux	[23]	84	84	2.752	266.28	732.8
	[19]	64	64	1.364	117.31	160.01
	Proposed	21	21	2.7	125.48	338.79
1X64 DeMux	[23]	264	264	2.017	113.97	229.87
	[19]	128	128	1.338	122.79	164.29
	Proposed	68	68	1.384	92.44	127.93

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