Communications on Applied Nonlinear Analysis
ISSN: 1074-133X
Vol 32 No. 10s (2025)

Optimized High Speed Design of Arithmetic BCD Block Utilizing Complementary MOS Process

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Article History:

Received: 12-01-2025

Revised: 15-02-2025

Accepted: 01-03-2025

Abstract: Most applications especially those in scientific computing and finance, require decimal arithmetic. Conventional binary hardware necessitates conversions between binary and decimal as well as between decimal and binary, which results in errors that cost money. Using complementary metal-oxide semiconductor (Complementary MOS) technology, the research reported here proposes decimal addition circuits.The circuits examine several BCD arithmetic unit designs and minimize errors brought on by decimal-binary conversions. Using contemporary binary adders, five distinct BCD arithmetic units—Conventional, Modified, Compact, Novel, and High-Speed 4-bit Carry Look-Ahead (CLA) architectures—are presented. The suitability of each architecture for BCD addition is assessed through comparison. The suggested circuits' functionality is simulated and confirmed using CADENCE simulator software. The performance over 45nm technology is evaluated using the metrics of power-delay product (PDP), latency, and power consumption. According on the experimental findings, the suggested decimal adder outperforms current models. The suggested adder, for instance, yields a PDP of 23.798 fJ for 4-digit operands, whereas other efforts yield 41.364 fJ, 31.137 fJ, 32.376 fJ, 49.059 fJ, and 49.882 fJ.

Keywords: — BCD arithmetic units, Complementary MOS, CLA (Carry Look-ahead Adder)

1. Introduction

Decimal accuracy is usually more than 32 digits, necessitating repeated conversions and introducing rounding errors [2], [5]. Direct decimal calculation enhances accuracy, and hardware solutions are thus more desirable [1], [6], [7]. BCD arithmetic units provide accurate decimal calculations with four-bit codes [9], [11]. A BCD arithmetic unit uses binary adders and correction logic, adding 6 for sums greater than 9 [12], [13]. Low-power and efficient Complementary MOS technology is most suitable for high-speed computing [14] – [17]. This paper designs and emulates five BCD units for 2-, 3-, 4-, and 8-digit operations, utilizing Complementary MOS benefits [18]–[20].The paper includes literature review (Section II), the suggested BCD unit (Section III), modelling and results (Section IV), and conclusions (Section V).

2.Review and Background of Literature

As illustrated in Figure 1, BCD additions of the N-digit operand are usually applied in ripple revenue construction with an N-Cascaded single-digit BCD arithmetic unit. Each of the units carries out decimal numbers, which prolongs the extended output to the subsequent stage. The N-digit BCD arithmetic unit delay linearly increases n, and nt A single digit BCD arithmetic unit carries out binary additions of the BCD code in the decimal diagram. When 9 Arithmetic Block BCD adds two that overflows or produces transmissions, we implement the alteration of (0110) to sustain legitimate BCD outputs [12] [13]. For instance, add 3 and 4 to the binary (0111) (0111). This data is correct and does not require modification. While adding 5 and 9 leads to 1110. This needs to be fixed by adding (0110) to the BCD because it is greater than 9. Similarly, adding 7 and 8 (1111) will correct for BCD (0101).

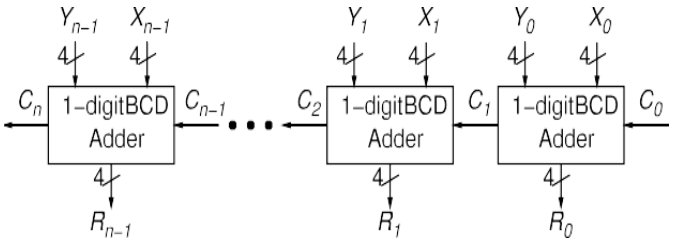


Fig 1: n-digit arithmetic BCD addition block diagram.

Proper multi-digit BCD arithmetic is provided by this method. The first adder does binary summing, and a logic gate corrects if required. Correction logic and binary arithmetic are combined in high-speed BCD arithmetic unit. There is little research on transistor-level BCD units, although there is a lot on gate-level designs [21] [22], FPGA, and ASIC implementations.

With a novel current mirror technique, the proposed voltage level shifter circuit introduces and also consists an output buffer to increases the speed and reduces consumption of power in the circuit. Table-1 shows the size of the transistors for the proposed voltage level shifter, and figure-1 shows the proposed design of the optimized voltage level shifter.

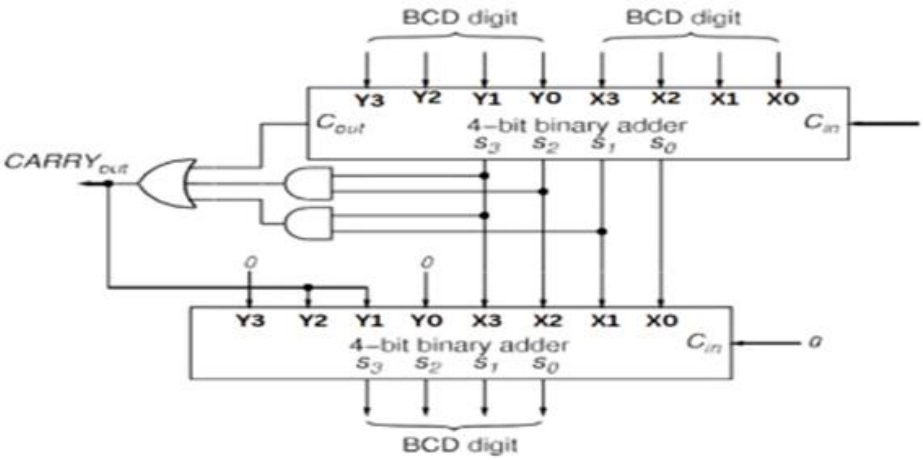


Fig 2: One – digit Conventional Arithmetic BCD arithmetic unit.

Arithmetic BCD Low-Level Units:

Dual Threshold Voltage (DVT) techniques are used in small, energy-efficient Complementary MOS BCD modules to balance speed and leakage [23], [24]. Power gating, varying channel lengths, and drowsy MOSFETs are methods used to mitigate leakage [23], [24]. Higher channels reduce leakage, but smaller channels increase speed [24]. Power dissipation is decreased by using a 32-bit adder with 14 transmission-gated transistors [25].

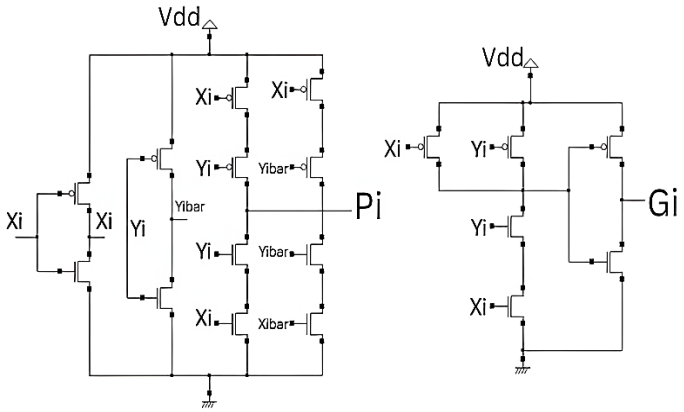
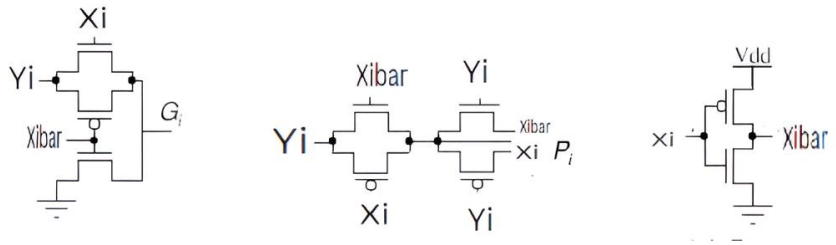


FIG 3: Pi and Gi used in Conventional 4-bit CLA



(a) AND (b) XOR (c) Inverter

FIG 4: The modified 4-bit CLA uses AND and XOR logic for Pi and Gi generation.

Binary Low Level Adders:

By reducing carry propagation time, Carry Look-Ahead (CLA) enables high-speed binary addition [26]. To lower the latency of carry generation, it includes the Propagate (P) and Generate (G) signals.

1) CLA STRUCTURE OF CONVENTIONAL 4-BIT

Conventional CLA hypotheses are described in research [27], [30], and [31]. Propagate (P) and Generate (G) signals are used by 4-bit CLA adder to perform sum and carry calculations. Their application in complementary MOS is studied.

2) CLA STRUCTURE OF MODIFIED 4-BIT

Better XOR and AND gate implementations are provided in Reference [26] (Fig. 4). In [27], gates in the enhanced CLA generate Pi and Gi signals, which are the only generational differences from the conventional CLA.

3) CLA STRUCTURE OF COMPACT 4 - BIT

A 4-bit CLA is addressed in Fig. 5 in [28], where carry generation is dependent only on Pi and Pi generation is based on the normal CLA, eliminating the need for Gi.

4) CLA STRUCTURE OF NOVEL 4 - BIT

A fresh CLA reorganization of the Pi generation in terms of NOR gates instead of XOR is shown in [29]. Using the improved logic provided by equations [1]–[5], an inverted Gi signal improves efficiencies

5) CLA STRUCTURE OF HIGH SPEED 4 - BIT

In [29], a new 4-bit CLA produces carry signals directly from Ai, Bi, and C0 in the CLA circuitry without requiring Gi and Pi signals.

3. BCD Proposed Arithmetic Chain

This subsection shows a high-speed MOS-based BCD digit adder without correction for enhanced speed. The two-level netlist (Netlist1 and Netlist2) is given in Fig. 9.The unit BCD accepts inputs X = $X_3X_2X_1X_0$ and Y = $Y_3Y_2Y_1Y_0$ with carry Cin, and X, Y ∈ [0,9]. The output is Cout and sum S ∈ {0,9}. Boolean functions (6) and (7) are given by X and Y as N = $Y_3Y_2Y_1$ and M = $X_3X_2X_1$.

$$X = (2 \times M) + X0,$$
$$Y = (2 \times N) + Y0.$$

Since A and B are both decimal numbers, $0 \le M \le 4$ and $0 \le N \le 4$ are the reasonable conclusions. Therefore, the result of the BCD arithmetic unit can be represented as follows:

$$\{Cout, sum\} = X + Y + Cin$$
$$= 2 \times (M + N) + (X0 + Y0 + Cin)$$
$$= 2 \times P + (X0 + Y0 + Cin), \quad (8)$$

P is given by (M + N) = $(P_3P_2P_1P_0)$BCD, with 2 × P from Netlist1 (Fig. 8). P_3 is the decimal carry (1 or 0), while $(P_2P_1P_0)$BCD forms the least significant bits. Since decimal even digits make the LSB 0, only P_3, P_2, P_1, and P_0 are sent to Netlist2 (Fig. 9) for the final output.For X = (0111)BCD = 7 and Y = (0100)BCD = 4, we get M = 3, N = 2, and P = 5. Thus, $2 \times P = (10)_{10}$ = (0001 0000)BCD, where $(P_2P_1P_0)$BCD = (0000)BCD and P_3 = 1. Netlist1 is implemented using Boolean logic in (9), optimizing the NAND-NAND design.

$$P_0 = \overline{A}_0 \cdot \overline{A}_1 \cdot \overline{A}_2 \cdot \overline{A}_3 \cdot \overline{A}_4 \cdot \overline{A}_5 \cdot \overline{A}_6 \cdot \overline{A}_7,$$
$$P_1 = \overline{A}_0 \cdot \overline{A}_8 \cdot \overline{A}_9 \cdot \overline{A}_{10} \cdot \overline{A}_{11} \cdot \overline{A}_{12} \cdot \overline{A}_{13} \cdot \overline{A}_7,$$
$$P_2 = \overline{A}_{14} \cdot \overline{A}_{15} \cdot \overline{A}_{16} \cdot \overline{A}_{17} \cdot \overline{A}_{18},$$
$$P_3 = \overline{A}_{19} \cdot \overline{A}_{20} \cdot \overline{A}_{21} \cdot (\overline{A}_{22} \cdot \overline{A}_{23}) \cdot \overline{A}_{24} \cdot \overline{A}_7,$$

where

A0 : = $X^{-}3X^{-}2X^{-}1Y2Y1$, A1 := $X1Y^{-}3Y^{-}2Y^{-}1$, A2 : =$X^{-}3X^{-}1Y^{-}2Y1$,
A3 := $X^{-}2X1Y2Y^{-}1$, A4 : = X2X1Y2Y1, A5 := $X2X^{-}1Y3$,
A6 : = $X3Y2Y^{-}1$, A7 := X3Y3, A8 : = $X2Y^{-}3Y^{-}2Y^{-}1$,
A9 := $X^{-}3X^{-}2Y2Y^{-}1$, A10 = $X2X^{-}1Y^{-}2Y1$, A11 := $X^{-}2X1Y^{-}2Y1$,
A12 : = X2X1Y3, A13 := X3Y2Y1, A14 : = $X^{-}3X^{-}2X^{-}1Y3$,
A15 := $X3Y^{-}3Y^{-}2Y^{-}1$, A16 : = $X2X^{-}1Y2Y^{-}1$, A17 := $X2X1Y^{-}2Y1$,
A18 : = $X^{-}2X1Y2Y1$, A19 := X2X1Y2, A20 : = $X2X^{-}1Y3$,

A21 := X2Y2Y1, A22 : = X3Y2Y¯1, A23 := X1Y3, A24 : = X3Y1.

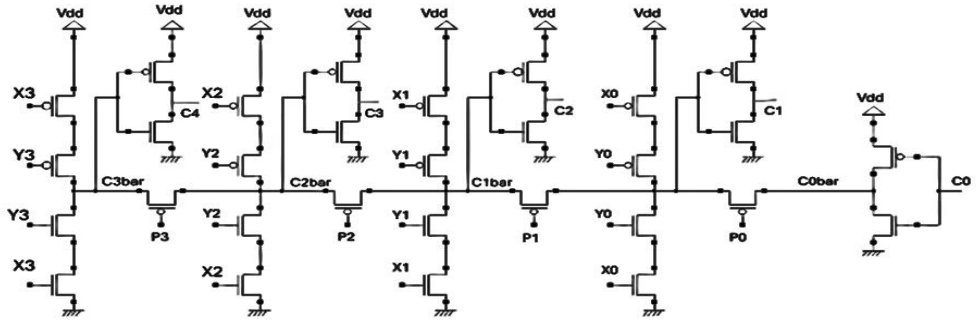
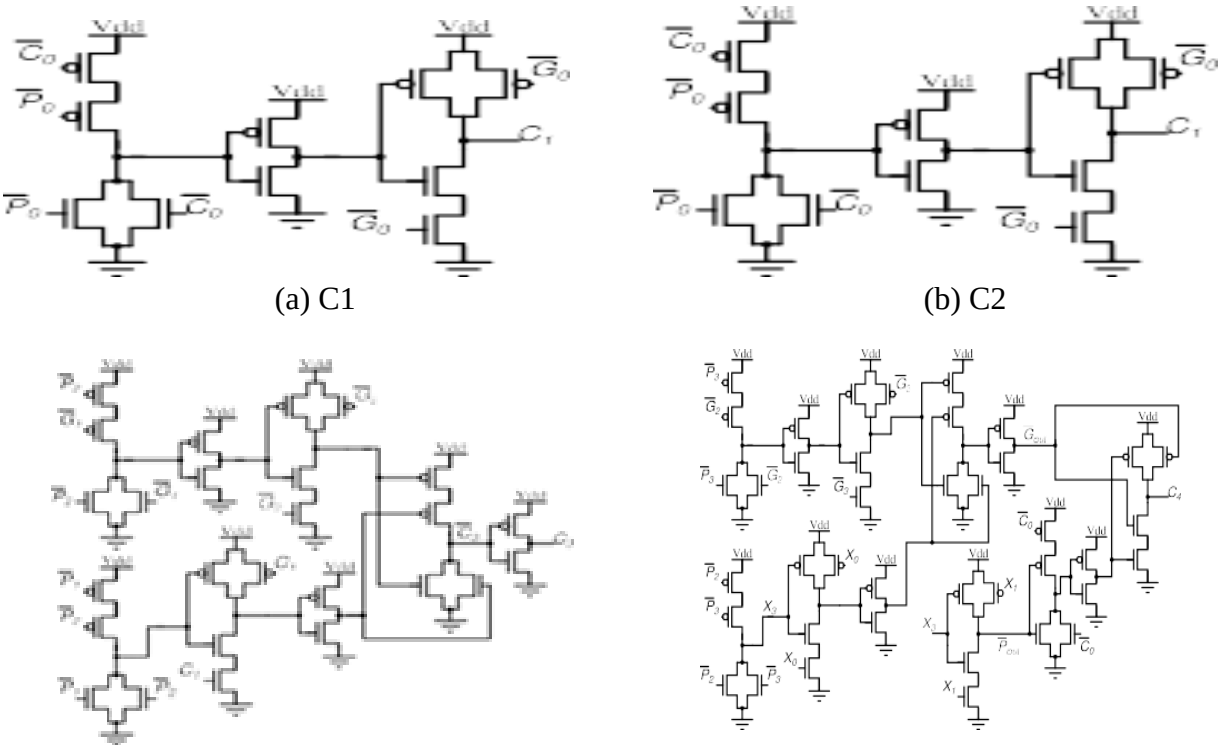


FIG 5: 4-bit circuit for Compact CLA

(a) NOR (b) NAND

FIG 6: Novel 4-bit CLA structure used both NAND and NOR circuitry



(a) C1 (b) C2

(c) C3 (d) C4

FIG 7: CLA structure for Novel 4-bit

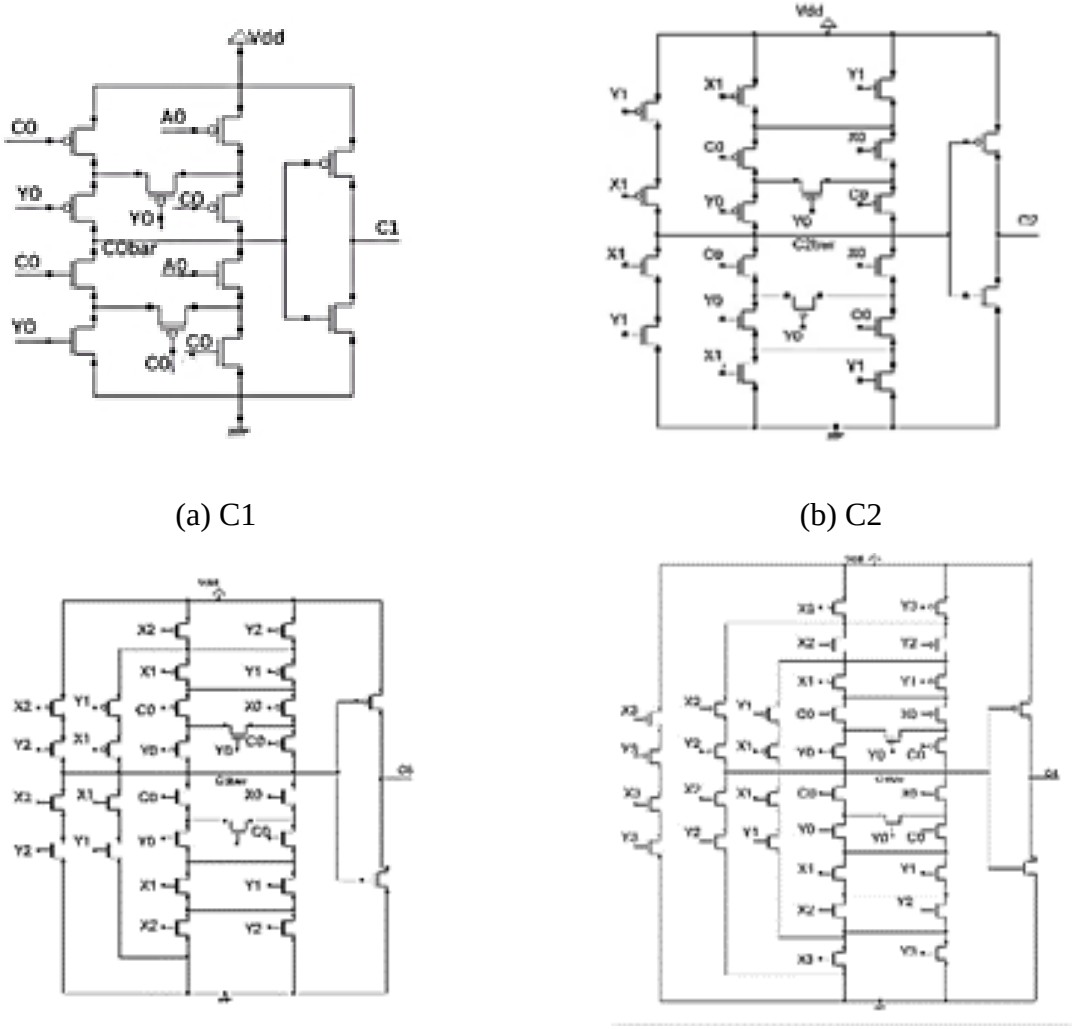


FIG 8: Generation of Carry signals in 4-bit CLA high speed structure.

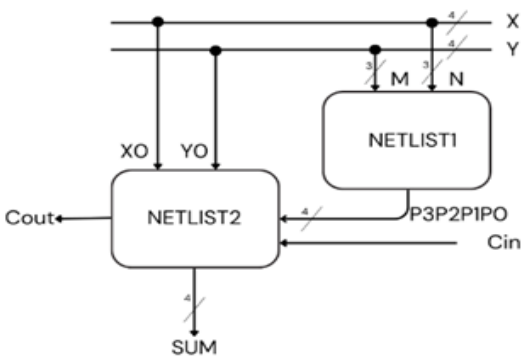


FIG 9: Block diagram of proposed BCD arithmetic unit

Fig. 10 illustrates the Netlist1 implemented using Complementary MOS. Netlist2 (P, X_0, Y_0, Cin) provides final S = ($S_3S_2S_1S_0$)BCD and carry Cout.Proper P alignment will achieve correct addition. For $P_3P_2P_1P_0$ = 1001, 2 × P = $(12)_{10}$ = (1 0010)BCD. Since X_0 = 1, Y_0 = 1, and Cin = 0, X + Y = 2 × P + (X_0 + Y_0 + Cin) = $(14)_{10}$ = (1 0100)BCD, obtaining Cout, S_3, S_2, S_1, S_0 as 1, 0, 1, 0, 0.Netlist2's NAND-NANDdesign (Fig. 11) maximizes Cout and S values through the Complementary MOS process (10).

$$S_0 = \overline{\overline{B_0} \cdot \overline{B_1} \cdot \overline{B_2} \cdot \overline{B_3}}, \quad \text{10-a}$$

$$S_1 = \overline{B_4} \cdot \overline{B_5} \cdot \overline{B_6} \cdot \overline{B_7} \cdot \overline{B_8} \cdot \overline{B_9}, \quad \text{10-b}$$

$$S_2 = \overline{\overline{B_{10}} \cdot \overline{B_{11}} \cdot \overline{B_{12}} \cdot \overline{B_{13}} \cdot \overline{B_{14}} \cdot \overline{B_{15}} \cdot \overline{B_{16}}}, \quad \text{10-c}$$

$$S_3 = \overline{\overline{B_{17}} \cdot \overline{B_{18}} \cdot \overline{B_{19}} \cdot \overline{B_{20}} \cdot \overline{B_{21}} \cdot \overline{B_{22}}}, \quad \text{10-d}$$

$$C_{out} = \overline{\overline{B_{23}} \cdot \overline{B_{24}} \cdot \overline{B_{25}} \cdot \overline{B_{26}}}, \quad \text{10-e}$$

Where

B0 : = CinX¯0Y¯0, B1 := C¯inX0Y¯0, B2 : =C¯inX¯0Y0,

B3 := CinX0Y0, B4 : = P¯2P¯0CinY0, B5 := P¯2P¯0CinX0,

B6 : = P¯2P¯0X0Y0, B7 := P0X¯0Y¯0, B8 : = P0C¯inY¯0,

B9 := P0C¯inX¯0, B10 = P¯1P0CinY0, B11 := P¯1P0CinX0,

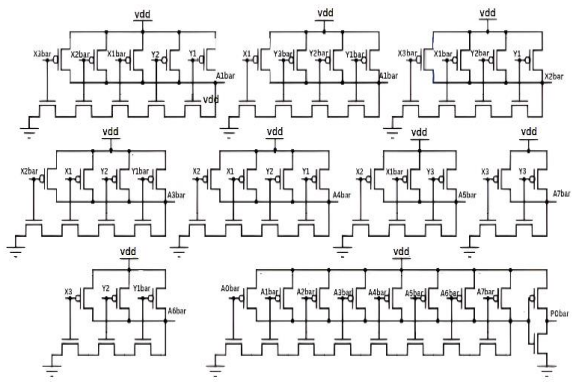
B12 : = P¯1P0X0Y0, B13 := P1C¯inY¯0, B14 : =P1C¯inX¯0,

B15 := P1X¯0Y¯0, B16 : = P1P¯0, B17 := P1P0CinY0,

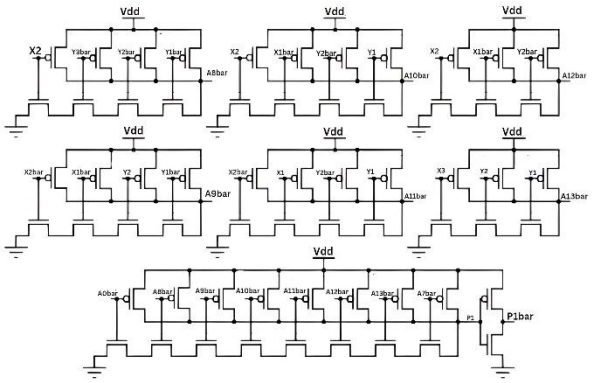
B18 : = P1P0CinX0, B19 := P1P0X0Y0, B20 : =P2C¯inY¯0,

B21 := P2C¯inX¯0, B22 : = P2X¯0Y¯0, B23 := P2CinY0,

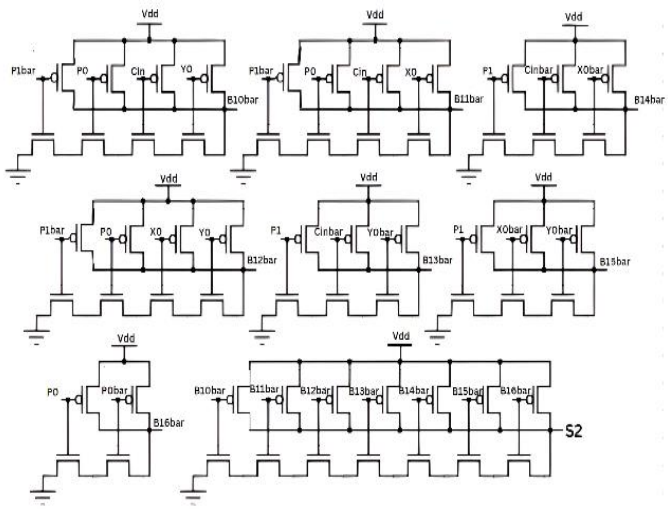
B24 : = P2CinX0, B25 := P2X0Y0, B26 : = P3.



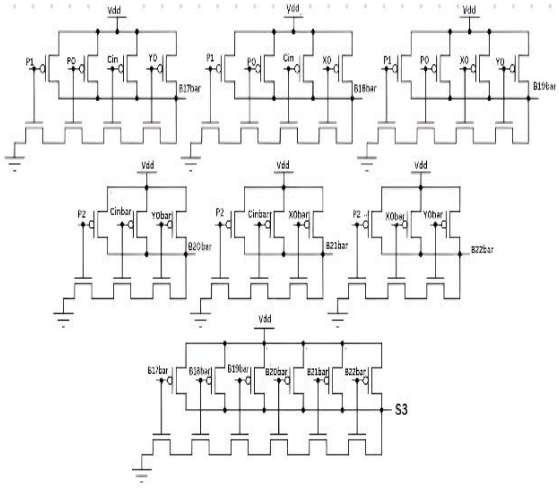
(a) Output P0



(b) Output P1

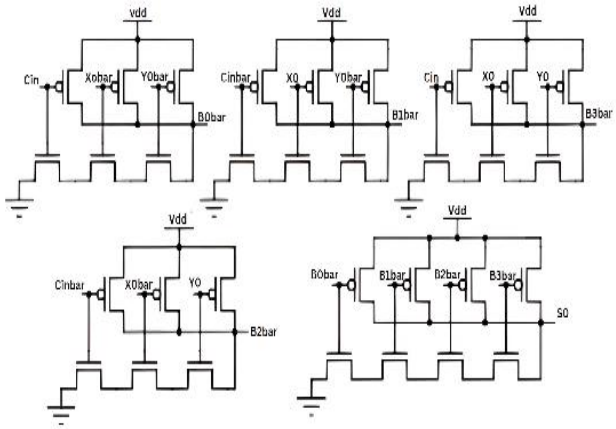


(c) Output P2

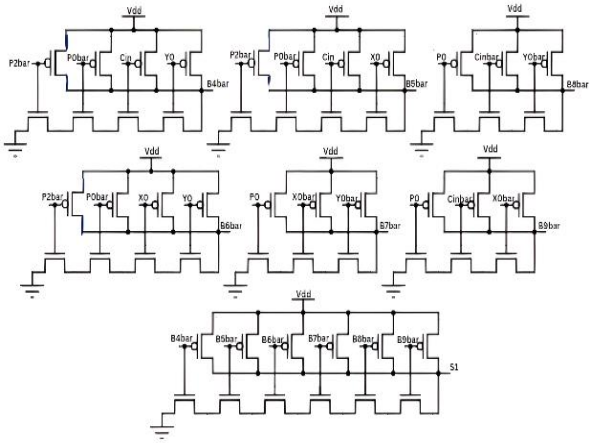


(d) Output P3

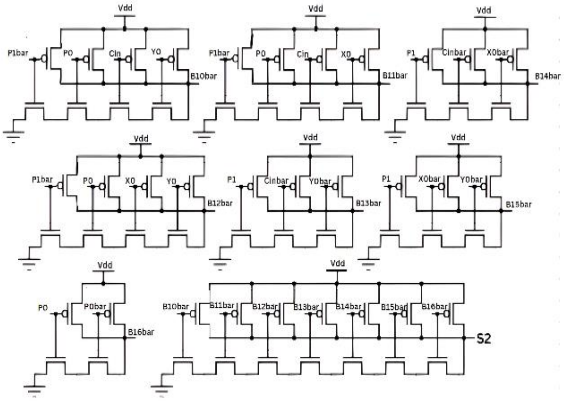
Fig 10: The proposed BCD arithmetic unit design's Netlist 1



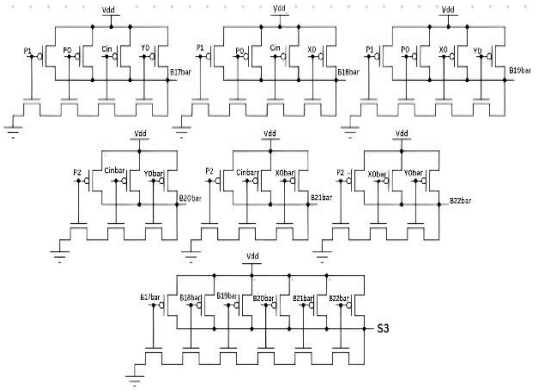
(a) Output S_0



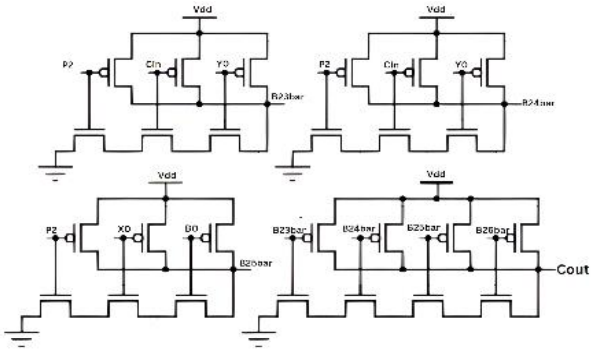
(b) Output S_1



(c) Output S_2



(d)Output S_3



(e) Output Cout

Fig 11: The proposed BCD arithmetic unit's Netlist 2.

4. Results and Analysis

For both design and simulation, the CADENCE program was utilized. The 45nm Complementary MOS Process was used to design decimal adder circuits for operands with one, two, three, four, and eight digits. At 1V and 100 MHz, transient analysis was carried out. Table 1 identifies five BCD units that are produced from different binary adders of [29], [27], and [28]. Critical latency was computed using the same method, but the 1-digit unit was scaled to larger adders.

Performance Analysis of BCD Arithmetic unit

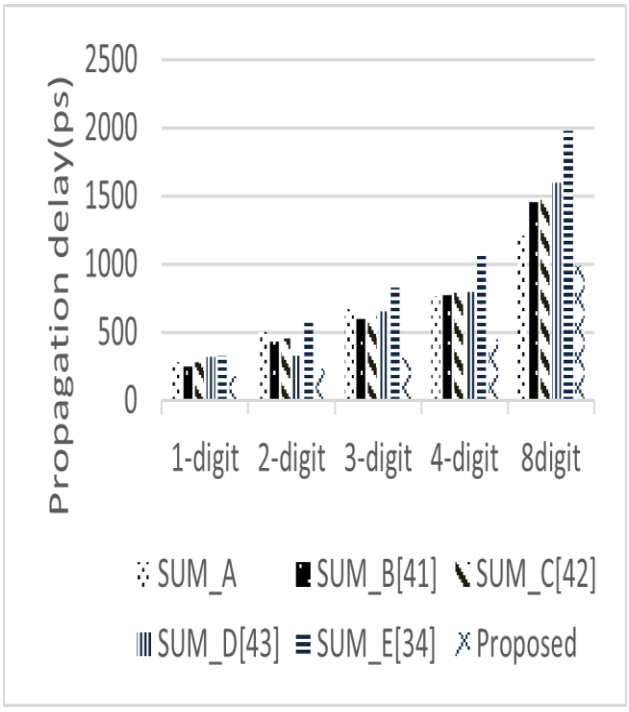


Fig 12: Propagation delay analysis includes several BCD arithmetic units for varying lengths of digits

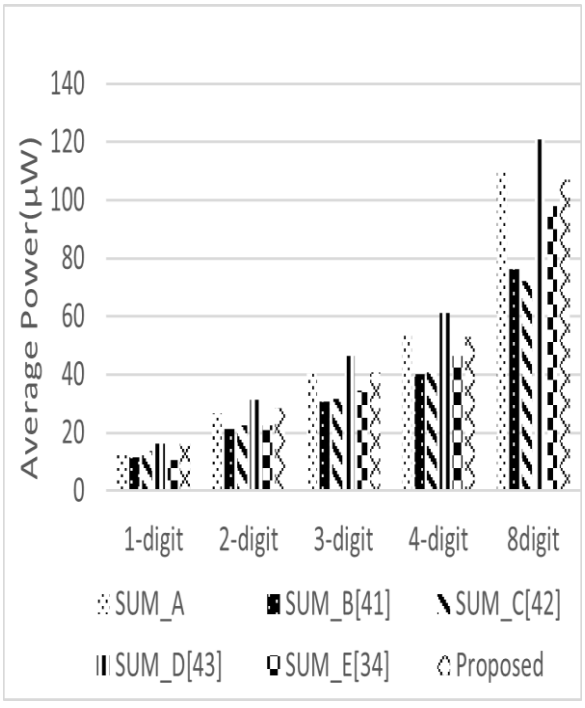


Fig 13: Comparison of Average power usage between various BCD arithmetic units of varying digit length

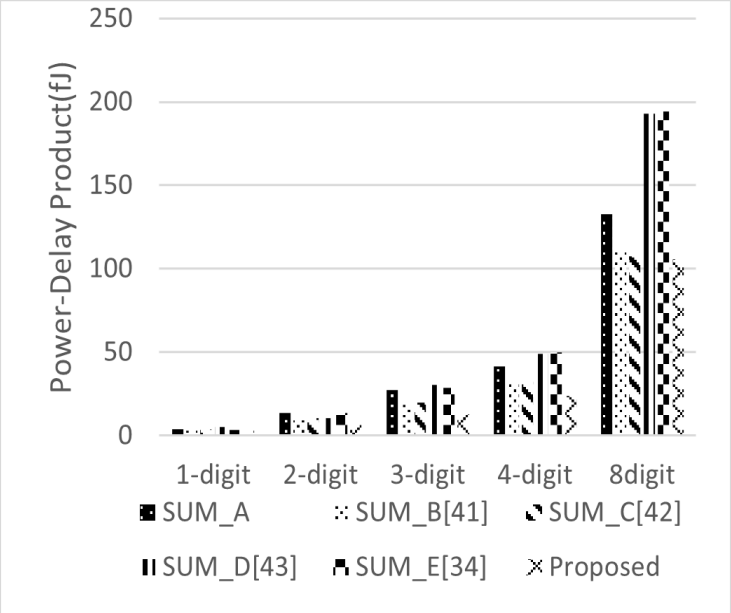


Fig 14: Power-delay Product evaluation of several BCD arithmetic units for multiple-digit length.

Signal path delays of 8-, 4-, 3-, 2-, and 1-digit decimal adders are examined. SUM-A to SUM-E delays in the 3-digit BCD unit are 672.2 ps, 600.33 ps, 624.71 ps, 658.4 ps, and 832.39 ps, whereas the proposed design realizes 316.76 ps (Table 1).Tables 2–6 and Figures 11–13 compare the proposed adder and SUM-A to SUM-E in terms of Transistor Count, Mean Power Consumption, and Power Delay Product (PDP). With a slight increase in transistor count and power consumption, it improves PDP, especially for 2-digit operands. PDP is 12.884 fJ for a 3-digit unit, which is significantly less than the competition. It uses more power than SUM-B, SUM-C, and SUM-D, but 0.6% and 12.3% less than SUM-A and SUM-E. However, it reduces delay by 52.9% to 55.2% while increasing transistor count by 6.2% to 51.5%.

TABLE 1: Results of comparisons for the 1 - digit BCD arithmetic unit

BCD arithmetic unit	Average Power (μW)	Propagation Delay(ps)	Transistor Count	Power Del. Product (fj)
Conventional	12.889	285.4	366	3.678
Modified	11.652	252.8	246	2.945
Compact	13.661	285.5	266	3.9
Novel	16.397	319.2	448	5.233
High Speed	10.531	331.5	398	3.491
Proposed	16.225	174.8	470	2.836

TABLE 2: Results of comparisons for the 2 - digit BCD arithmetic unit

BCD arithmetic unit	Average Power (μW)	Propagation Delay(ps)	Transistor Count	Power Del. Product (fj)
Conventional	26.656	501.55	732	13.369
Modified	21.204	431.95	492	9.159
Compact	22.681	455.89	532	10.34
Novel	31.378	329.5	896	10.33
High Speed	22.532	591.86	796	13.335
Proposed	28.45	230.88	940	6.568

TABLE 3: Results of comparisons for the 3 - digit BCD arithmetic unit

BCD arithmetic unit	Average Power (μW)	Propagation Delay(ps)	Transistor Count	Power Del. Product (fj)
Conventional	40.423	672.2	1098	27.172
Modified	30.756	600.33	738	18.463
Compact	31.701	624.71	798	19.803
Novel	46.359	658.4	1344	30.5
High Speed	34.533	832.39	1194	28.744
Proposed	40.675	316.76	1410	12.884

5. Conclusion

Using Cadence tools with the 45nm Complementary MOS Process, an arithmetic unit of high-speed multi-digit BCD has been developed. The design is better than existing designs by providing 8-digit BCD addition with considerable speed and efficiency improvements. Formal netlist design methodology incorporates correction logic, providing lower propagation delay and higher energy efficiency. In order to have a fair comparison, the designed adder was compared with BCD units fabricated on 180nm and 65nm Complementary MOS technology. Performance analysis reveals it maintains competitive power consumption and reduces propagation delay and power-delay product

(PDP) dramatically. While there is slightly higher transistor count in certain instances, the trade-off is worth the significant improvement in speed. The 1-, 2-, 3-, 4-, and 8-digit BCD arithmetic unit simulations validate the intended design to accommodate low-power and high-performance requirements. These results set a new standard for high-speed decimal arithmetic circuits and identify areas for further improvement in decimal computing architectures.

TABLE 4: Results of comparisons for the 4 - digit BCD arithmetic unit

BCD arithmetic unit	Average Power (μW)	Propagation Delay(ps)	Transistor Count	Power Del. Product (fj)
Conventional	54.19	763.33	1464	41.364
Modified	40.308	772.48	984	31.137
Compact	40.721	795.08	1064	32.376
Novel	61.34	799.8	1792	49.059
High Speed	46.534	1071.95	1592	49.882
Proposed	52.9	449.88	1880	23.798

TABLE 5: Results of comparisons for the 8 - digit BCD arithmetic unit

BCD arithmetic unit	Average Power (μW)	Propagation Delay(ps)	Transistor Count	Power Del. Product (fj)
Conventional	110.136	1206.39	1464	132.86
Modified	76.416	1453.96	984	111.106
Compact	72.16	1486.91	1064	107.295
Novel	120.848	1596.32	1792	192.912
High Speed	98.008	1982.65	1592	194.316
Proposed	107.004	989.58	1880	105.889

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