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Implementation of Fast, Power and Energy Efficient CMOS Flip-Flops in 45 Nm Regime

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Abstract: This paper presents the design and simulation of three novel D-flip-flops in Cadence 45nm CMOS technology. They are Implicit Pulsed Dual-Edge Triggered D Flip-Flop (IPDFF), D-Flip-Flop with Asynchronous Reset (DFFAR), and 18-transistor Single-Phase Clocked (18-TSPC) D-Flip-Flop aimed at achieving the lowest power, delay and energy efficiency in modern digital Systems. The first flip-flop is an Implicit Pulsed Dual-Edge Triggered D-Flip-Flop using CMOS VLSI pass transistor logic and dual-edge triggering for efficient clocking with reduced transistor count and leakage current thus targeting low-power, low-energy portable applications. The second flip-flop is the D-Flip Flop with Asynchronous Reset (DFFAR) that addresses power aspects while ensuring complete data integrity reliability and immediate reset capabilities. The third design, a single-phase clocked flip-flop (18-TSPC) with 18 transistors realizes high speed, optimizes power consumption and stability for compact high-performance applications. Results show that IPDFF exhibits the lowest power consumption of 0.0308µW and the lowest energy 0.0029fJ, making it highly efficient for IoT devices, embedded systems, and battery-operated electronics. DFFAR despite its higher delay of 4157ps, has exceptional low power consumption of 0.176µW making it suitable for power-sensitive applications. 18-TSPC flipflop achieves the shortest propagation delay of 5.064ps but consumes higher power of 14.16µW, making it ideal for high-speed applications like real-time processing and high-frequency computing.

Keywords: Asynchronous Reset, CMOS technology, dual edge triggering,Energy efficiency, flip flops, low power, Power Delay Product (PDP), Single-Phase Clocked (SPC).

1. Introduction

The increasing demand for power-efficient, high-speed Very LargeScale Integration (VLSI) circuits has spurred extensive research into optimizing fundamental sequential elements such as flip-flops. These elements play an essential role in digital circuits, particularly in clocking systems that contribute significantly to power consumption.

As digital systems scale to smaller technology nodes, minimizing dynamic power, leakage power, and overall energy consumption is crucial for improving performance and extending battery life in embedded systems, processors, and communication hardware.

Traditional flip-flop designs often rely on single-edge triggering, which requires high clock frequencies and results in higher switching power dissipation. To address this issue, Dual-Edge

Triggered Flip-Flops (DEFFs) have been introduced, enabling data sampling on both clock edges to lower the required clock frequency and reduce dynamic power consumption without compromising performance. However, conventional DEFF architectures are often encumbered by excessive transistor counts and increased power-delay products (PDP).

Flip-flops are integral to sequential circuit design, synchronization, and data storage. The D-Flip-Flop (DFF) is particularly important for timed storage and controlled data flow, capturing input values (D) at the clock signal's edge and holding them until the next cycle.

This paper presents the design and simulation of three novel D-flip-flops in 45nm CMOS technology. They are Implicit Pulsed Dual-Edge Triggered D-Flip-Flop (IPDFF), D Flip-Flop with Asynchronous Reset (DFFAR), and 18-transistor Single-Phase Clocked(18-TSPC) D-Flip-Flop aimed at achieving the lowest power, delay and energy efficiency(PDP) in modern digital Systems.

2. Literature Survey of Related work of CMOS Flipflops : A Critical Review

Conventional flip-flop designs often face challenges such as high dynamic power consumption, propagation delays, and excessive switching activity, rendering them inefficient for contemporary low-power needs. To overcome these challenges, researchers have investigated various low-power design strategies, including clock gating, dual-edge triggering, implicit pulsing, and pass-transistor logic (PTL). The survey identifies research gaps and highlights areas where existing designs are lacking, paving the way for the development of enhanced flip-flop architectures tailored for power-efficient VLSI circuits.

Kalarikkal Absel et.al [8] introduced a low-power dual dynamic node pulsed hybrid flip-flop that incorporates embedded logic functions to boost energy efficiency and switching performance. The researchers designed a hybrid pulsed flip-flop architecture that merges dynamic logic principles with embedded logic functionality to enhance power efficiency. The proposed design features a dual dynamic node structure that minimizes glitching effects and unnecessary transitions. Simulations demonstrated a significant improvement in energy efficiency, making it well-suited for low-power applications such as mobile processors.

Clocking power dissipation is a major contributor to energy consumption in VLSI circuits. Nagarajan et.al [9] presented an optimized register element that employs clock-gating techniques to reduce redundant switching activity in synchronous circuits. Their approach selectively disables clock signals for inactive registers, preventing power waste when data transitions remain unchanged. Simulation results revealed that the proposed register element achieved a significant reduction in switching power, making it ideal for low-power embedded systems and processors.

Timing elements are crucial for ensuring synchronization and power efficiency in sequential digital circuits. Nagarajan, Kavitha et.al [10] proposed a low-power timing element design aimed at minimizing propagation delay and dynamic power dissipation in clocking networks. Their methodology introduced clock-controlled sequential elements that optimize state transitions to reduce switching overhead while maintaining timing accuracy. Implemented using a 45nm CMOS technology node, simulations demonstrated a significant reduction in power dissipation, making it highly suitable for IoT devices, portable electronics.

Neethu Anna Sabu and K. Batri [11] proposed a dual-edge triggered flip-flop (DETFF) utilizing transmission gates (TG) to enhance energy efficiency and charge retention. Their research introduced a dual-edge clocking mechanism that allows data capture on both rising and falling clock edges, thereby reducing clock dependency and power consumption. Simulations conducted on 90nm CMOS technology showed a marked decrease in switching power and power-delay product (PDP).

Heng You et.al [12] developed a true single-phase clocked (TSPC) flip-flop that eliminates redundant precharge operations to enhance energy efficiency. Unlike traditional master-slave flip-flops that rely on dual-phase clocking, the proposed design operates with a single-phase mechanism, reducing switching losses and improving power performance. Fabricated using 65nm CMOS technology, the flip-flop demonstrated a 30% reduction in power consumption, proving its effectiveness for low-power embedded applications.

Jun Young Park et.al [13] introduced a dual change-sensing 24-transistor (24T) flip-flop designed to enhance timing efficiency by dynamically detecting necessary state changes rather than relying on continuous clocking. This design features an adaptive sensing mechanism that triggers state transitions only when an actual change occurs, preventing redundant toggling. Simulations conducted on 65nm CMOS technology demonstrated a 40% reduction in power dissipation compared to conventional flip-flops.

3. Design Methods for the three proposed CMOS flipflops

This work explores three CMOS novel flipflops which offer practical solutions for low power, high speed and energy efficiency in 45 nm technology regime and are given below.

A) Implicit Pulsed Dual Edge Triggered Flip-Flop (IPDFF)

Implicit Pulsed Dual-Edge Triggered Flip-Flop (IPDFF) uses CMOS Pass Transistor Logic (PTL). By eliminating the need for an external pulse generation circuit and leveraging implicit pulsing, the IPDFF reduces clocking overhead and complexity, resulting in lower power dissipation and improved switching speed.

B) D Flip-Flop with Asynchronous Reset (DFFAR)

The Asynchronous Reset D Flip-Flop (DFFAR) enhances its functionality by enabling immediate data reset, independent of the clock signal. This feature provides improved control over data flow in critical applications where quick data clearing is essential. The DFFAR architecture, which includes data (D), clock (CLK), and asynchronous reset inputs, ensures data integrity during clock cycles while allowing for immediate resetting.

C) 18-Transistor Single-Phase Clocked D Flip-Flop (18TSPC)

The 18-transistor Single-Phase Clocked D Flip-Flop (18-TSPC) leverages a single-phase clocking system to streamline clock distribution and significantly reduce power consumption. This design minimizes the transistor count, achieving a compact, energy-efficient structure ideal for low-power and space-constrained applications. The simplicity of its clocking mechanism ensures reduced circuit complexity, making it highly suitable for modern VLSI systems where both energy efficiency and compactness are critical.

PROPOSED FLIPFLOP1: PASS TRANSISTOR LOGIC BASED IMPLICIT PULSED – DUAL EDGE

TRIGGERED FLIPFLOP (IPDFF)

The proposed IPDFF is a low-power flip-flop circuit that implements pass transistor logic and an implicit dual-edge trigger as shown in fig.1. The 14 transistors, divided into three dynamic parts: Upper Latch (UL), Lower Latch (LL), and data selection network; comprise 6 clock-enabled transistors for the latch's sections. All these sections comprise 5 transistors with minimum active components for reduced power. Unlike conventional designs that use an external clock distribution network, the flip-flop directly applies the clock signal to the latch sections in an implicit manner, which further reduces power wastage. The data selection logic employs a simplified pass transistor design using only two N-type transistors, namely N5 and N6, thereby minimizing complexity and energy usage.

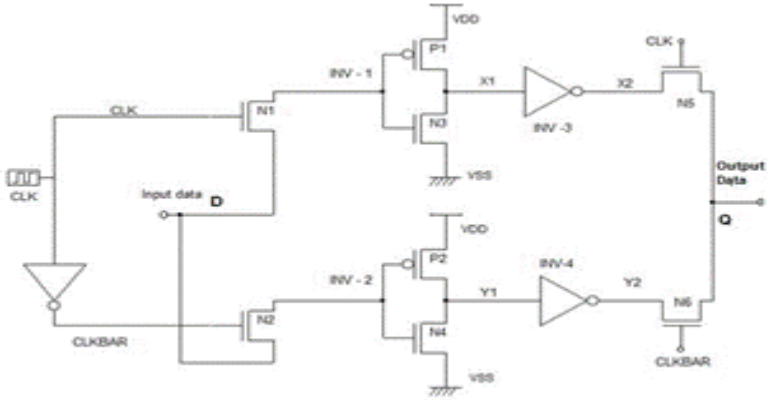

Fig. 1.Circuit of Proposed Pass Transistor Logic based ImplicitPulsed–Dual Edge Triggered Flipflop (IPDFF)

The clock signal controls the UL and LL in parallel: when CLK is high, the UL captures input data, and when CLK is low, the LL captures data. The data path also is controlled by the clock signal and its inverse, CLKBAR, so that at any time one latch section is active, while the other is idle, thus optimizing power usage. The proposed design has high efficiency as it also saves power with lower data-to-output delays which would make its applicability suitable for the low-energy domain.

UL consists of two NMOS transistors N1, N3, PMOS transistor P1, and an inverter INV-3. Input D is applied to N1. N1 is driven by the CLK signal, and when CLK = 1, N1 allows data at node X2 to be captured and passed through to N5 in the data selection network. In this circuit, the INV-3 inverter ensures data integrity before transmission to the output.

The Lower Latch consists of NMOS transistors N2, and N4, one PMOS transistor P2, and one inverter named INV-4. When CLK = 0, CLKBAR = 1, enabling N2 for conduction of data at node Y2. The data is then passed to N6, which is controlled by CLKBAR. This ensures that the value stored is available at the output Q when CLKBAR is high.

The Data Selection allows the correct latched value to be transferred to the output Q. When CLK is high, N5 turns on, allowing X2 → Q tobe passed, while when CLK is low (CLKBAR is high), N6 turns on, and Y2 → Q is passed. This parallel pass transistor selection does not use complicated transmission gates; it instead saves power and switching overheads. The circuit of

IPDFF simulated in Cadence 45nm technology is shown in fig.2 and its input and output waveforms are shown in fig.3.

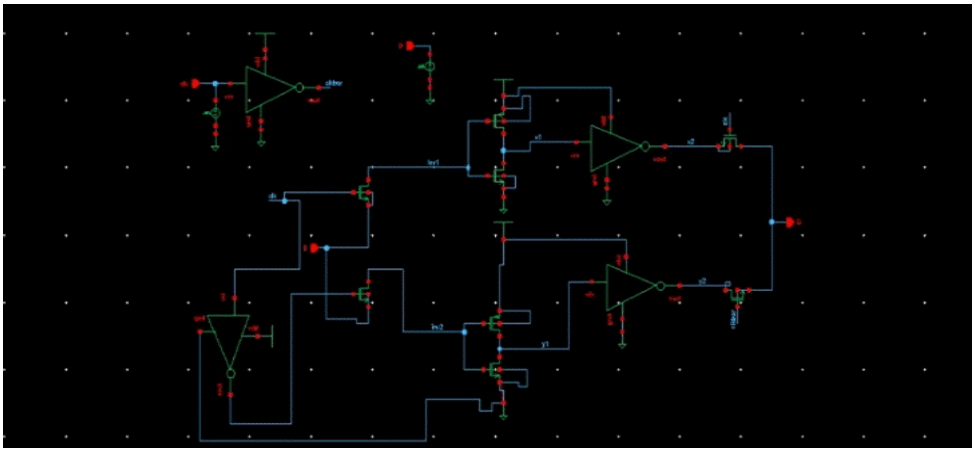

Fig. 2. Schematic of PTIP-DETFF

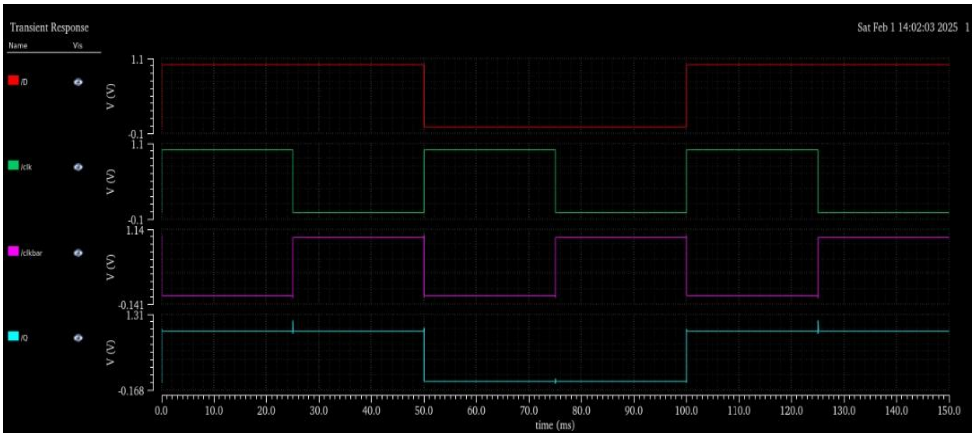

Fig 3: Input and Output Waveforms of PTIP-DETFF

The Implicit Pulsed Dual Edge Triggered Flip-Flop (IPDFF) operates by capturing data on both the rising and falling edges of the clock signal. It consists of two latching stages—Upper Latch (UL) and Lower Latch (LL) and a pass transistor-based data selection network. The functionality of the proposed PTIP-DETFF is elaborated as 4 sets of operations with the right data set of input Data D and output Q as follows

Case 1: D = 0, CLK = 0 (Falling Edge - Lower Latch Active)

When CLK = 0, the Lower Latch (LL) is activated, and N2 conducts, allowing the input D (0) to be stored at Y2. The inverter (INV-4) inverts Y2, producing Q = 0 at the output. The Upper Latch (UL) remains inactive, ensuring no unnecessary switching, thereby saving power. The pass transistor N6, controlled by CLKBAR (1), passes Y2 to the output.

Output: Q = 0

Case 2: D = 0, CLK = 1 (Rising Edge - Upper Latch Active)

When CLK transitions to 1, the Upper Latch (UL) becomes active, and N1 conducts, allowing D (0) to be stored at X2. The inverter (INV-3) inverts X2, keeping Q = 0 at the output. The Lower Latch (LL) remains inactive, ensuring minimal switching power consumption. The pass transistor N5, controlled by CLK (1), passes X2 to the output.

Output: Q = 0

Case 3: D = 1, CLK = 0 (Falling Edge - Lower Latch Active)

When CLK transitions to 0, the Lower Latch (LL) is activated, and N2 conducts, allowing D (1) to be stored at Y2. The inverter (INV-4) inverts Y2, producing Q = 1 atthe output. The Upper Latch (UL) remains inactive, ensuring efficient power usage. The pass transistor N6, controlled by CLKBAR (1), passes Y2 to the output.

Output: Q = 1

Case 4: D = 1, CLK = 1 (Rising Edge - Upper Latch Active)

When CLK transitions to 1, the Upper Latch (UL) becomes active, and N1 conducts, allowing D (1) to be stored at X2. The inverter (INV-3) inverts X2, keeping Q = 1 at the output. The Lower Latch (LL) remains inactive, ensuring low power dissipation. The pass transistor N5, controlled by CLK (1), passes X2 to the output.

Output: Q = 1

PROPOSED FLIPFLOP2: D-FLIP-FLOP WITH ASYNCHRONOUS RESET (DFFAR)

The design flow for a D Flip-Flop with Asynchronous Reset (DFFAR) in 45nm technology encompasses a series of well-defined steps aimed at achieving a functional and efficient digital component and is shown in fig.4. The process begins by establishing the functional requirements, which include defining the inputs: data (D), clock (CLK), and asynchronous reset (Reset), along with the outputs (Q and Q'). Following this, the logic circuit is designed using standard digital logic gates, specifically two 2-input NAND gates and four 3-input NAND gates, to create the internal circuitry that incorporates the asynchronous reset feature. This circuit is implemented at the transistor level using PMOS and NMOS transistors in 45nm technology, utilizing the Cadence design environment. Overall, this design flow ensures that the DFFAR is not only functional but also optimized for use in modern digital systems where rapid response and error handling are critical. The input and output wave forms of DFFAR are shown in fig.5.

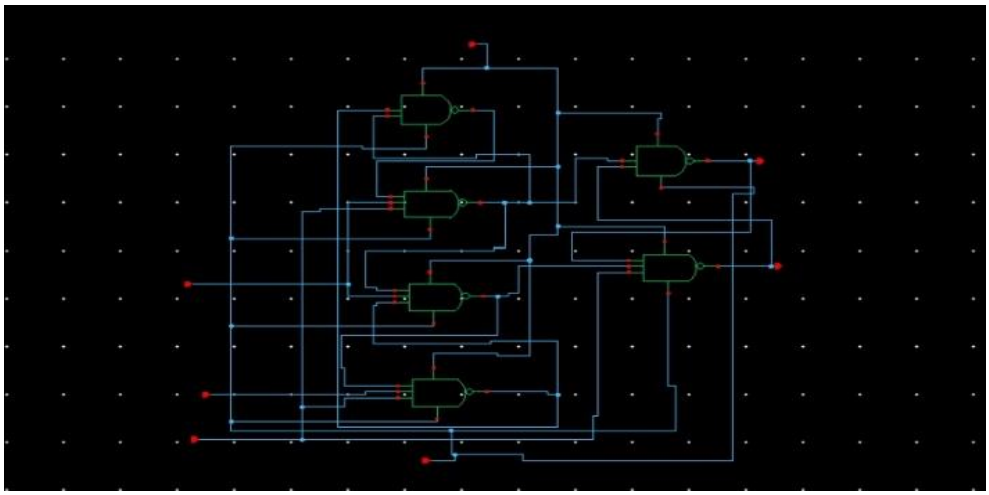

Fig. 4. Schematic of D FF with Asynchronous Reset

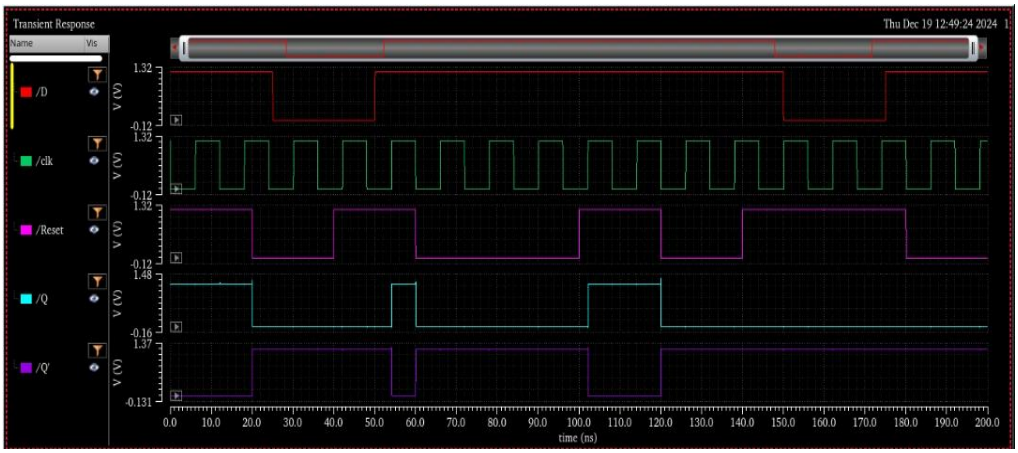

Fig .5: Input and Output Waveforms of DFFAR

PROPOSED FLIPFLOP3:18-TRANSISTOR SINGLE-PHASE CLOCKED FLIP-FLOP (18-TSPC D-FF)

The design procedure for the 18-transistor single-phase clocked flip-flop as shown in fig.6 begins by defining the key requirements, such as using a single-phase clock (Clk), minimizing the number of transistors, and ensuring low power consumption and reliable data retention. The flip-flop is divided into two stages: the master stage, which captures input data during the low clock phase, and the slave stage, which transfers the stored data to the output during the high clock phase. Clock-controlled transmission gates are implemented using complementary CMOS technology, with NMOS and PMOS transistorsworking together to pass strong logic levels. These gates are controlled by the clock signal (Clk) to enable data flow during specific phases.

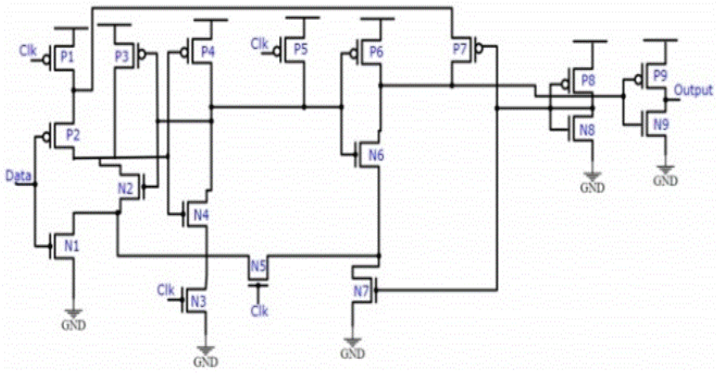

Fig. 6. Circuit of 18-TSPC D-FF

The data storage mechanism is implemented using cross-coupled inverters, forming a bistable structure that retains the stored data until updated by the clock. The master and slave stages are connected such that the master captures the input (Data) and the slave reflects the data at the output during the appropriate clock transitions. The design ensures operation using a single-phase clock without requiring a complementary signal (Clk'), simplifying clock distribution and synchronization. Transistor sizing is carefully optimized to balance speed, power consumption, and noise margins.

FUNCTIONALITY & **O**PERATION **O**F 18-TSPC D FF

The flip-flop operates in a master-slave configuration, where the master stage captures the input data (Data) during one phase of the clock, and the slave stage transfers it to the output during the other phase.

1. Low Clock Phase (Master Active): When the clock (Clk) is low, the transmission gates in the master stage are enabled, allowing the input data (Data) to propagate into the master stage. The cross-coupled inverters in the master stage store the data, while the slave stage holds its previous state.

2. High Clock Phase (Slave Active): When the clock transitions high, the transmission gates in the master stage are disabled, and the stored data is transferred from the master stage to the slave stage. The cross-coupled inverters in the slave stage maintain the data, and the output reflects the stored value.

Fig.7 shows the Schematic of 18-transistor Single-Phase Clocked D Flip-Flop simulated in Cadence 45 nm technology and Fig.8 Shows input and output waveforms of 18-TSPCD-FF.

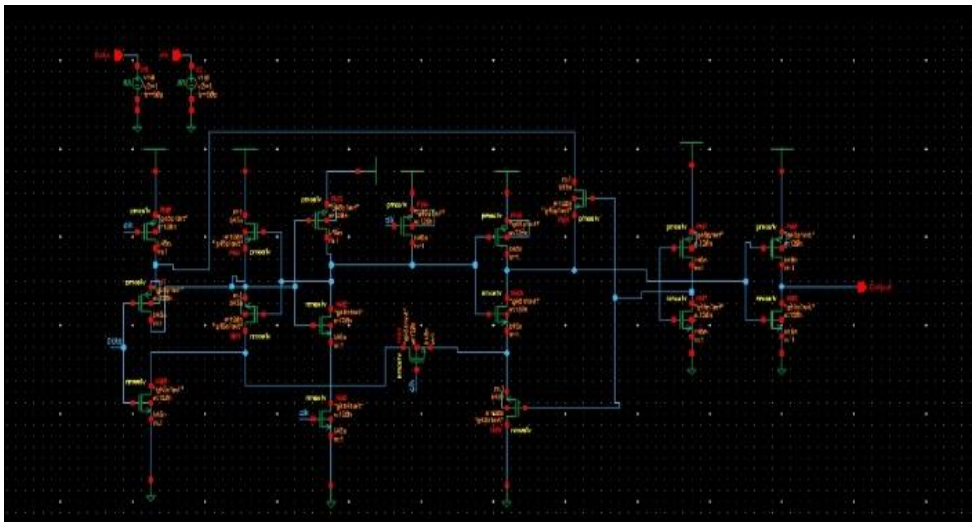

Fig. 7. Schematic of 18-transistor Single-Phase Clocked D Flip-Flop

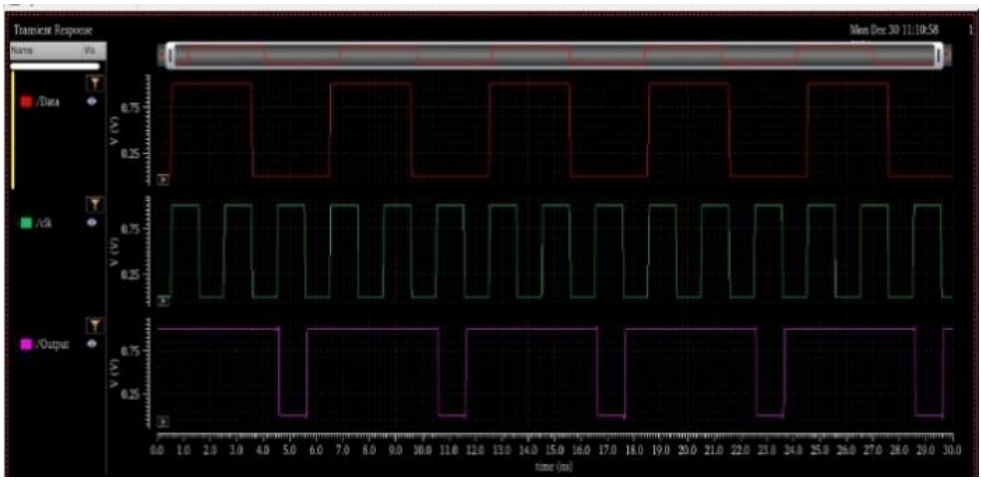

Fig. 8. Input and output waveforms of 18-TSPC D FF

4. Results of the Proposed Work

This part presents the simulation results of the proposed Implicit Pulsed Dual-Edge Triggered Flip-Flop (IPDFF), D Flip-Flop with Asynchronous Reset (DFFAR), and 18-true Single-Phase Clocked Flip-Flop (18TSPC). These designs were evaluated based on power consumption, propagation delay, transistor count, and power-delay product (PDP) or energy to assess their efficiency against conventional flip-flops. All simulations were conducted using Cadence Virtuoso with a 45nm CMOS technology node and a 1V power supply under identical test conditions.

Table1. Comparison of proposed flip-flops with existing flip-flops

Flip-Flop Design	**Transistor Count**	**Delay (ps)**	**Power (µW)**	**PDP (fJ)**
CTS-DETFF [9]	23	179	8.347	1.503
DDNET-D2[10]	14	91	7.610	0.692
S-TCRFF [11]	16	861	7.310	0.630
RTSPCFF [12]	26	77.31	8.598	0.664
DCSFF [13]	24	112.7	7.40	0.833
MS-PTDFF [14]	16	206	5.945	1.224
Proposed IPDFF	**14**	**96.83**	**0.0308**	**0.0029**
Proposed DFFAR	**32**	**4157**	**0.176**	**0.732**
Proposed 18TSPCFF	**18**	**5.064**	**14.16**	**71.71**

5. Discussions & Observations

IPDFF exhibits the lowest power consumption (0.0308 µW) and the lowest energy or PDP (0.0029 fJ), making it highly efficient for IoT devices, embedded systems, and battery-operated electronics.

DFFAR, despite its higher delay (4157 ps), has exceptional low power consumption (0.176 µW), making it suitable for power-sensitive applications where low power consumption is critical.

18TSPC flipflop achieves the shortest propagation delay (5.064 ps) but consumes higher power (14.16 µW), making it ideal for high-speed applications like real-time processing and high-frequency computing.

Fig.9, 10 and 11 show the propagation delay, power consumption and energy (PDP) graphs for the proposed three flipflops in comparison with the state of the art techniques.

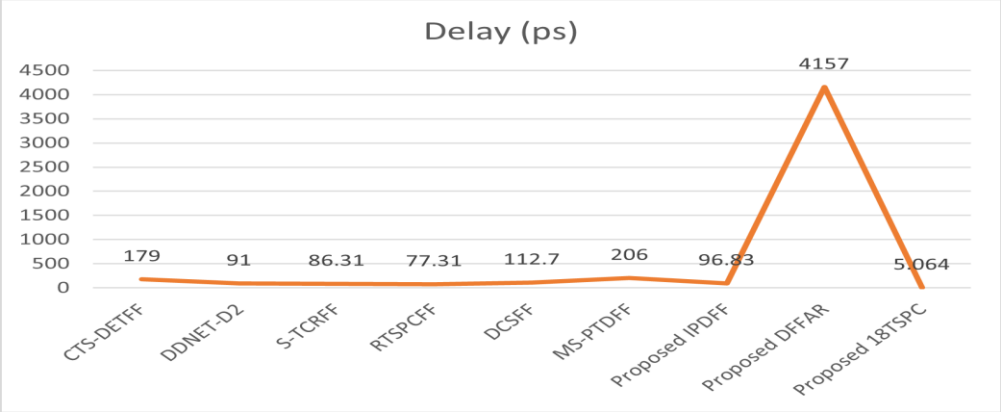

Fig.9: Comparison of Propagation Delay

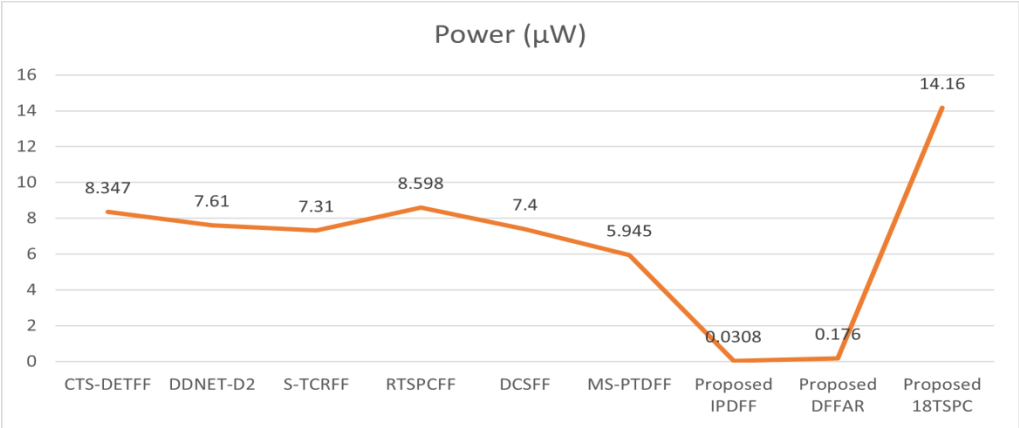

Fig.10: Comparison of Power Consumption

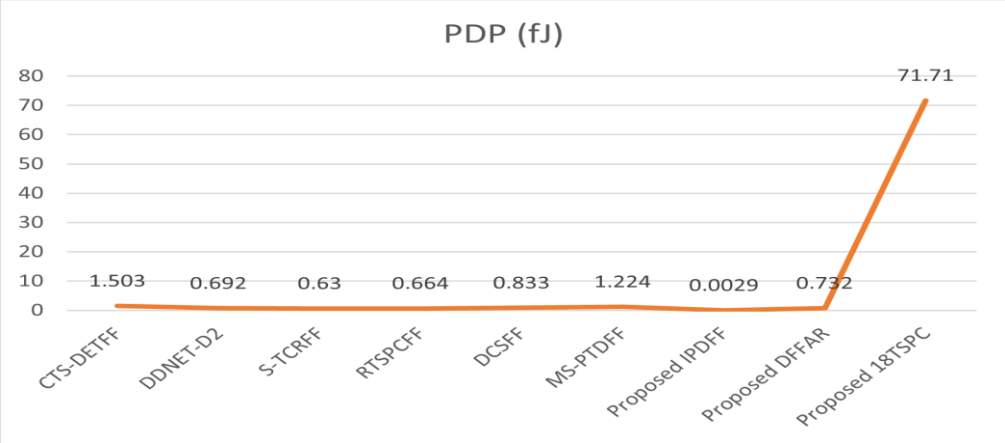

Fig.11: Comparison of energy (PDP)

6. Conclusions

This paper presents the design and detailed transistor level simulations of three novel D-flip-flops in Cadence 45nm CMOS technology. They are Implicit Pulsed Dual-Edge Triggered D Flip-Flop (IPDFF), D-Flip-Flop with Asynchronous Reset (DFFAR), and 18-transistor Single-Phase Clocked (18-TSPC) D-Flip-Flop aimed at achieving the lowest power, delay and energy efficiency in modern digital Systems. Results show that IPDFF exhibits the lowest power consumption of 0.0308µW and the lowest energy 0.0029fJ, making it highly efficient for IoT devices, embedded systems, and battery-operated electronics. DFFAR despite its higher delay of 4157ps, has exceptional low power consumption of 0.176µW making it suitable for power-sensitive applications. 18-TSPC flipflop achieves the shortest propagation delay of 5.064ps making it ideal for high-speed applications like real-time processing and high-frequency computing. Further there is a future scope to study these designs with process, voltage and temperature variations regarding performance and may build a variation resilient design in nanometer technology.

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