Communications on Applied Nonlinear Analysis
ISSN: 1074-133X
Vol 32 No. 10s (2025)

Pseudo CMOS Logic Indium Tin Oxide Thin Film Transistor ZnO for Transparent Electronics

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Article History:

Received: 12-01-2025

Revised: 15-02-2025

Accepted: 01-03-2025

Abstract: In this study, Pseudo-CMOS digital circuits were implemented and investigated using n-type indium tin oxide stabilized ‘ZnO’ thin film transistors (TFTs). The optical transmittance of the circuit varies between 78% and 91% along the light path. The operating frequency of the circuit was found to be greater than 10 kHz at a supply voltage of 9 to10 V. This inverter produced a maximum latency of 4 µs at a nominal voltage of 10 V and VDS = 0.5 V. The delay of the circuit is 1.78 micro sec. and the power/energy is 0. 385nJ.This results gives the advantage of the reduction of the 70% energy or power.

Switching transistor circuits with logic have been developed shaped on “n-type indium tin oxide” (ITO) “ZnO” thin film transistor ("TFT") technology. The logic oscillation of electronic devices with pure n-type ‘TFT’ transistor logic circuits are discussed in detail to expand the characteristics of the systems. In order to accomplish better performance, the performance of various "OR" operations, control logic comparison style, and better speed and smaller area are adopted. All circuits are completed of transparent glass sheets.

Keywords: Pseudo CMOS logic, ITO-Stabilized ZnO ‘TFT’.

1. Introduction

‘ZnO’ is a semiconductor material with ionicity between covalent semiconductor and ionic semiconductor. The global value of the “highest valence band” of n-type semiconductor materials coincides with the global extreme value of the “lowest conduction band”, ‘ZnO’ is a direct conductor with n-type conductivity.

For n-type doping of ‘ZnO’, “Group III” elements are Al, Ga, In replace Zn or “Group VII” elements are Cl , I replace O in the ‘ZnO’ crystal structure. When the raw material is exposed to light, instabilities occur during operation, which reduces the production costs compared to photosensitizer materials. Electrical conduction in ‘ZnO’ materials can be separated into (I) electrical conduction under low voltage and (II) electrical conduction under high voltage. For high voltage environments, “Monte Carlo simulations” used to calculate the velocities and electrical properties of bulk ‘ZnO’. The mobility is determined only by the breakdown process and has nothing to do with energy consumption hot. Crystal orientation and defects cause the number of carriers to decrease at room temperature.These high voltages are not fully functional during equipment operation; however, the performance of TFT, a low-cost material for metal-semiconductor contacts, is exaggerated by the interference between the “drain/source” electrodes and the semiconductor process. Electrical & electronic components are important in determining whether it is a power surge or an injection. Carrier injection depends on the location of the “Fermi level” of the material relative to the valence/conduction bands of the inorganic semiconductor.

The theory of metal semiconductors is very broad, the contact between metal and n-type materials and the effects and nonlinearities that affect the TFT performance. The material used for flow and electrode mixing is metal because it can increase the current rate of the device and reduce the junction resistance of changed transistors, which is a requirement of circuit mixing [7].

2. Operation and Analysis TFT

Semiconductor materials can also cause the TFT behavior to be unstable and poor.

Indeed, the thickness of this layer depends on the control of the electric field. The semiconductor process affecting the unpackaged inverse transistors & gate electrode can be affected by the contact with other materials.

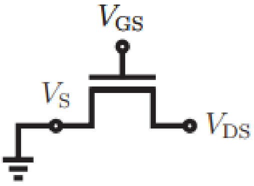

Figure 1: Equivalent circuit of ideal TFT

The total layer thickness effect modeled as a “capacitance” in series with the “gate” dielectric capacitance.

The “Effective Gate Capacitance” (CG) decreases as follows:

$$c_g = \frac{c_{ins} c_{sem}}{c_{ins} + c_{sem}}$$

where

c_{ins}=The Gate Insulator per unit area capacitance

The “parallel plate capacitor” modeled are

$$c_{ins} = \frac{\epsilon_{ins} \epsilon_0}{t_{ins}}$$

‘ϵ_0’= The “permittivity” of the “vacuum”.

‘ϵ_{ins}’= The “permittivity” of the “insulator”.

‘t_{ins}’= The “thickness” of the “insulator”.

The rate of change of the junction process and the potential drop in electronic components depend on the properties of the semiconductor material.

The “capacitance” of “semiconductor per unit area” (c_{sem}) are determined the

$$c_{sem} = \int_{t_{int}}^{t_{sem}} \frac{q\Delta n(y)}{v(y)} dy$$

Where

‘$q\Delta n(y)$’= Accumulation layer “Induced charge carrier density”.

‘$v(y)$’= Semiconductor voltage drop .

‘t_{int}’=Semiconductor/gate dielectric interface

‘t_{sem}’=Semiconducting layer thickness

3. Simulation with “ITO-ZnO- TFT”

Figure 2 shows the conversion of “ITO-ZnO-TFT” with ‘100 μm’ channel width and ‘10 μm’ channel length. A typical device transfer η is 18.4 cm^2/V.s, threshold voltage is close to 0.7 V, ON/OFF ratio is greater than 10^{10} and low pass filter is 10^{10} mV/decimal. The performance of TFTs is largely due to the composite material in the “ITO-ZnO-channel”.

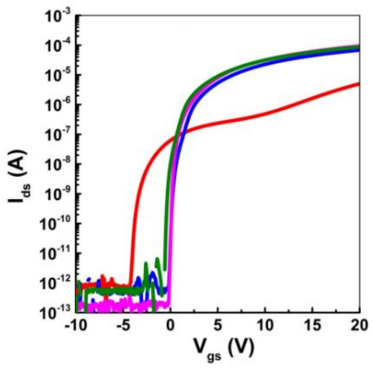

Fig. 2. The “ITO-ZnO- TFT” transfer characteristics.

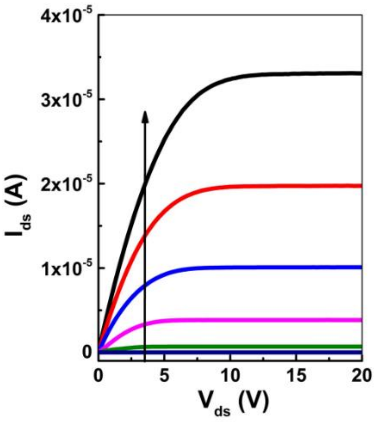

Figure 3:“ITO-ZnO- TFTs” Output plot

The problems such as high power consumption and unstable operation are often experienced in diode-load inverters. In contrast, a zero-Vgs inverter uses very little power because the pull-up transistor is always off. However, it is not easy to provide sufficient driving capacity by paying for the load capacity, and low efficiency occurs. Recently, demonstrate a “pseudo-CMOS inverter” as shown in Figure 3.

4. Results of Pseudo-CMOS ITO-stabilized ‘ZnO’ TFT

It has some advantages over traditional power supply models. It is used in unipolar ‘TFT’ circuit designs. More than “two transistors” are used, the circuit requirements to be complete more “complex” and the “speed” of the circuit is slower than the diode-loaded logic.V_{SS} must be higher than V_{DD} + $2V_T$

to ensure power balance with V_{DD} [13]. The large power loss is another important factor that is inevitable.

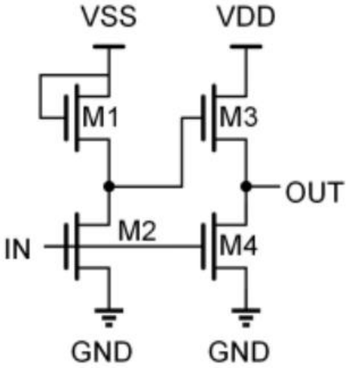

Fig. 4. Pseudo-CMOS (a) inverter

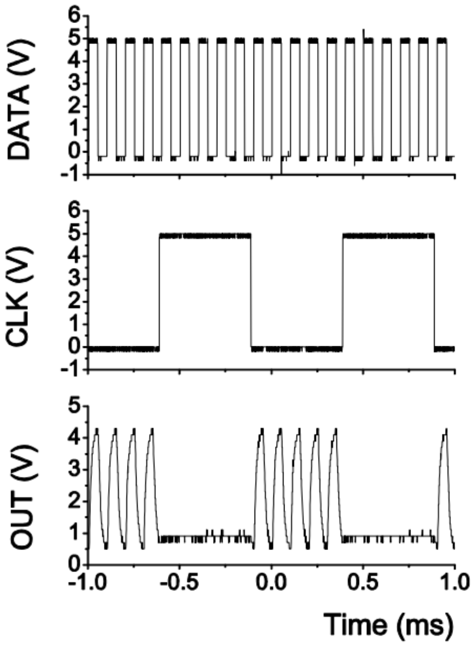

Figure 5:Output waveform of Pseudo-CMOS ITO-stabilized 'ZnO' TFT

Pseudo-CMOS logic is used and VSS is set to 2VDD for simplicity. In this study, the channel width (W) of M1-M4 for the inverter is 30, 170, 170 and 170 µm, respectively.

Fig.5 show the measured values of the inverter at VDD = 5 V and VSS = 10 V. The input signal frequency for the gate is 10 kHz. Input signals frequency 'DATA' & 'CLK' is 10-1 kHz respectively. The frequency of the I/P signals 'DATA' & 'CLK' is 5-10 kHz, respectively. The correct value of the "high level" of '4.3 V' and a "low level" of '500 mV' for all logic circuits. Most of the drop in output fluctuate is due to the 1 MΩ resistive load. The distortion at input frequencies up to 10 kHz in the output waveform presented in all the circuits. Therefore, it has been determined that these circuits can operate at frequencies above 10 kHz. This superior performance is mainly due to the mobility of the mixed-phase "ITO-ZnO" active layer.

Table I: Value of n-type indium tin oxide (ITO)-stable ZnO thin film transistor Design

Design	Supply voltage	Process	Delay	Power/Energy
Pseudo CMOS Inverter	10 V	ITO-ZnO- TFT	1.78micro sec.	0.385nJ

Conclusions

In this work, a transparent pseudo-CMOS inverter based on “ITO-ZnO-TFTs” is introduced. All simple digital circuits have operating frequencies greater than “10 kHz” with a “supply voltage” of “10 V”. The results show that the proposed circuit for transparent electronic devices requiring transitional performance, such as driving in transparent films.

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