A High-Efficiency Hybrid Resonant Converter with 2:1 Conversion Ratio and Inductor Bypass for Loss Reduction

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ABSTRACT

Fully integrated power management is crucial for many applications but has been proven to be challenging due to the limitations of passive components. This paper introduces a voltage regulator that uses an on-chip LC resonator to reduce the number of off-chip passive components. When integrated on-chip, the inductors interact with internal capacitors, causing trapezoidal ringing and power loss during off-time. To address these problems, a simple bypass scheme was proposed and added to the *LC* tank. As a result, the bypass scheme helped achieve at least 5% higher efficiency compared to a converter without an inductor bypass. The proposed design implemented in the 180 nm CMOS process occupies a chip area of 2.88 mm^2, and the voltage regulator achieved an efficiency of 95% at 2.4 V input voltage, with a peak efficiency of 89% in closed-loop utilization. Furthermore, the light-load efficiency was extended using Off-Time Modulation (OTM), resulting in a minimal under/overshoot of less than 100 mV during output load transients ranging from 6-105 mA/80 ns.

Keywords-anti-ringing; DC-DC converter; resonant converters; voltage regulator; switched-capacitor

I. INTRODUCTION

Recent advances in semiconductor scaling have revolutionized low-power management designs, particularly for IoT and biomedical applications [1-5]. Efficient DC-DC converters are indispensable in these domains, providing stable voltages to maximize performance, extend battery life, and enable seamless integration with modern electronics [6, 7]. The push for compact and high-efficiency on-chip DC-DC solutions is critical for implantable and IoT devices, where portability and area constraints demand miniaturization [8, 9]. Traditional buck converters, although effective for wide output voltage ranges, struggle with on-chip integration due to bulky inductors [10]. Recent advances, such as air-core inductors [11,12] and on-die MIM capacitors [13], improve the transient response but compromise quality factors and area efficiency [14]. Switching-based control also introduces voltage/current ripples, which are typically mitigated by larger *LC* filters, a trade-off incompatible with area-constrained systems. Higher switching frequencies reduce ripple but exacerbate power dissipation and node ringing from parasitic capacitances, reducing reliability [15-18].

Recent hybrid converter designs have sought to address these challenges through soft-switching techniques and resonant topologies to reduce switching losses and electromagnetic interference. For instance, soft-switching methods such as Zero-Voltage Switching (ZVS) and Zero-Current Switching (ZCS) [19-22] have been integrated with buck-derived architectures to improve efficiency. Additionally, high-frequency operation (enabled by advances in semiconductor materials and switching devices) has been explored to shrink passive components, although this often amplifies node ringing and control complexity [15-17]. Wide-Bandgap (WBG) devices, such as GaN and SiC, have further pushed the efficiency boundaries in hybrid converters by enabling faster switching with lower conduction losses [23, 24]. However, these approaches still face critical limitations: soft-switching implementations often require auxiliary circuits

(e.g., snubbers, active clamps) that increase design complexity [20-22] while WBG-based designs struggle with parasitic oscillations and gate-drive challenges at ultra-high frequencies [17, 18]. Moreover, existing hybrid topologies frequently prioritize either efficiency or miniaturization, failing to holistically address area overhead, transient response, and reliability in deeply scaled CMOS processes. Although previous studies have demonstrated progress in hybrid converters, key gaps remain. First, soft-switching and resonant techniques often rely on external damping components or complex control schemes, affecting their suitability for fully integrated designs [25]. Second, high-frequency operation with WBG devices introduces node ringing and overvoltage stresses that degrade reliability in resource-constrained systems [26]. Third, existing solutions do not adequately balance efficiency, area, and transient performance, a critical requirement for IoT and biomedical applications where load currents vary dynamically [27].

This paper proposes a novel hybrid resonant converter that addresses these problems with: (i) a topology integrating NMOS switching and inductor bypassing to allow soft switching without auxiliary circuits, eliminating node ringing via intrinsic *LC* resonance, (ii) a self-damping mechanism that suppresses oscillations during off-states, reducing conduction loss and voltage stress, and (iii) Off-Time Modulation (OTM) for extended light-load efficiency and rapid transient response. Unlike previous hybrid designs, this architecture achieves compact on-chip integration by obviating snubbers, sensors, and complex gate drivers, while maintaining compatibility with standard CMOS processes. Implemented in 180 nm CMOS, the converter achieves 95% peak efficiency at 2.4 V input and 89% closed-loop efficiency, with less than 100 mV under/overshoot during 6-105 mA load transients of 80 ns. These metrics address the limitations of previous hybrid converters, offering a unified solution for applications demanding miniaturization, reliability, and dynamic performance, from neural implants, where suppressed ringing enhances safety, to edge AI processors, where OTM sustains efficiency across sleep-active cycles. By resolving trade-offs between area, efficiency, and control complexity, this work advances the frontier of on-chip power management for next-generation electronics.

II. DESIGN

Figure 1 shows the schematic of the proposed converter, circuit, and voltage current waveforms. The circuit comprises two separate gate driver schemes for dual-phase operation connected to a Voltage Control Oscillator (VCO), an Operational Transconductance Amplifier (OTA), and a switched capacitor power stage that interfaces with the merged *LC* resonator. The power stage switches only use NMOS exclusively with a feedback loop, controlled by the VCO and OTA, to manage the switching time and maintain regulation during transients. The phases are symmetrically arranged 180° out of phase to optimize the use of bypass capacitance while lowering the voltage ripple. With symmetric two-phase interleaving, significant output voltage ripple reduction is achieved, as low as one-fifth compared to a single-phase design with the same bypass capacitance. If the same ripple is to be maintained, it allows the converter to be reduced in size due to a substantial decrease in the bypass capacitance, down to five times less than what a single-phase design would require.

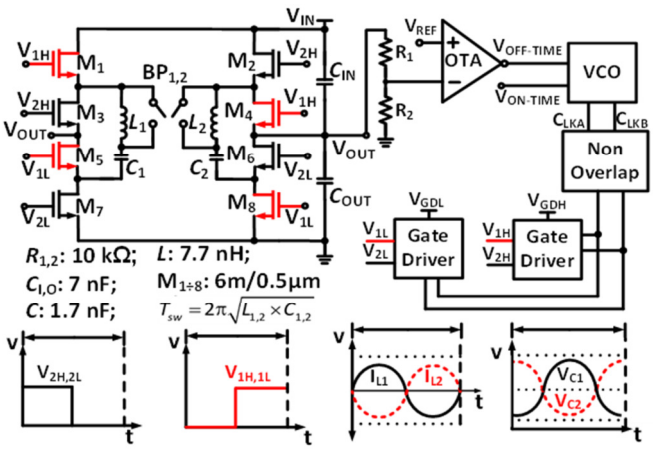


Fig. 1. Overview of the converter and voltage current waveforms.

However, it is noteworthy that there is a trade-off, as coupling capacitance between interleaving phases creates losses. This effect can become greatly problematic with higher voltage swings and high switching frequency, which should be considered when using interleaving phases. To reduce the output ripple during operation, equal bypass capacitances (C_{IN}, C_{OUT}) are used and implemented off-chip, leading to symmetrical switching phases, provided that the resonant frequencies are also equal. Moreover, C_{IN} and C_{OUT} help cancel the current spike at the start of the operation without needing more bypass capacitance. As shown in Figure 1, using the interleaved operation creates currents that fluctuate over time in sync but in reverse polarities. This arrangement allows for the coupling of magnetic fields and yields a higher inductance with the same space needed by the self-inductances of each phase. Therefore, consolidating inductors into one construct reduces the operating frequency and improves the overall efficiency and power density.

Regarding the operation of the switch-cap resonant power stage of the converter in Figure 1, since the power stage operates in interleaving phases, when the control voltage signal $V_{1H,1L}$ is at a high level, the power CMOS transistors $M_{1,5}$ are turned on, charging the resonant tank on the left side L_1 and C_1. Simultaneously, when the control voltage signal $V_{2H,2L}$ is at a low level, the power CMOS transistors $M_{2,6}$ are turned off, and as a result, L_2 and C_2 of the resonant tank on the right side will be discharged as output voltage (V_{OUT}), supplying the Load. From the above observations, it can be concluded that increasing the charge rate and decreasing the discharge rate of the *LC* resonant tanks will increase V_{OUT}, and increasing the discharge rate while lowering the charge rate of the resonant tank will decrease V_{OUT}. Thus, the charge and discharge rates of the power stage can be said to be controlled by the On-time (t_{ON}) and Off-time (t_{OFF}) of each individual phase. During the off-state, L_1, C_1 and L_2, C_2 are coupled, causing the *LC* tank to oscillate dissipating energy stored inside the inductors and capacitors themselves; therefore, in the next on-state, V_{OUT} will be reduced, subsequently leading to a decrease in efficiency,

increased output ripple, and forcing the converter to operate with a greater duty cycle, reducing t_{OFF} to compensate for a diminishing output voltage. To address this issue, a simple inductor bypass scheme is also employed to mitigate the ringing noise caused by the *LC* resonator. Two power switches are placed to provide a path for the current when the converter enters t_{OFF}, as shown in Figure 2. Each switch is controlled by a NOR logic gate so that when both control clock signals are absent, the inductor and capacitor are no longer coupled, helping to minimize the *LC* tank oscillation, and as of result, energy consumption during the Off-state will be lowered, increasing the overall efficiency of the converter.

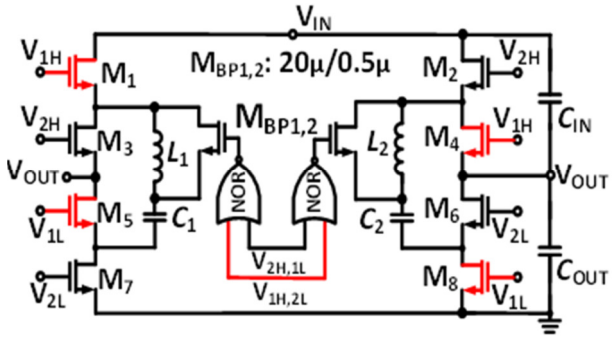


Fig. 2. The schematic of the inductor bypass scheme in the power stage.

III. IMPLEMENTATION

Figure 3 shows the VCO using voltage-mode control OTM, where the t_{ON} of the circuit is determined by the frequency of the *LC* tank, and t_{OFF} is used to regulate the delay between two resonant pulses of the operating phases. An OTA is used to compare the output voltage (V_{OUT}) to a reference to generate a current signal in proportion to the error through resistor R_1, which is injected into the VCO. This current will adjust the discharge rate of $V_{C,OFF}$, controlling how fast the flip-flop changes state. On the side of $V_{C,ON}$, an external voltage of V_{ON} is connected to the circuit via resistor R_2 to inject a current that is modulated by a current mirror, setting the discharge rate of $V_{C,ON}$, similar to the current from the OTA, generating an clock and inverse clock signal, and creating a fully enclosed control loop to create $C_{LK1,2}$ signal for the bootstrap circuit in the next stage. The t_{ON} is fixed by an external voltage supply so that it is equal to half of the resonant period, thereby achieving ZCS. With this OTM scheme, the switching frequency will be adjusted by changing the t_{OFF}, resulting in less switching losses and linear scaling for the converter's effective resistance (R_{eff}). For a given t_{OFF}, the R_{eff} can be calculated as:

$$Reff \approx \left(1+\frac{t_{OFF}}{t_{ON}}\right) R_{eff,full\ resonant} \quad (1)$$

where $R_{eff,full\ resonant}$ is the effective resistance when the converter enters full resonant.

It is important to consider that OTM is a linear regulation approach; therefore, when the conversion ratio gets lower, the voltage ripple will increase since t_{OFF} is prolonged, which proves to be problematic in scenarios where bypass capacitance is limited. Considering this, OTM offers enhanced efficiency during light-load and when fast V_{OUT} regulation is needed.

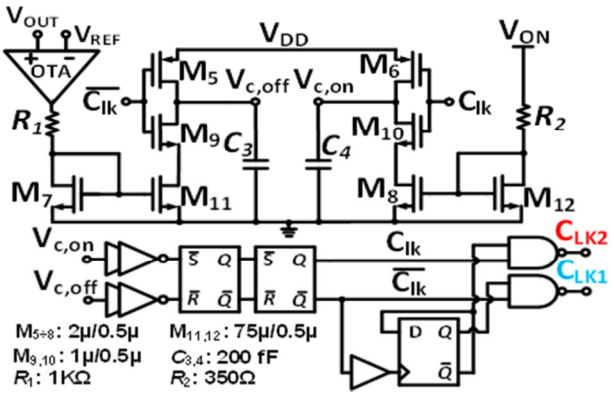


Fig. 3. Schematic of the Voltage-Controlled Oscillator (VCO).

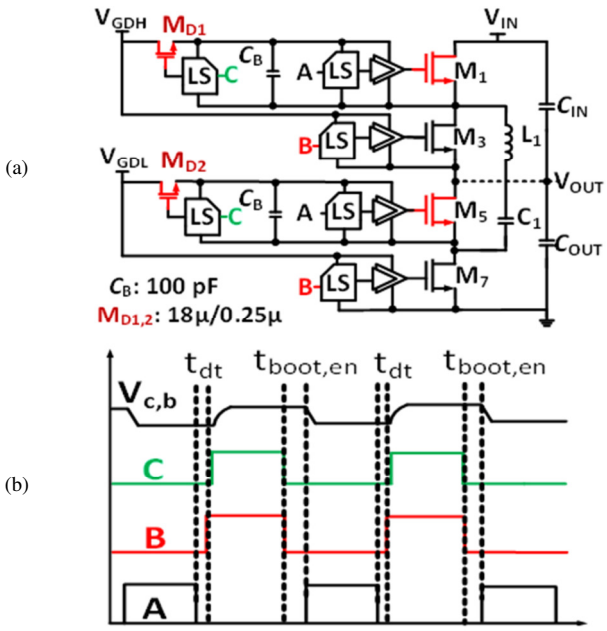


Fig. 4. (a) Schematic of the bootstrapped gate drive circuit and level shifter, (b) waveforms generated.

As shown in Figure 4, each converter phase comprises two complementary switch pairs. In the higher voltage domain pair, M_1 and M_3 are coupled to V_{IN} and V_{OUT}, respectively, while the lower domain pair has M_5 linked to V_{OUT} and M_7 connected to GND. All low-side switches are referenced to the ground and V_{OUT}, whereas high-side switches remain floating and require bootstrapping to operate. Deadtime is inserted between $C_{LK1,2}$ to create high/low side gate signals, as well as the bootstrap enable signal. The bootstrap capacitors are charged from external voltage sources, V_{GDH} and V_{GDL}, which are 1.2 V referenced to V_{OUT} and GND, respectively. The operation of the bootstrapped gate-drive scheme is similar to that of a conventional bootstrap circuit. Other than the source and drain terminal of M_1 and M_7, which are tied to V_{OUT} and GND, while the other terminals are all floating, the same applies to

complementary switches on the other phase. The fundamental property of a capacitor is utilized, which maintains a potential difference between its two plates. Therefore, the high-level and low-level voltages are properly maintained when the potential of source-drain terminals varies and float in M_1, M_3, M_5 and M_4, and consequently, the gate-drive signal, after generated from the Level-Shifter (LS) and having its power amplified through the buffer chain, is capable of operating the NMOS switches in the resonant circuit.

Figure 5 shows the level shifter used in the gate driver to ensure that the propagation delay is less than 800 ps while maintaining low current consumption. Switches M_{19} and M_{20} sink capacitive gate charge from diode-connected devices M_{21} and M_{24} through 5V cascodes at M_{25}, M_{26}, which are high-voltage switches with their gate terminals connected to a 5 V supply and act as upper transistors in a cascode configuration, protecting the input transistors M_{19}, M_{22}, M_{20}, M_{23} from V_H, which can go up to 4.5 V by sharing the voltage drop between them, allowing the circuit to safely interface with higher voltage levels. M_{21} and M_{24} use long-channel devices to increase C_{gs} and decrease propagation delay while consuming minimal current. The current is amplified and digitized to generate the level-shifted voltage from V_L to V_H. V_L connects to the source of the respective power switch, while V_H connects to the supply of the gate driver.

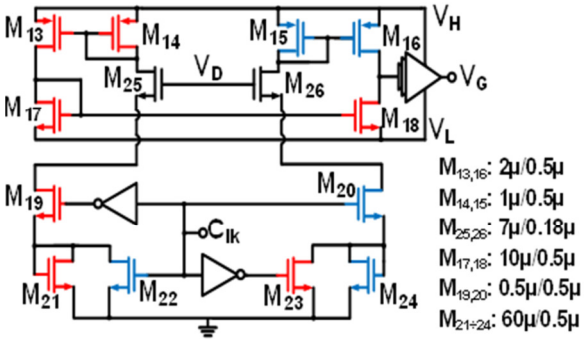


Fig. 5. Schematic of the level shifter.

Figure 6 illustrates the inductors used in the power stage. Two single-layer octagonal planar spiral inductors were implemented in the layout process to save chip area while providing the required inductance calculated using the Wheeler formula [28]:

$$L = K_1 \mu_0 n^2 \times d_{avg} / (1 + K_2 \rho) \quad (2)$$

$$\rho = \left(\frac{d_{out} - d_{in}}{d_{in} + d_{out}}\right) \quad (3)$$

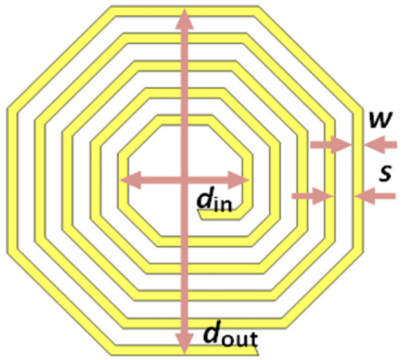
$$d_{avg} = 0.5 \times (d_{out} + d_{in}) \quad (4)$$

$$d_{avg} = d_{in} + 2 \times n \times w + 2(n-1) \times s \quad (5)$$

$$d_{in} = d_{avg} + n \times (w + s) \quad (6)$$

where μ_0 is the vacuum permeability (H/m), K_1 and K_2 are coefficients dependent on the coil shape, n is the number of turns, d_{avg} is the average diameter (m) and ρ is the filling ratio of the coil, d_{in} is the interior diameter, and d_{out} is the external diameter. Inductors were designed with the parameters d_{out} = 200 µm, d_{in} = 150 µm, n = 5, w = 6 µm, s = 2 µm, ρ = 0.203 and d_{avg} = 187 µm. According to simulated results using the CST Studio Suite, the inductor of this design obtained 7.76 nH with a modest quality factor (Q-factor) of 5.45 at an operating frequency of 45 MHz, as illustrated in Figure 6.

(a)



(b)

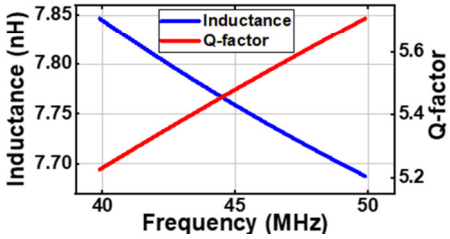


Fig. 6. (a) Planar spiral inductor; (b) simulated relation of Inductance, Q-factor, and Frequency.

IV. SIMULATIONS RESULTS

Figure 7 shows the layout of the proposed DC-DC converter. Most of the converter's passive components are integrated on-chip, including capacitors for the gate driver, power stage, VCO, and inductors, with the only exception being the bypass capacitors. As a result, the active chip area of the proposed design using an 180 nm CMOS process occupies 2.88 mm^2.

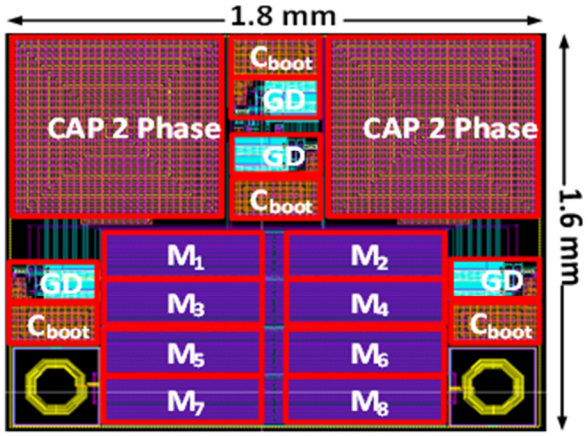


Fig. 7. Layout of the proposed DC-DC converter.

Figure 8 demonstrates the transient response to rapid changes. The control technique involving VCO and OTA proved to be effective, as V_{OUT} remains relatively constant with a mismatch under 100 mV. Importantly, the output voltage ripple remains unaffected, ensuring converter stability. The effectiveness of the linear control scheme is proven by a negligible response time of 70-80 ns. In Figure 9, the On-time t_{ON} of the converter is 11.5 ns, which equals half of the resonant period, resulting in an operating frequency of 43.5 MHz with a fixed On-time in the VCO. Adjusting the conversion ratio involves changing t_{OFF}. As discussed above, having a smaller t_{OFF} resulted in more energy being discharged to the load, minimizing the issue of excessive V_{OUT} drop. Ideally, V_{OUT} will reach 1.2 V regardless of the load value when there is no t_{OFF}, allowing the converter to enter full resonant mode. The duration of high- and low-level voltages of all control signals, as shown in Figure 9(b), is based on the charge/discharge period of capacitors in VCO (Figure 3), meaning that changing the capacitors values or the current mirrors' conversion rate will change the clock pulses, therefore directly adjusting V_{OUT} and CR.

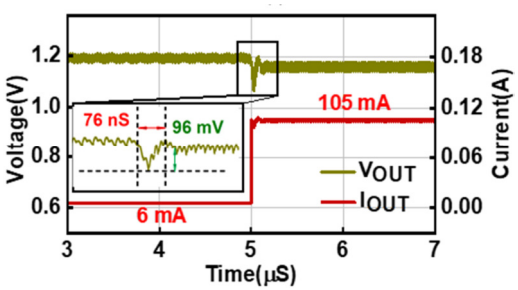


Fig. 8. Transient response for ± mA/µs with V_{IN} = 2.4 V, output regulated to 1.2 V: (a) 105-6 mA in 80 ns overshoot; (b) 6-105 mA in 76 ns undershoot.

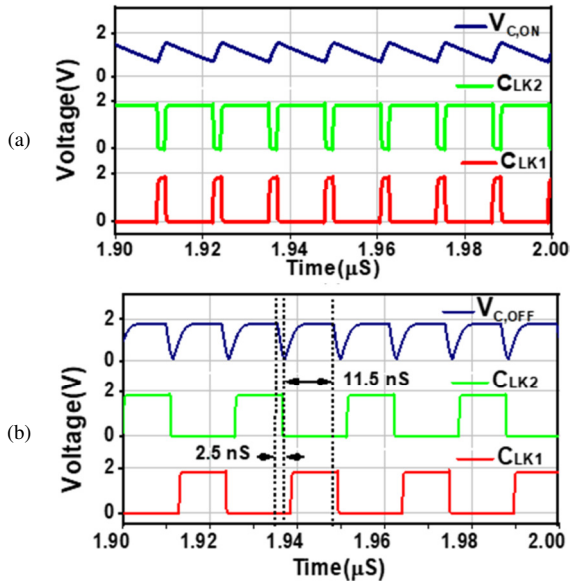


Fig. 9. Simulation results of: (a) generated internal clocks from VCO, (b) control signals.

With increasing load resistance, power loss occurs steadily due to the output current decreasing faster than the increasing output voltage can compensate for. Conversely, under light load conditions, a higher output current results in a significantly greater output power compared to other scenarios, leading to higher efficiency. The waveform of a power transistor control clock signal is shown in Figure 10 for cases without and with inductor bypass.

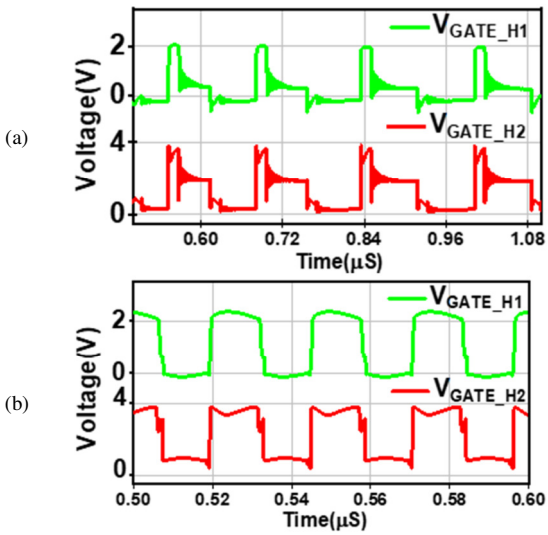


Fig. 10. Simulation results of the gate drive signal: (a) without bypass scheme, (b) with bypass scheme.

In Figure 10(a), due to the effect of the unwanted *LC* tank node ringing impact, the efficiency of the converter is reduced by interfering with the high-side and low-side gate control signal. Figure 10(b) shows the simulation result after the node ringing issue was addressed using the inductor bypass scheme. Figure 11 shows the effect of bypassing the inductor during t_{OFF}. The reduction in *LC* tank ringing means less energy dissipation stored inside the inductors and capacitors themselves. Therefore, energy consumption during the Off-state will be reduced, increasing the overall efficiency of the converter. The comparison was also conducted when the converter was supplied with V_{IN} = 2.4 V and used OTM for improved light-load performance. Moreover, all efficiency calculations included power consumption from external gate drive supplies in a load value range of 0.25 to 20 Ω. The converter, when operating at V_{IN} = 2.4 V with the bypassing inductor proposal, achieves a peak efficiency of 89% at 0.44 W and has an efficiency of around 80-85% in the range of 0.5-0.55 W output power compared to the 83.56% efficiency when the inductor is not bypassed during Off-time, which is a roughly 5% improvement. In Figure 11(a), the converter operates with a 2.4 V input voltage. This puts it in an operational region where the conduction losses are significant due to a fixed power output, and as the current is inversely proportional to voltage, at lower output voltages, the current is higher. As the output voltage increases, the current decreases, initially leading to lower conduction losses. However, as the output voltage increases, the span of t_{OFF} decreases, leading to a

greater operating frequency, and, subsequently, switching losses become significant. The combination of increasing switching losses and decreasing conduction losses leads to an overall decrease in efficiency as the output voltage increases. In Figure 11(b), the converter at low output power has low current, and conduction losses are relatively small; however, the switching losses are large in proportion to the total power, leading to lower efficiency. As the output power increases, the conduction losses increase as a result of the higher current, but the relative impact of fixed switching losses decreases, leading to an increase in efficiency.

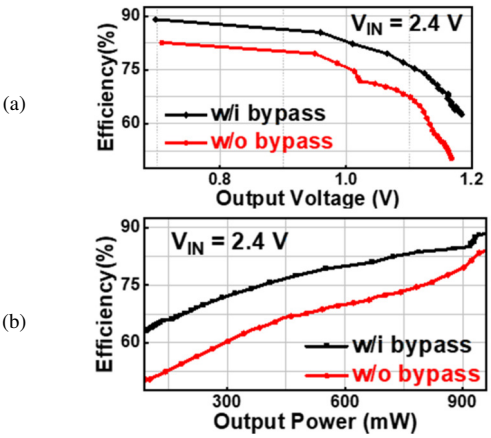


Fig. 11. Efficiency comparison at V_{IN} = 2.4V considering: (a) output voltage, (b) output power.

The proposed design was simulated at various temperatures to investigate the impact of thermal noise on efficiency. Figure 12 shows the efficiency of the proposed converter under varying thermal conditions from -10°C to 60°C, revealing a 5 to 10% drop in peak efficiency as temperatures increase. This decline aligns with established thermal effects in power electronics: elevated temperatures increase NMOS switch on-resistance R_{ON} due to reduced carrier mobility, increasing conduction losses $P_{cond} \propto I^2 \cdot R_{ON}$ [29], while planar spiral inductors suffer from rising ac resistance, degrading their Q-factor and amplifying core losses [30]. Additionally, parasitic leakage currents in on-chip capacitors at higher temperatures further contribute to efficiency loss [31]. The converter's OTM scheme mitigates these effects by adaptively reducing the switching frequency, thereby lowering switching losses $P_{sw} \propto f_{SW} \cdot V_{IN}^2 \cdot C_{oss}$ and maintaining greater than 80% efficiency at 60°C in full load.

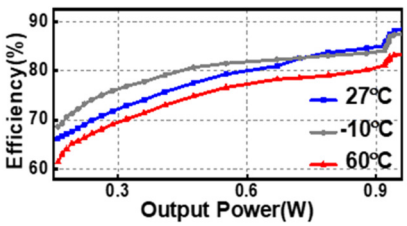


Fig. 12. Converter performance under different thermal conditions.

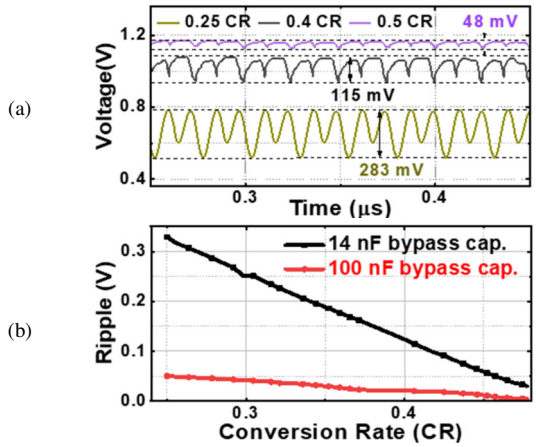


Fig. 13. (a) Voltage ripples approaching 0.5 CR at V_{IN} = 2.4 V, (b) Voltage ripples at different CR and capacitance.

In Figure 13(a), the V_{OUT} ripple changes as the conversion ratio increases to 1:2 VCR. As discussed in Section II, significant output ripple can occur if the t_{OFF} is large, as the circuit's output stability is not properly regulated during this period. A higher t_{OFF} at the beginning results in more energy being stored and subsequently discharged by the *LC* tank to load, thereby increasing the output voltage. As the converter continues to operate, the VCO linear adjustments determine the appropriate t_{ON} and t_{OFF}, achieving the 1:2 conversion ratio and minimizing output voltage ripple. Figure 13(b) shows the benefit of utilizing a symmetric two-phase resonant architecture instead of a single-phase design. The simulation results show that with the same conversion rate, a trade-off can be achieved between having five times the ripple for a fifth of the bypass capacitance or increasing the bypass capacitance five times and having a fifth of the output voltage ripple. In more detail, using only 14 nF bypass capacitance will result in a voltage ripple ranging from 30-329 mV over the conversion ratio from 0.25 to 0.5. On the other hand, if larger than 100 nF bypass capacitors are used, the output voltage ripple remains under 50 mV in the same conversion ratio range, which is roughly five times less than using 14 nF capacitors.

Table I shows a performance comparison between the proposed converter and existing works. The proposed design can be compared to the buck converter in [32], operating at 35.5 MHz, occupying a space of 7.83 mm^2 based on a 130 nm CMOS process, and achieving an efficiency of 85%. In [36], using the SC approach, the converter operates at up to 340 MHz using a 65 nm CMOS process with an efficiency of 79.5%. The design in [35] also uses the SC approach with a 180 nm CMOS process to achieve an efficiency of 75% with a chip area of 2.85 mm^2. Despite using the 180 nm CMOS process, the proposed design used a smaller bypass capacitance value of 7 nF with dual phase, compared to 10 nF with single-phase [34], a lower operating frequency compared to [33], leading to increased passive component sizes and managed to achieve a higher efficiency of 90% while only taking up an area of 2.88 mm^2.

TABLE I. PERFORMANCE COMPARISON

Specs.	Similar works					This work
	[32]	[33]	[34]	[35]	[36]	
Topology	ReSC	SC	SC	SC	Hybrid	ReSC
CR	2:1	2:1	4:3	3:1, 2:1	3:1	2:1
Phases	1	2	1	4	2	2
In. Cap. (nF)	0.18+ off-chip	0	0	0	0	7
Out. Cap. (nF)	10	N/A	10	0.1	N/A	7
F_{SW} (MHz)	35.5	340	0.44~15	N/A	0.05	43.5
V_{IN} (V)	3-4.5	2-2.4	5	1.8	1.15-1.145	2.4-4.4
V_{OUT} (V)	1.5-1.8	0.4-1.2	2.6-3.2	0.5-0.85	0.35-0.45	1-2.2
L_{total} (nH)	9	0.8	0	0	0	7.7
C_{fly} (nF)	2	2	0.9	2.25	300	3.4
Area (mm^2)	7.83	1.5	N/A	2.85	0.012	2.88
Peak eff. (%)	85	79.5	74	75	92	90
Control	None	None	PFM	SAMVRM	None	OTM
Process (nm)	130	65	350	180	28	180

V. CONCLUSIONS

This paper introduced a dual-phase switched-capacitor converter featuring an on-chip *LC* resonator and inductor bypassing scheme, designed in 180 nm CMOS technology. The design achieves 95% peak efficiency in the power stage and 89% closed-loop efficiency at 43.5 MHz, all within a compact 2.88 mm² footprint. By integrating an inductor bypass mechanism and OTM, the converter effectively suppresses trapezoidal ringing in passive components while maintaining under/overshoot below 100 mV during rapid load transients of 6-105 mA in 80 ns. These advances position the converter as a compelling solution for IoT nodes, medical implants, and mobile systems that require stability and miniaturization under light-load conditions.

Beyond academic benchmarks, the converter demonstrates compelling relevance. Its at least 5% closed-loop efficiency improvement addresses critical energy waste in Electric Vehicle (EV) auxiliary systems (e.g., sensor networks, infotainment), directly extending battery life and driving range. Implementation insights reveal robustness and ease for practical implementation: a symmetric dual-phase layout minimizes magnetic coupling losses, while 7 nF off-chip bypass capacitors suppress high-frequency ripple. Compact octagonal spiral inductors (7.76 nH, *Q*-factor ~5.5) balance performance and area constraints, ensuring compatibility with mixed-signal environments. The architecture's scalability allows high-power domain interleaving phases, combined with GaN switches, to mitigate switching losses in kW-level EV traction inverters. Additionally, the dynamic OTM scheme holds promise for renewable energy systems, such as solar microinverters, where adaptive duty cycling aligns with intermittent energy harvesting. By harmonizing efficiency, transient response, and miniaturization, this work helps connect foundational research and industrial deployment, offering a versatile platform for next-generation automotive, IoT, and sustainable energy solutions.

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