Advanced SVPWM Technique for Multilevel Inverter Systems

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ABSTRACT

A computationally efficient Space Vector Pulse Width Modulation (SVPWM) technique is presented in this paper, especially for the Space Vector Modulation (SVM) of three phase, multilevel H-bridge Inverters (HbIs). The primary objective is to improve voltage waveform quality and significantly reduce Total Harmonic Distortion (THD) without the use of additional filtering components. In contrast to the conventional modulation approaches, the proposed method offers a simplified method to compute dwell times through a sector-based vector segmentation technique that enables precise voltage control at lower switching frequency with a relatively simple system architecture. A key strength of this work lies in its comprehensive validation framework, which includes both MATLAB/Simulink simulations and hardware implementation on the Atmega-328 microcontroller. Thus, the proposed solution is not only possible in theory, but also practical and feasible in the real world. The efficiency of the introduced method is confirmed by the experimental results, where a considerable reduction of THD to 10.4% can be still achieved under a modulation index of 0.9, even better than those of the traditional Sinusoidal Pulse Width Modulation (SPWM) techniques. Moreover, it preserves waveform symmetry and increases the DC bus utilization. This approach provides a scalable and low-complexity solution for medium and high-power inverter applications by removing the need of external harmonic filters and encompassing a structured framework to select optimal modulation indices. The work makes a meaningful contribution to the advancement of SVPWM strategies and lays the foundation for future enhancements in adaptive control and modulation strategies for higher-level inverter systems.

Keywords-three-level inverter; harmonic reduction; multilevel inverter; total harmonic distortion

I. INTRODUCTION

Multilevel inverters (MLIs) are widely known for generating higher-quality output waveforms than conventional two-level inverters. They offer several advantages, such as lower harmonic distortion, reduced Common-Mode Voltage (CMV), and reduced switching frequencies without sacrificing performance. Additionally, MLIs can handle higher voltages by cascading power devices, leading to better power quality, improved power factors, and reduced stress on motor insulation, ultimately minimizing eddy current losses [1, 2]. These features make MLIs ideal for medium and high-power applications, including industrial drives, traction systems, and Flexible AC Transmission Systems (FACTS). The three main MLI types are Cascaded H-Bridge (CHB) [3], Neutral Point Clamped (NPC) [4], and flying capacitor topologies [5]. Among these, CHB inverters are particularly preferred for their modular design, which eliminates the need for extra components, such as diodes or capacitors. This modularity allows for independent control of individual phases, making CHB inverters well-suited for renewable energy systems using multiple DC sources [6, 7].

Modulation strategies play a crucial role in the efficient operation of power converters. For CHB MLIs, SPWM and SVM are two widely used methods [8-10]. While both control voltage source converters effectively, SVM stands out for its ability to reduce switching losses and optimize DC bus usage by selecting ideal switching states. Though SVM is straightforward for two-level inverters, applying it to multilevel systems adds complexity. Nevertheless, SVM remains a powerful and reliable choice, particularly in advanced inverter designs requiring high efficiency and performance.

Implementing SVM starts by identifying the sector in which the reference voltage vector (V_{ref}) lies. Based on this, the three nearest space vectors are selected, and their dwell times are calculated to generate optimal switching signals. For example, simplified SVPWM techniques exist for three-level inverters [11], but extending these methods to higher-level configurations becomes increasingly difficult. Solutions for five- and seven-level inverters aim to reduce the number of two-level hexagons, but rely on 3D lookup tables, which increases computational load [12-14]. Other strategies, like the series-based SVM for 13-level CHB inverters [15] and modified SVPWM for nine-level designs [16, 17], attempt to manage complexity by breaking down larger hexagons into smaller ones. Still, as the number of levels rises, computational demands grow rapidly, making practical implementation in high-level MLIs a considerable challenge. An improved Whale Optimization Algorithm (WOA) has been introduced, this approach outperforms nine other metaheuristic algorithms in terms of speed, consistency, and computational efficiency [18]. Using a Genetic Algorithm (GA), the study also addressed nonlinear equations to reduce harmonic distortion, achieving a drop in third and fifth harmonics. The simulation of a five-level inverter in MATLAB/Simulink showed a reduction in THD from 17.88% to 16.74% [19]. Additionally, a compact Artificial Neural Network (ANN) with a single hidden layer of 10 neurons was implemented, offering a good balance between accuracy and computational load [20].

A Modified Dingo Optimization Algorithm was proposed to address the Selective Harmonic Elimination (SHE) problem in MLIs. It achieves better accuracy and optimization efficiency, proving highly effective for harmonic reduction in complex systems [21]. In power systems, a Voltage Optimizer (VO) using a direct PWM AC-AC buck converter was developed to handle overvoltage conditions [22]. For aerospace applications, a deterministic approach was applied to optimize the weight of a three-phase PWM voltage-source inverter [23]. Additionally, a novel Predictive Direct Torque Control (PDTC) method was introduced for permanent magnet synchronous motors, using two active and one zero-voltage vector to reduce torque and flux ripple [24].

Authors in [25] examined harmonic losses in three-phase induction motors powered by six-step Voltage Source Inverters (VSIs). While modern PWM techniques enhance motor speed control, they also introduce low-order harmonics (such as the 5th, 7th, and 11th), which can reduce efficiency, cause overheating, and lead to pulsating torque. A dynamic model was developed to assess these effects under both transient and steady-state conditions, factoring in elements, like skin effect, magnetic saturation, stray load losses, and temperature rise. In related work, a seven-level Reduced Switch Multilevel Inverter (RS MLI) was proposed for medium-voltage, high-power applications [26]. A practical Optimal PWM Signal Modulation technique was introduced to reduce CMV in MLIs. By modifying traditional SPWM through control signal offsetting, the method demonstrates improved CMV suppression over phase disposition techniques, validated through both simulation and hardware tests [27]. Authors in [28] presented a hybrid control method combining fuzzy logic observation with sliding mode control (SMFC) to improve the performance of cascaded MLIs without relying on carrier-based modulation. The proposed SVPWM method simplifies computation while delivering a high-quality output voltage for inverters. It was tested on a three-level inverter and compared with the common carrier-based SPWM across various modulation index values.

II. THREE LEVEL INVERTER

Figure 1 shows a simplified diagram of a three-level HbI. Each unit includes four active switches and four antiparallel diodes, typically using IGBTs in practical setups. A neutral point (N) is formed by connecting one leg of each HbI to an equally rated DC source, typically via a capacitor on the DC side. By varying the switching combinations, the inverter generates three-phase output voltages, allowing for precise voltage control and waveform shaping in power applications. Figure 1 illustrates a three-phase, three-level HbI setup. Each phase R, Y, and B has its own H-bridge circuit with four switches (S_1–S_4) and matching anti-parallel diodes. A DC link voltage (V_{dc}) powers each bridge, while a common neutral point (N) connects all phases. The switches operate in complementary pairs, allowing each phase to output three voltage levels: V_{dc}, 0, and -V_{dc}. This setup enables the inverter to produce a near-sinusoidal waveform with lower harmonic distortion, making it ideal for balanced three-phase load applications.

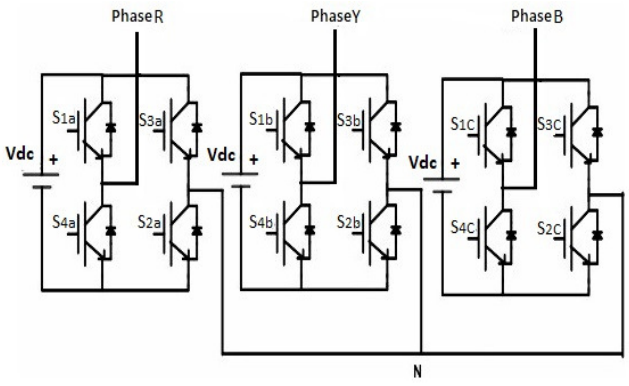

Fig. 1. Topology of three phase three level HbI.

III. GENERATION OF SPACE VECTOR PULSE WIDTH MODULATION

Various SVM techniques have been developed to enhance the control and performance of three-level inverters, particularly in NPC configurations. A typical SVM

implementation for NPC inverters consists of three main steps. First, the reference vector is located within the SVM diagram by determining the specific triangular region in which its tip lies, which determines the operating region. Next, duty cycles are calculated for each triangle, defining how much time each active vector takes to be applied during one modulation cycle. Finally, the appropriate switching states are assigned to generate the desired output voltage, ensuring that the selected switching sequence is maintained. This method allows for more precise control of the inverter, resulting in improved output voltage waveforms and reduced harmonic distortion.

A. Stationary Space Vectors

Each inverter phase can assume three distinct switching states. When all three phases are considered, the inverter exhibits 27 possible switching state combinations. The SVD in Figure 2 shows that these permutations correspond to nineteen separate voltage vectors. Voltage vectors are categorized into four types based on their magnitude. The zero vector is represented by the three zero-magnitude switching states, and the zero-dimensional vector (V_0) is represented by the three zero-magnitude switching states [PPP], [OOO], and [NNN]. Two separate switching states, one involving [P] and the other [N], are linked to the small vectors (V_1 to V_6), which have a magnitude of $\frac{Vd}{3}$. The switching states of these tiny vectors further categorize them as either P-type or N-type. The magnitude of medium vectors (V_7 to V_{12}) is V_d, and the magnitude of large vectors (V_{13} to V_{18}) is $\frac{2Vd}{3}$.

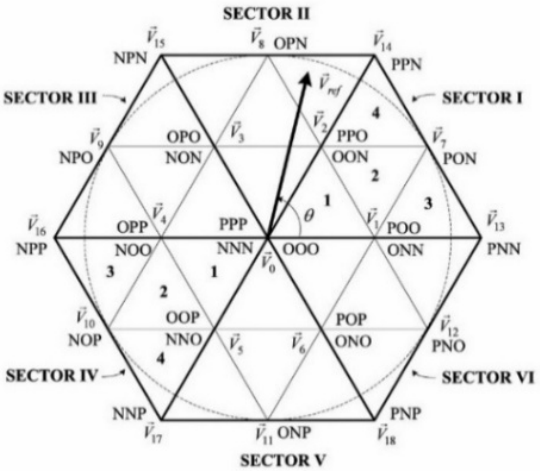

Fig. 2. Segmentation of sectors and regions.

B. Dwell Time Calculation

To simplify the dwell time calculation [29], the SVD can be segmented into six triangular sectors (I to VI), with each sector being further subdivided into four triangular regions (1 to 4). The switching states of all sectors are illustrated in Figure 2. The SVM for a bridge inverter is based on the principle of "volt-second balancing." This principle ensures that the product of the V_{ref} and the sampling period T_S is equal to the combined effect of the space vectors' voltages, each multiplied by their respective time intervals. The reference voltage V_{ref} is synthesized by combining the three nearest stationary vectors. For example, if V_{ref} is in region 2 of sector I, as depicted in Figure 3, the three closest vectors used for synthesis are V_1, V_2, and V_3.

$$\overrightarrow{V_1}\,T_a + \overrightarrow{V_7}\,T_b + \overrightarrow{V_2}\,T_c = \overrightarrow{V_{ref}}\,T_s \quad (1)$$

$$T_a + T_b + T_c = T_s \quad (2)$$

The dwell times T_a, T_b, and T_c correspond to the voltage vectors V_1, V_7, and V_2, respectively. Although the reference voltage vector can technically be synthesized using alternative vector combinations, such methods often result in increased harmonic distortion in the inverter's output voltage, which is generally undesirable in practical applications. The voltage vectors V_1, V_7, V_2, and V_{ref}, as illustrated in Figure 3, can be mathematically represented as:

$$\overrightarrow{V_1} = \frac{1}{3}\,V_d\,, \overrightarrow{V_2} = \frac{1}{3}\,V_d e^{j\pi/3},\ \overrightarrow{V_7} = \frac{\sqrt{3}}{3}\,V_d e^{j\pi/6},\ \overrightarrow{V_{ref}} = V_{ref} e^{j\theta} \quad (3)$$

Substituting (3) into (1) yields:

$$\frac{1}{3}\,V_d T_a + \frac{\sqrt{3}}{3}\,V_d e^{j\pi/6} T_b + \frac{1}{3}\,V_d e^{j\pi/3} T_c = V_{ref} e^{j\theta} T_s \quad (4)$$

$$\frac{1}{3}\,V_d T_a + \frac{\sqrt{3}}{3}\,V_d \left(\cos\frac{\pi}{6} + \mathrm{jsin}\frac{\pi}{6}\right) T_b + \frac{1}{3}\,V_d \left(\cos\frac{\pi}{3} + \mathrm{jsin}\frac{\pi}{3}\right) T_c = V_{ref}\,(cos\,\theta + sin\,\theta) T_s \quad (5)$$

Splitting (5) into the real and imaginary parts, we have:

$$Re: T_a + \frac{3}{2} + T_b + \frac{1}{2} T_c = 3\frac{V_{ref}}{V_d}(\cos\theta) T_s \quad (6)$$

$$Im: \frac{3}{2} T_b + \frac{\sqrt{3}}{2} T_c = 3\frac{V_{ref}}{V_d}\,(sin\,\theta)\,T_s \quad (7)$$

Solving (6) and (7) together with (2), the expressions for dwell times are obtained:

$$T_a = T_s[1 - 2m_a * \sin\theta] \quad (8)$$

$$T_b = T_s\left[2m_a * \sin(\tfrac{\pi}{3} + \theta) - 1\right] \quad (9)$$

$$T_c = T_s\left[1 - 2m_a * \sin(\tfrac{\pi}{3} - \theta)\right] \quad (10)$$

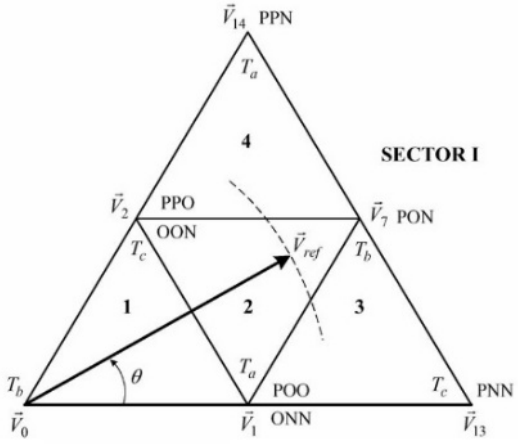

Fig. 3. Voltage vectors and their dwell times.

IV. SOFTWARE IMPLEMENTATION

As shown in Figure 4, the three-phase, three-level H-bridge MLI is modeled in MATLAB/Simulink using twelve IGBTs and twelve diodes. It operates using twelve control signals at a switching frequency of 2 kHz, synchronized with the AC supply. Each H-bridge is supplied with a fixed DC link voltage. For a modulation index of 0.6 and an output frequency of 50 Hz, the simulation captures cyclic angle shifts, intra-sector angle variations, and sector selection at 60° intervals, as displayed in Figure 5. The SVM block manages timing signal design, dwell time calculation, and switch sequencing. Figure 6 depicts the dwell time waveforms for T_a, T_b, and T_c.

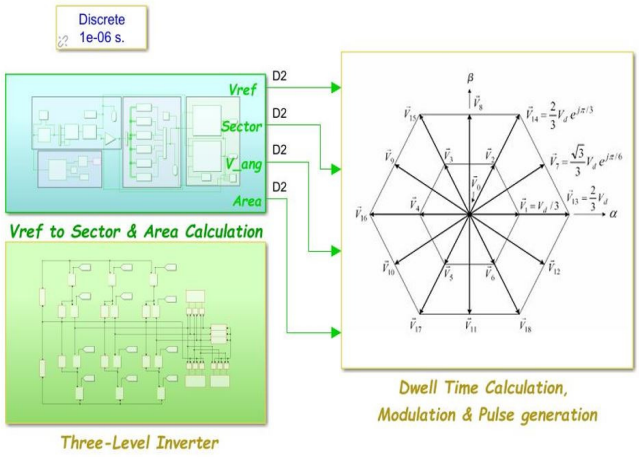

Fig. 4. Simulation model of SVM algorithm.

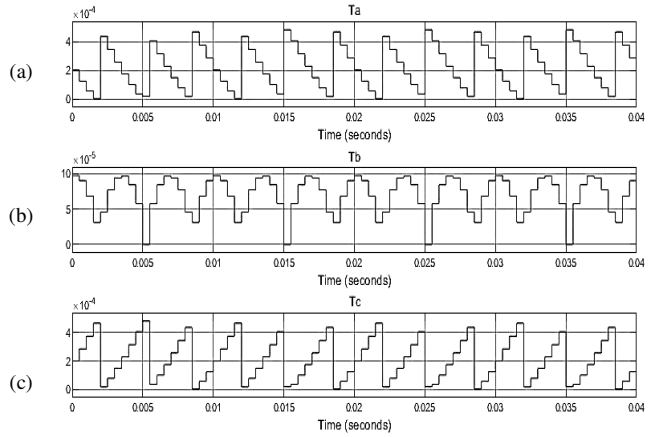

Fig. 5. Waveforms for: (a) cyclic angle waveform in degrees, (b) angle ariation in radians, and (c) sector identification.

V. RESULTS AND DISCUSSION

For the experimental validation, the SVPWM algorithm was programmed in C and implemented on an Atmega-328 microcontroller, tested using a three-level HbI prototype, with each H-bridge powered by 25V, as shown in Figure 7. Tests were conducted under various operating conditions on a 4-pole, 400 V, 50 Hz squirrel cage induction motor rated at 0.5 HP. A 2 kHz switching frequency was used, and the output data were captured using a TBS1072C two-channel oscilloscope with a 1 GS/s sampling rate. The simulated output voltage waveform and corresponding harmonic analysis for a modulation index of 0.6 closely match the experimental results. The waveform exhibits a stepped structure consistent with the three-level inverter operation, while the harmonic spectrum indicates significant suppression of low-order harmonics, resulting in a THD of 12%. The output voltage waveforms and harmonic spectra at M=0.6 are presented in Figure 8 (a) and (b).

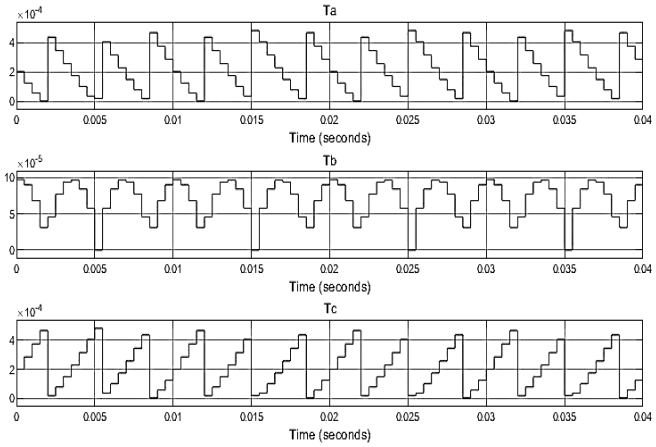

Fig. 6. Dwell time variations.

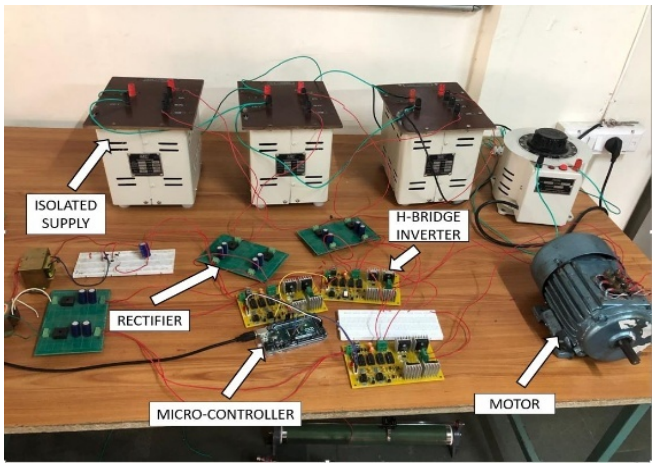

Fig. 7. Experimental setup for three level HbI.

The experimental waveform and harmonic content for a modulation index of 0.6 closely measure THD with simulation results, validating the accuracy and real-world applicability of the proposed SVPWM approach. At a modulation index of 0.9, the waveform closely follows a sinusoidal shape, indicating effective modulation. The harmonic spectrum shows a 50 Hz fundamental frequency with a THD of 10.4%. The output voltage waveforms and harmonic spectra at M=0.9 are portrayed in Figure 9 (a) and (b). Most harmonic components are concentrated around higher-order frequencies, mainly at multiples of the switching frequency. Although the THD is relatively high, the output is acceptable for typical MLI uses. Further filtering or tuning could improve waveform quality and reduce harmonic distortion.

Although M=0.6 provides higher voltage output (better DC bus utilization), the increased THD makes it less favourable in applications sensitive to power quality. Therefore, M=0.9 may be considered optimal in this case, offering a balanced trade-off between voltage output and harmonic performance. Further optimization through advanced filtering could be considered for high M applications.

(a)

(b)

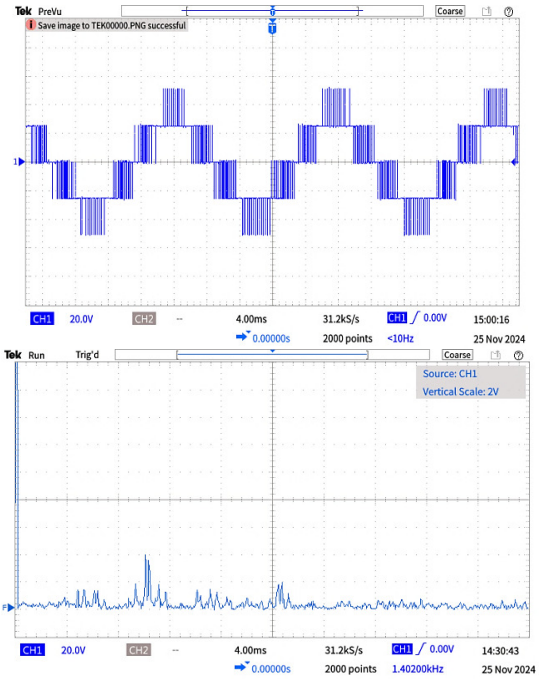

Fig. 8. (a). Line-Line Voltage waveforms and (b) harmonic spectra for M=0.6.

For low modulation indices, SVPWM exhibits higher THD, but maintains a notable advantage. As M increases, THD decreases for SVPWM, reaching a minimum around M=0.9. SVPWM demonstrates superior harmonic performance and is more effective in minimizing THD compared to SPWM, especially at higher modulation indices, as summarized in Table I.

TABLE I. SUMMARIZES COMPARATIVE ANALYSIS OF THD FOR DIFFERENT MODULATION INDICES

Parameter	Observation
Modulation index (M)	0.6
THD at M=0.6	12% (Measured)
Modulation index (M)	0.9
THD at M=0.9	10.4% (Measured)

Figure 10 shows how THD varies with the modulation index (*M*) for both SPWM and SVPWM. Across all values, SVPWM consistently delivers lower THD, especially at higher modulation indices. While both methods show higher THD at low M, SVPWM maintains a clear edge. THD drops as M approaches 0.9, then slightly rises more for SVPWM. SVPWM produces a consistently higher voltage, showing better DC bus utilization. This makes SVPWM more efficient and suitable for applications needing higher voltage output and improved power delivery.

(a)

(b)

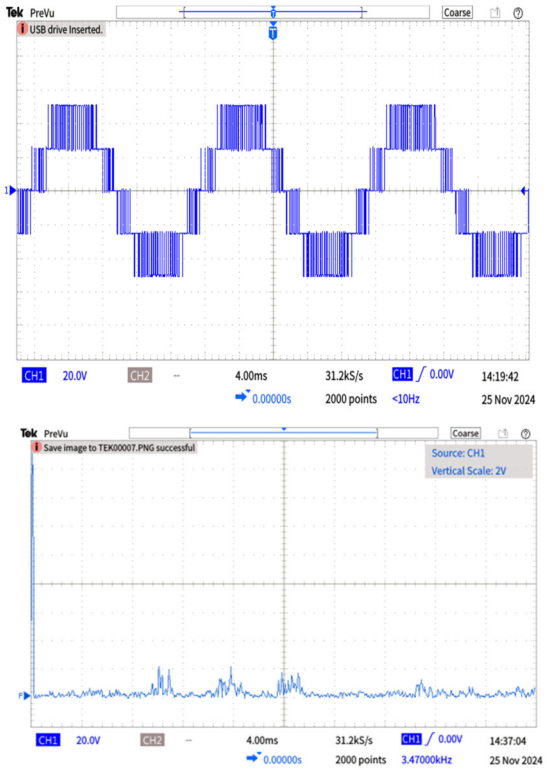

Fig. 9. (a). Line-Line Voltage waveforms and (b) harmonic spectra for M=0.9.

The proposed SVPWM method performs well with three-level inverters, generating near-sinusoidal waveforms as the modulation index approaches 1. Low-order harmonics are effectively suppressed, reducing the need for large filters. Most harmonics appear at higher frequencies ,2 kHz, 4 kHz, 6 kHz, and beyond. As the modulation index increases, THD drops significantly, confirming SVPWM's efficiency in producing clean output waveforms.

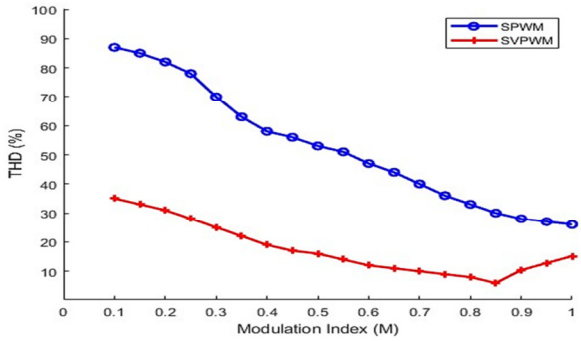

Fig. 10. Comparison of THD for SPWM and SVPWM techniques.

VI. CONCLUSION

This paper presents a novel and highly efficient Space Vector Pulse Width Modulation (SVPWM) scheme designed for three-level H-bridge Multilevel inverters (MLIs). The proposed method strikes a balance between computational

simplicity, compatibility with low-power hardware, and effective harmonic reduction, which enables its suitability for real-world application, in contexts where the resources are limited. The proposed dwell-time modulation strategy uses sector-based vector decomposition, departing from conventional modulation techniques, while this process does not compromise with the quality of the waveform accuracy and the nature of the output. Consequently, the maintained waveform integrity holds, and a Total Harmonic Distortion (THD) as low as 10.4% at a modulation index of 0.9 may be achieved. Through a two-tier theoretical robustness that involves MATLAB/Simulink simulations and hardware prototype based on Atmega-328 microcontroller, system reliability is also proven as well as system performance.

The study offers two key factors; one is the high level SVPWM framework, which is specially designed for mid-range inverter systems with no need for complicated hardware, such as digital signal processors. Second, it provides some interesting information on how performance changes with the modulation indices to define a set of optimal parameters for such applications in industrial automation and renewable energy systems. By addressing practical limitations of conventional SVPWM methods, the proposed approach enhances both accessibility and scalability, paving the way for future development of advanced inverter topologies and adaptive modulation strategies.

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