

Design and Optimization of Speed and Power in FinFET Based Binary and Ternary CAM Cells and 4x4 CAM Arrays Using MTCMOS and GDI Techniques

N. Praveena

Department of Electronics and Communication Engineering, Rashtreeya Vidyalaya College of Engineering, Bengaluru-560059 (working at Electronics and Communication Engineering, Sir M. Visvesvaraya Institute of Technology, Bengaluru), Affiliated to Visvesvaraya Technological University, Belagavi, Karnataka, India
praveena_ec@sirmvit.edu

N. Shylashree

Department of Electronics and Communication Engineering, Rashtreeya Vidyalaya College of Engineering, Bengaluru—560059, Karnataka, India
shylashreen@rvce.edu.in (corresponding author)

Received: 7 April 2025 | Revised: 10 June 2025 | Accepted: 21 June 2025

Licensed under a CC-BY 4.0 license | Copyright (c) by the authors | DOI: <https://doi.org/10.48084/etasr.11346>

ABSTRACT

Content Addressable Memories (CAMs) are primarily used in routers and packet forwarding. The biggest problems in CAM design are the parallel comparison of Match Lines (MLs), latency, and power usage. This paper discusses the following techniques for reducing the latency and power: a binary 4T CAM cell, a 4x4 CAM array, novel 8T and 4T TCAM cells, a 4x4 TCAM array, Multi-Threshold CMOS (MTCMOS), and Gate Diffusion Input (GDI). The proposed binary MTCMOS CAM cell reduces the power dissipation by 31% and the delay by 11%, while the GDI CAM cell reduces the delay by 94.4%. The power consumed by the 8T-TCAM cell in the proposed TCAM designs is 754.5 nW, and the delay is 1015.4 ps. The 4T-TCAM cell reduces the power consumption by 37.65% and the delay by 18% compared to the 8T-TCAM cell. To further reduce the power and delay, the MTCMOS technique was applied to the 4T-TCAM cell. This resulted in a 32.5% reduction in power and a 13.09% reduction in delay, using Cadence 18nm FinFETs.

Keywords-FinFET; Multi-threshold CMOS (MTCMOS); Gate Diffusion Input (GDI); ternary inverter; Content Addressable Memory (CAM); Ternary CAM (TCAM)

I. INTRODUCTION

CAM, also known as associative memory, is useful in applications related to quick searching. A Binary CAM (BCAM) cell stores only binary values, i.e., 0s and 1s, and can search only for 0s and 1s [1]. The Ternary CAM (TCAM) is a special type of high-speed memory that searches its entire contents in a single clock cycle. The term ternary indicates the memory's ability to store and search for data with values of 0 and 1, similar to BCAM, as well as an intermediate value of X, which may be termed a "don't care" or "wildcard" state [2-5]. The CAM cells are known for their fast-operating speed, but this comes at the cost of increased power consumption and area [6]. Therefore, if the power consumption is reduced using certain techniques, it is important to ensure that the speed is not sacrificed. The CAM cells are primarily used to create lookup

tables [7] and the main power consumption is due to the MLs. Another important factor in a circuit design is the delay; therefore, optimizing these two components is the most important task. The power consumption increases by using more transistors and more complex circuits [8, 9], while the delay increases when there are many logic blocks between the input and output, so various techniques must be used to minimize the power demand and delay [10-12], such as MTCMOS. FinFETs are used because they have more advantages than MOSFETs [13, 14], with the channel between the source and drain being elevated above the surface, while the gate surrounds this elevated channel. A FinFET can have multiple channels between the source and drain, all of which are connected to the gate [15-17]. There are different models of CAM cells, such as 10T, 9T, 8T, and 4T. This paper uses a

binary 4T CAM cell and novel ternary 8T and 4T CAM cells designed using MTCMOS techniques.

II. PROPOSED DESIGNS

A. Methodology

The flow chart in Figure 1 presents the methodology of the binary CAM. The delay and power comparison analysis are carried out between the conventional binary CAM memory and the proposed MTCMOS and GDI binary CAM memory, using FinFETs.

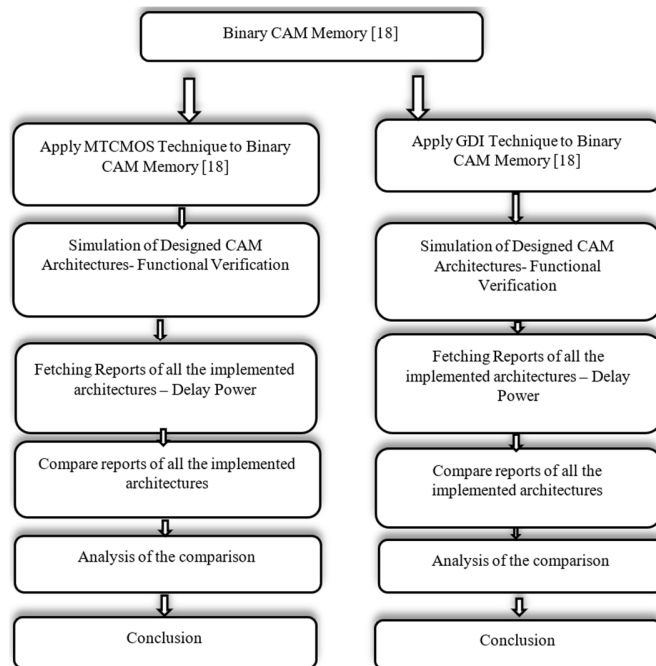


Fig. 1. Flow chart of the methodology of BCAM.

B. MTCMOS Technique

The MTCMOS technology has become a promising alternative to traditional CMOS for the construction of logic gates that operate at high speeds while exhibiting relatively low power dissipation. MTCMOS is a circuit-level technique that has proven effective in delivering high performance and low power design by leveraging both low and high-threshold voltage transistors. This technology is used to minimize the subthreshold currents in standby mode while ensuring the continuity of the circuit performance, as shown in Figure. 2. The device under consideration consists of six transistors in total; two sleep transistors, designated M1 and M6, with elevated V_t values, have been integrated into the 4T CAM cell circuit, which consists of low V_t transistors. The device is equipped with two distinct operational modes: active mode and sleep mode. The primary function of these modes is to regulate the device's power management. The presence of two distinct threshold voltages is observed: the low V_t is derived from the power supply, while the high V_t originates from the ground circuit. The two sleep transistors, contribute to the reduction of the standby leakage, as indicated by their high V_t . When S is set to zero, the data are stored in M2 and M3. The storage of the

data is managed by M3 and M4 and the circuit consists of four NMOS transistors. M4 and M5 are used to compare the Search Line (SL) and ML. When $W_r = 1$, $SL = 1$, and $bit = 1$, then $ML = 0$ and if $SL = 1$, $bit = 0$, then $ML = 1$. The construction of a 4X4 CAM array using the MTCMOS technique is possible, but the 4T CAM cell must be replaced with the 4T CAM cell that utilizes the MTCMOS technique.

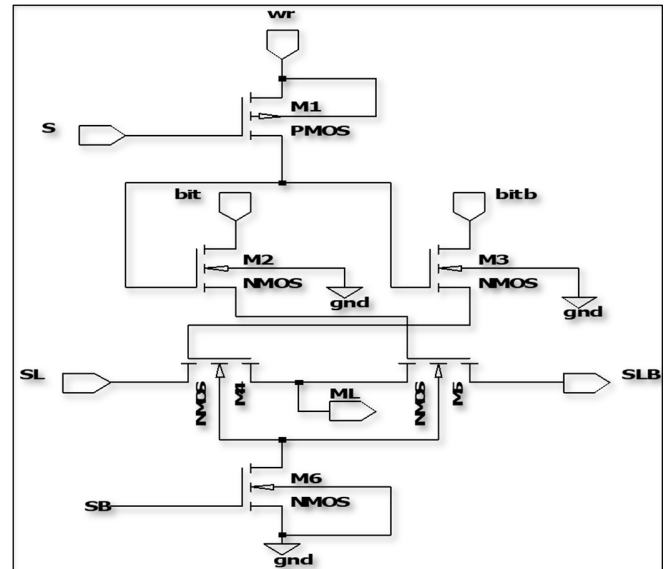


Fig. 2. 4T CAM cell using MTCMOS Technique.

C. GDI Technique

Two transistors, consisting of one PMOS and one NMOS, are used to design circuits for the CAM cell, as portrayed in Figure 3. A combination of GDI cells was used to design the CAM cell. The inputs for the different transistors were selected depending on their functionality and are combined to form the circuit, while buffers can be used to stabilize the output, if necessary. A total of sixteen transistors were used and a 4x4 CAM array was built deploying the GDI technique, consisting of sixteen CAM cells.

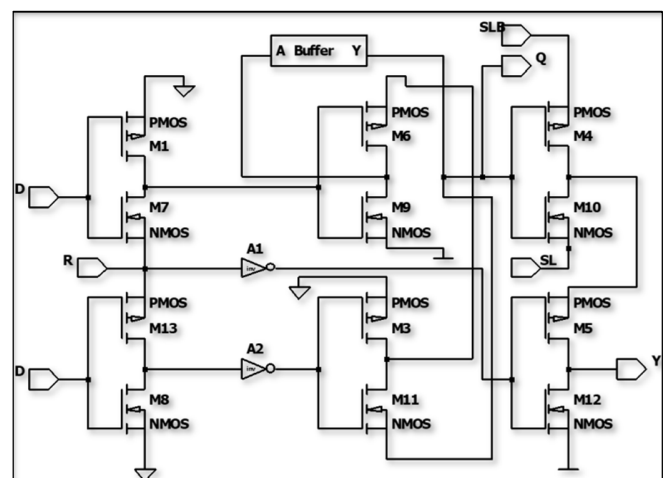


Fig. 3. CAM cell using GDI technique.

D. Ternary CAM

Figure 4 displays the flowchart of the binary CAM methodology. The basic element used in designing the novel TCAM cell is the Ternary Inverter (TI), utilized in an 8T-TCAM cell and then in a 4T-TCAM cell. To reduce the power consumed by the proposed 4T-TCAM, the MTCMOS technique is applied to the circuit, with a 4x4 array being employed for both the 4T-TCAM cell and the MTCMOS-based 4T-TCAM cell. The supply voltage for all designs is 0.5 V.

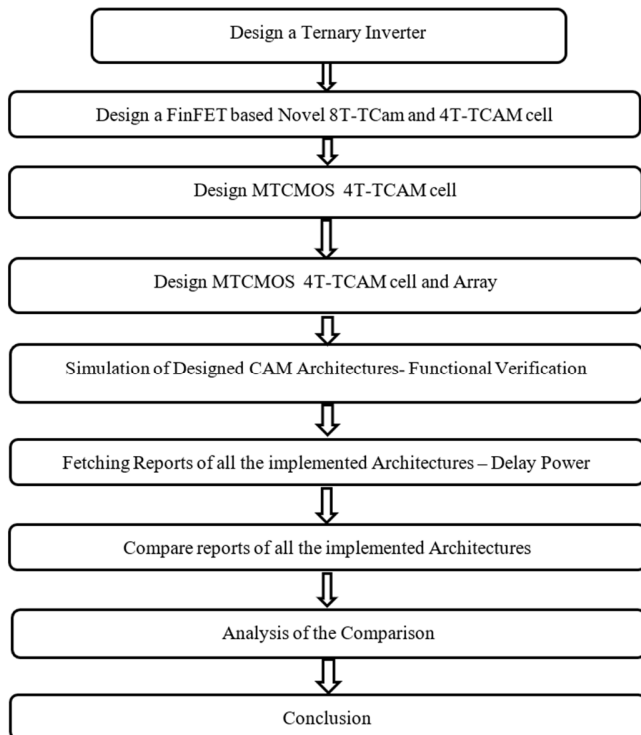


Fig. 4. Flow chart of the methodology of ternary CAM.

E. Ternary Inverter

Digital logic systems use radix two, comprising two logic levels: 0 and 1. The TI is a multi-valued logic system that utilizes a radix of three, making it a ternary system and it is designed to have three logic states: 0, 0.25, and 0.5, as illustrated in Table I and in Figure 5. The TI provides a value of 0.5 when the input is 0, a value of 0 when the input is 0.5, and a value of 0.25 when the input is 0.25. Thus, the TI retains three logic values when used in a memory configuration and the V_{th} is 264.125 mV.

TABLE I. TRUTH TABLE FOR TERNARY INVERTER

Input state	Output State
0	0.5
0.25	0.25
0.5	0

F. Proposed 8T-TCAM Cell

The cross-coupled inverter of the proposed 8T-TCAM functions as a memory element. M1 and M3, and M2 and M4 are P-FinFETs, and they form the two discharge paths for M, respectively. Prior to the initiation of the match operation, the M is precharged to 0.5V and if there is a deviation between SL and D, a discharge path is initiated, resulting in a low M, as presented in Figure 6. There are two case scenarios:

- Case 1: Match operation, $D = 0$, and $SL = 0$. M2 is operational, while M4 is not. Consequently, the discharge path M2-M4 is rendered ineffective. In addition, given that Db is 1, M1 is deactivated, and SL is set to 0, this results in M3 being activated. Consequently, the discharge path from M1 to M3 is rendered ineffective and M remains high signifying that the operation is ongoing.
- Case 2: Mismatch operation, $D = 0$, and $SL = 1$. M2 and M4 are both operational. Consequently, the discharge path M2-M4 is valid, and given that Db is 1, M1 is deactivated, and SL is set to 1, which consequently deactivates M3. This results in the discharge path from M1 to M3 being rendered ineffective. In the event that one of the discharge paths (M2-M4) is active, the M discharges to 0, indicating a mismatch operation.

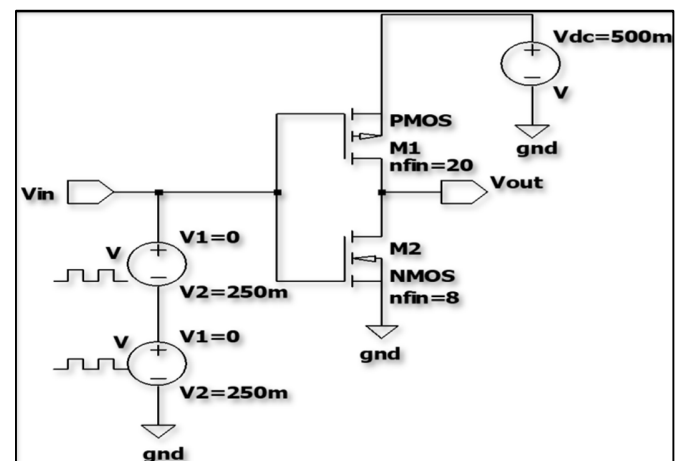


Fig. 5. Proposed TI circuit.

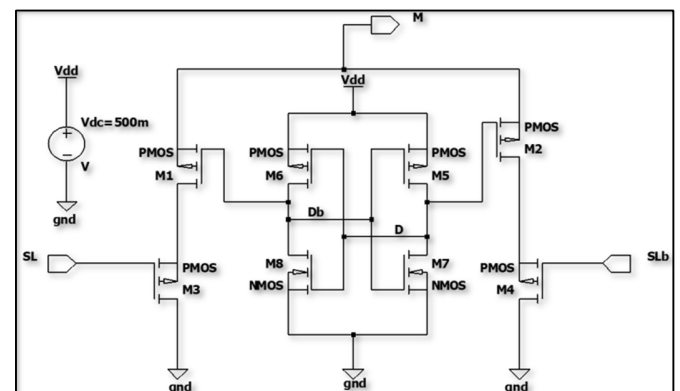


Fig. 6. Proposed 8T-TCAM cell circuit.

G. Proposed 4T-TCAM Cell

As exhibited in Figure 7, the circuit diagram of the proposed 4T-TCAM cell is composed of six forms that serve as the base for the 4T-TCAM cell. The circuit under consideration contains four FinFETs. P1 and N1 form the TI, while the P-FinFET P2 is used to write the value into the TCAM and the P-FinFET P3 is utilized as an evaluation FinFET. The 4T-TCAM cell's design is such that when the input to the TI used in the 4T-TCAM cell is set to 0.25 (X value), while the output of the TI remains at 0.25. This results in the input to the P3 being set to 0.25 V, thereby deactivating the P3. The P-FinFET is activated when the gate input reaches 0 V. The P3 function is enabled exclusively under circumstances wherein the voltage at node X is at 0V. This condition is met during instances of mismatch operation. Consequently, the ML remains high when a X value (0.25V) is stored in the 4T-TCAM cell. The value Q, which is written into the cell, is stored gate capacitance of the TI. The two operational phases of the proposed 4T-TCAM are divided into two: the write operation and the search operation. In order to execute the write operation, the Word Line (WL) is pulled down to 0, thereby disabling the Metal-Liquid (ML). In the search operations, ML is precharged to V_{dd} (0.5V) and WL is set to 0.5V:

- Write operation: WL is set to 0V in order to activate P2. The data presented on DL is written to node Q and stored in the gate capacitance of TI.
- Search operation: The ML is precharged to a voltage of 0.5 V and WL is pulled to 0.5V to turn off P2.
- Match Case: When $Q=0$ V, $SL=0$ V, $SLb=0.5$ V, this results in the activation of P1 and the deactivation of N1. Therefore, the voltage at node X is 0.5V. The P3 function is deactivated, and the ML remains high.
- Mismatch Case: When $Q=0$ V, $SL=0.5$ V, $SLb=0$ V, this results in the activation of P1 and the deactivation of N1. Therefore, the voltage at node X is 0 V, the P3 is activated, and the ML discharges to the ground.

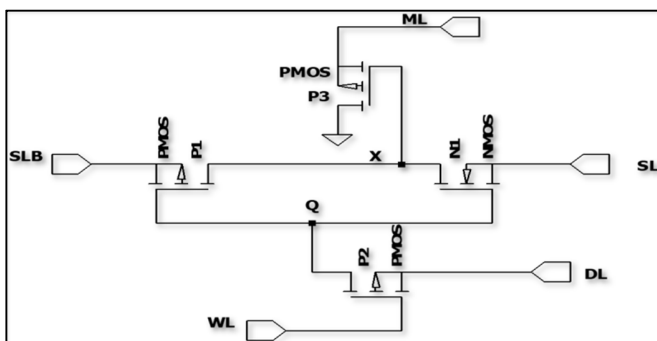


Fig. 7. Proposed 4T-TCAM cell circuit.

H. Proposed MTCMOS based 4T-TCAM Cell

The ML is the most power-consuming component of the TCAM cell. The objective of this study is twofold: first, to reduce the power consumption, and second, to increase the speed of operation of the 4T-TCAM cell, by applying the

MTCMOS technique to the proposed 4T-TCAM. The 4T-TCAM logic circuit, is designed through the usage of low V_t (L_{vt}) (threshold voltage) FinFETs, a method that uses the MTCMOS technique. The ML configuration results in the highest power consumption within the circuit. To resolve this issue, the ML is isolated from the circuit by applying a high V_t (H_{vt}) header P-FinFET, as shown in [15]. The H_{vt} header P-FinFET is enabled or disabled by the Sleep (SLP) signal. The precharged ML is evaluated solely under the condition that the SLP signal is 0 V during the match operation. When the SLP is pulled to V_{dd} (0.5 V), the ML is isolated from the circuit, resulting in a further reduction in the circuit's power consumption. The operational speed of the MTCMOS-based 4T-TCAM logic circuit is enhanced through the usage of L_{vt} transistors. The SL and SLb lines of each TCAM cell in a given column are shorted and the search operation is executed in a row-by-row manner. The ML remains high only when the data stored in each of the TCAM cells in a given row are a match with the corresponding data on the SL. In all other cases, the ML discharges to ground. The 4x4 TCAM array contains four MLs and the design of the array is made through the usage of the Cadence Virtuoso tool.

III. SIMULATION AND RESULTS

A. Binary CAM Cell

The CAM cells and 4X4 CAM arrays were thoroughly analyzed in Cadence Virtuoso. A series of simulations were conducted on the 4T CAM cell, exploring a range of techniques including MTCMOS and GDI. Table II presents a comparison of the power and delay for a CAM cell. It was observed that the CAM cell, using the MTCMOS technique, exhibited a reduced power loss and delay. Additionally, it was observed that the CAM cell using the GDI technique exhibited a reduced delay.

TABLE II. COMPARISON OF POWER AND DELAY FOR A CAM CELL

Design type	4T CAM cell		4X4 CAM array	
	Delay (ns)	Power dissipation (μ W)	Delay (ns)	Power dissipation (μ W)
Proposed design-4TCAM cell using MTCMOS technique	1.146	2.284	0.148	22.42
Proposed design-4T CAM cell using GDI technique	0.073	25.04	0.102	375.9
4TCAM cell [9]	1.291	3.3	0.58	35.37

B. Ternary CAM Cell

The proposed TCAM designs and 4X4 array usage are to be executed within the Cadence Virtuoso Analog Design Environment. The designs are simulated within the Cadence Virtuoso Analog Design Environment and the waveforms are recorded, estimating the power consumption and delay of the circuits. For all TCAM designs, the ML is charged for a duration of 30 ns, and the simulation is executed for 60 ns. Subsequently, the ML is evaluated for both the match and mismatch operations.

C. Ternary Inverter

As depicted in Figure 8, the waveform obtained for the TI design is in accordance with the truth table of the TI. The intermediate state of 0.25 V is retained, and can be regarded as a "don't care" value (X) when the transistor is used in the cross-coupled configuration within the memory circuit. Table III shows a comparison of the power and delay for the proposed TCAM designs. The TCAM cell that uses the MTCMOS technique exhibits a reduced power dissipation and delay in comparison to the 8T and 4T TCAM cells.

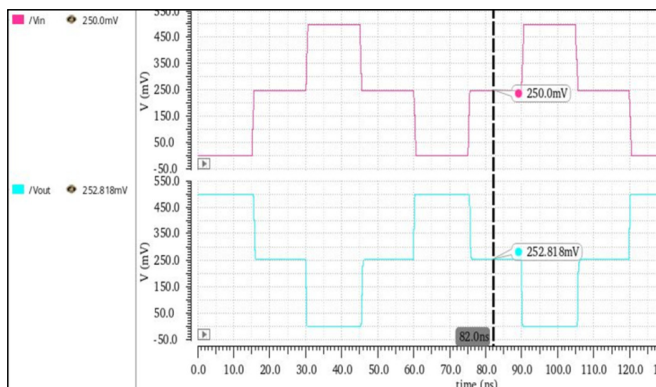


Fig. 8. Output waveform for proposed TI.

TABLE III. COMPARISON OF POWER AND DELAY FOR PROPOSED TCAM CELLS

TCAM cell	Transistor count	Delay (ps)	Power (nW)
Proposed 8T-TCAM cell	8	1015.4	754.5
Proposed 4T-TCAM cell	4	947.9	470.4
Proposed MTCMOS based 4T-TCAM cell	5	823.8	317.2

D. 4x4 TCAM Array Using 4T-TCAM Cells and MTCMOS based 4T-TCAM Cells

The TCAM array is simulated for three distinct cases: complete match, partial match, and a combination of partial and complete match. A partial match indicates that there is a subset of X values in the data. The term complete match is used to describe the presence of 0s and 1s in the data. Given that the array size is 4x4, the SL data consist of 4 bits each. The total number of MLs is four maintaining a high or low status, respectively, in accordance with the match or mismatch of data in each row. Table IV presents a comparison of the power and delay metrics for the proposed TCAM array designs. It was observed that the 4x4 array employing MTCMOS-based 4T-TCAM exhibited a reduced power consumption and a diminished delay compared to the 4x4 array using 4T-TCAM cells.

TABLE IV. COMPARISON OF POWER AND DELAY FOR PROPOSED TCAM ARRAYS

TCAM cell	Delay (ns)	Power (μ W)
Proposed 4x4 TCAM array using 4T-TCAM cell	1.12	24.4
Proposed 4x4 TCAM array using MTCMOS based 4T-TCAM cell	0.92	15.02

IV. CONCLUSIONS

This study examines techniques for the power and delay reduction, including a novel TCAM (8T, 4T CAM) cell, a 4x4 TCAM array, a binary 4T CAM cell, Multi-Threshold CMOS (MTCMOS), and Gate Diffusion Input (GDI) approaches. The findings revealed that using the MTMOS technique led to a 31% reduction in power dissipation and a 11% decrease in delay in the Binary CAM cell. Additionally, a 36.6% decrease in power dissipation was observed in the 4X4 CAM array. In GDI, a reduced delay was obtained in both the Binary CAM cell and 4X4 CAM array and the power consumption of the proposed 8T-TCAM cell has been determined to be 754.5 nW, while the delay was measured at 1015.4 ps. The proposed 4T-TCAM cell exhibits a 37.65% reduction in power consumption and an 18% decrease in delay when compared with the proposed 8T-TCAM, exhibiting a power consumption of 470.4 nW and a delay of 947.9 ps. In order to achieve a further reduction in power and delay, the MTCMOS technique was applied to the 4T-TCAM cell. This resulted in a 32.5% reduction in power and a 13.09% reduction in delay. The 4x4 TCAM arrays were installed using the proposed 4T-TCAM cells and the proposed MTCMOS-based 4T-TCAM cells. It has been observed that the array configuration employing MTCMOS-based 4T-TCAM cells exhibits a power consumption that is 38.5% less than that of the configuration using 4T-TCAM cells. Additionally, the delay in the former configuration is 17.8% less than that before. Consequently, it can be determined that the proposed MTCMOS-based 4T-TCAM cell exhibits the lowest power consumption and the fastest operating speed. This study provides evidence of the significance and benefits of employing techniques, such as MTCMOS and GDI. The design and simulation of these components was conducted using the Cadence Environment, with the power and delay of a single cell being estimated through simulation.

REFERENCES

- [1] D. Bhattacharya, A. N. Bhoj, and N. K. Jha, "Design of Efficient Content Addressable Memories in High-Performance FinFET Technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 5, pp. 963–967, Feb. 2015, <https://doi.org/10.1109/TVLSI.2014.2319192>.
- [2] M. Irfan, R. C. C. Cheung, and Z. Ullah, "Bank-selective Strategy for Gate-based Ternary Content-addressable Memory on FPGAs," in *2019 IEEE 30th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, New York, NY, USA, Jul. 2019, vol. 2160–052X, pp. 288–291, <https://doi.org/10.1109/ASAP.2019.00019>.
- [3] W. Yu, S. Sivakumar, and D. Pao, "Pseudo-TCAM: SRAM-Based Architecture for Packet Classification in One Memory Access," *IEEE Networking Letters*, vol. 1, no. 2, pp. 89–92, Jun. 2019, <https://doi.org/10.1109/LNET.2019.2897934>.
- [4] N. Trinh, A. L. T. Kim, H. Nguyen, and L. Tran, "Algorithmic TCAM on FPGA with data collision approach," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 22, no. 1, pp. 89–96, Apr. 2021, <https://doi.org/10.11591/ijeecs.v22.i1.pp89-96>.
- [5] T. Nguyen, K. Ngo, N. Trinh, B. Bui, L. Tran, and H. Trang, "Efficient TCAM design based on dual port SRAM on FPGA," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 22, no. 1, pp. 104–112, Apr. 2021, <https://doi.org/10.11591/ijeecs.v22.i1.pp104-112>.
- [6] T. Molom-Ochir, B. Taylor, H. Li, and Y. Chen, "Advancements in Content-Addressable Memory (CAM) Circuits: State-of-the-Art, Applications, and Future Directions in the AI Domain," *IEEE*

- Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 8, pp. 3971–3982, Dec. 2025, <https://doi.org/10.1109/TCSI.2025.3527309>.
- [7] V. R. Datti and P. V. Sridevi, "Performance Evaluation of Content Addressable Memories," in *2018 7th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO)*, Noida, India, Dec. 2018, pp. 596–598, <https://doi.org/10.1109/ICRITO.2018.8748808>.
- [8] D. Georgiev, "Low Power Concept for Content Addressable Memory (CAM) Chip Design," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, vol. 2, no. 7, pp. 3165–3170, Jul. 2013.
- [9] P. Ramakrishna, S. Rajendar, and N. Malladhi, "Design of low power memory architecture using 4T content addressable memory cell," in *2017 4th International Conference on Advanced Computing and Communication Systems (ICACCS)*, Coimbatore, India, Jan. 2017, pp. 1–6, <https://doi.org/10.1109/ICACCS.2017.8014618>.
- [10] M. Suresh, A. K. Panda, and J. Sudhakar, "Low power aware standard cells using dual rail multi threshold null convention logic methodology," *Microprocessors and Microsystems*, vol. 68, pp. 28–33, Jul. 2019, <https://doi.org/10.1016/j.micpro.2019.04.003>.
- [11] B. L. Dokic, "A Review on Energy Efficient CMOS Digital Logic," *Engineering, Technology & Applied Science Research*, vol. 3, no. 6, pp. 552–561, Dec. 2013, <https://doi.org/10.48084/etasr.389>.
- [12] S. Khmailia, J. Rouabeh, and A. Mami, "Design of a Low Power CMOS Inverter with the VBB Stack Approach," *Engineering, Technology & Applied Science Research*, vol. 12, no. 4, pp. 8891–8895, Aug. 2022, <https://doi.org/10.48084/etasr.4823>.
- [13] N. Patel and B. Soni, "A Research Paper On The Electrical And Physical Characteristics Of FinFET Using LTspice," in *2023 IEEE 11th Region 10 Humanitarian Technology Conference (R10-HTC)*, Rajkot, India, Jul. 2023, pp. 207–212, <https://doi.org/10.1109/R10-HTC57504.2023.10461900>.
- [14] P. Agrwal and A. Kumar, "Revolutionizing Semiconductor Technology: A Comprehensive Review of FinFET," in *2024 International Conference on Communication, Computer Sciences and Engineering (IC3SE)*, Gautam Buddha Nagar, India, Feb. 2024, pp. 478–482, <https://doi.org/10.1109/IC3SE62002.2024.10592992>.
- [15] D. Cerović, V. Del Piccolo, A. Amamou, K. Haddadou, and G. Pujolle, "Fast Packet Processing: A Survey," *IEEE Communications Surveys & Tutorials*, vol. 20, no. 4, pp. 3645–3676, 2018, <https://doi.org/10.1109/COMST.2018.2851072>.
- [16] M. Sathe and N. Sarwade, "Performance Comparison of CMOS and Finfet Based Circuits at 45nm Technology Using SPICE," *International Journal of Engineering Research and Applications*, vol. 4, no. 7, pp. 39–43, Jan. 2014.
- [17] M.-C. Chang, K.-L. He, and Y.-C. Wang, "Design of asymmetric TCAM (ternary content-addressable memory) cells using FinFET," in *2014 IEEE 3rd Global Conference on Consumer Electronics (GCCE)*, Tokyo, Japan, Jul. 2014, pp. 358–359, <https://doi.org/10.1109/GCCE.2014.7031172>.
- [18] K. Yuvana, P. Balavenkateswarlu, T. Mohammed Abbas, and S. Ashok, "Analysis And Design of Low Power Content Addressable Memory (CAM) Cell," *International Journal of Emerging Technology and Advanced Engineering*, vol. 3, no. 12, pp. 514–519, Dec. 2013, <https://doi.org/10.46338/ijet>.