

A Temperature-Adaptive Low Dropout Regulator Architecture with Dynamic Voltage Scaling for Low Power IoT Applications

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ABSTRACT

The aggressive scaling of CMOS technologies for Internet of Things (IoT) devices has intensified power management challenges, particularly under thermally stressed and battery-constrained conditions. Elevated temperatures exacerbate leakage and quiescent currents due to reduced gate oxide thickness and increased subthreshold conduction, severely degrading efficiency and system reliability. This work presents a temperature-adaptive Low Dropout (LDO) regulator architecture specifically designed for ultra-low power IoT applications. In contrast to conventional fixed-reference LDOs, the proposed design dynamically adjusts its output voltage based on die temperature using a composite temperature-sensitive reference, synthesized by combining a process-tunable bandgap reference with a Complementary-To-Absolute-Temperature (CTAT) voltage. The designed regulator supports dual-mode operation, providing 1.8 V and 1.2 V from a 2–3.3 V battery supply. The proposed architecture has been simulated and verified using the 45 nm Cadence technology node. Simulation results confirm its temperature-dependent performance, demonstrating a smooth voltage drop from 1.99 V at -40 °C to 1.65 V at 125 °C under a nominal 1.8 V supply. For a nominal 1.2 V output, the voltage scales from 1.27 V to 0.93 V, with 1.13 V at 25 °C. These results substantially outperform conventional fixed-reference LDOs. The proposed architecture is highly relevant for modern IoT edge devices, wearables that demand ultra-low power operation, extended battery life, and consistent performance in thermally dynamic environments.

Keywords-Low Dropout (LDO) regulator; low leakage current; Complementary-To-Absolute-Temperature (CTAT) voltage; low quiescent current

I. INTRODUCTION

System-On-Chip (SOC) design faces significant challenges in reducing the power consumption, as most devices are powered by batteries. The effective management of power at the device level is one of the most effective methods of managing power at the SOC level. The main advantages of low power dissipation include the extension of battery life and the reduction in battery cost within the system, which are critical for Internet of Things (IoT) devices used in wireless, mobile, and automotive systems [1]. Power dissipation can be defined in terms of three basic components in the devices switching power, static (or quiescent) power, and leakage power.

Switching power is mainly dependent on the supply voltage, the switching frequency, and the capacitive load in the system. The static power, often represented by the quiescent current, is the minimum current required for a device to be in an active state. The leakage current is due to leakage in the device it is in the off state. As the devices operate at higher ambient temperature of ~125 °C, the junction temperature will be higher due to the internal power dissipation [2]. This increase in temperature may cause further increase in leakage current and die heating. It is possible that the device may incur damage due to die heating. Therefore, a mechanism is used to detect the internal die temperature and reduce the power at

higher junction temperatures enabling the device to continue functioning [3-5].

The architecture must be defined in such a manner as to ensure minimal power dissipation. The following equation is used to calculate the power:

$$P = V_{DD}^2 * F * C_L \quad (1)$$

Equation (1) shows that power dissipation is directly proportional to the square of the supply voltage (V_{DD}). Therefore, it is required to generate the appropriate supply voltage using a linear or a switching regulator. Both static and switching power components can be reduced by reducing the supply, as shown in (1) [6, 7].

In this work, we present a Low Dropout (LDO) regulator architecture that introduces a temperature-compensated reference voltage, which decreases with temperature. This results in a gradual reduction in output voltage of LDO as temperature increases, effectively minimizing leakage and quiescent power without sacrificing regulation precision or stability. The proposed solution is particularly well-suited for ultra-low-power IoT environments characterized by significant temperature variations. Real case example includes a Bluetooth Low Energy (BLE) SoC used for short-range wireless communication, typically powered by a coin-cell battery or energy harvesting source with strict energy constraints. In deep submicron CMOS, such as the 45 nm used in our design, the leakage power becomes dominant at elevated temperatures. For instance, the subthreshold leakage doubles approximately every

10 °C increase. A BLE SoC in standby or sleep mode, where most blocks are idle, can lose over 30–50% of its energy budget to leakage alone when operating above 85 °C.

The proposed LDO dynamically reduces the output voltage with temperature using a Complementary-To-Absolute-Temperature (CTAT)-based reference. Reducing V_{DD} at elevated temperatures can yield up to 3-5 times reduction in leakage current. This directly reduces power and translates to longer battery life, less thermal stress, and better sustainability.

The major contributions of this work include:

- We conducted an in-depth study of traditional LDO architectures, identifying their limitations in terms of temperature adaptability and power efficiency for modern IoT applications.
- Successfully designed essential analog components, including a precise bandgap reference circuit, a current sense circuit, and a CTAT generator, all of which are critical for achieving a thermally adaptive control mechanism.
- An innovative LDO regulator architecture was developed that leverages a temperature-dependent reference voltage. This architecture enables dynamic modulation of the output voltage across varying temperatures, thereby enhancing power efficiency.

Table I presents a detailed comparison of LDO architectures and techniques for IoT applications.

TABLE I. LITERATURE SURVEY: COMPARISON OF LDO ARCHITECTURES AND TECHNIQUES FOR IOT APPLICATIONS

Ref	Architecture/ Technique	Key Features/ Methods	Pros	Cons	Quiescent Current (I _q)	Operating Temperature Range (°C)
[2]	Conventional PMOS LDO	Fixed bias, large pass device	Simple design, mature technology	High leakage, poor high-temperature stability	~50–100 μA	-40 to 125
[8]	Body-biased LDO	Adaptive body bias	Low leakage, better thermal response	Complex substrate control	~20–30 μA	-40 to 125
[6]	DTMOS-based LDO	Dynamic body tied to gate	Leakage suppression, better temperature resilience	Risk of instability at high frequencies	~10–30 μA	-40 to 125
[9]	Adaptive bias LDO	Load- and temperature-dependent bias	Low I _q , improved dynamic power	Vulnerable to load transients	~1–5 μA	-40 to 125
[10]	Capacitor-less LDO	Internal compensation, small load capacitor	Tiny area, fast transient response	Moderate PSRR degradation at temperature extremes	~1–5 μA	-40 to 85
[11]	Ripple cancellation LDO	Feedforward ripple suppression	Excellent PSRR across frequencies	Increased complexity and static power	~15–20 μA	-40 to 125
[12]	Temperature-compensated bias LDO	Temperature-stabilized current mirrors	Stable operation over temperature	Increased area, moderate power	~20–50 μA	-40 to 125

a. PSRR: Power Supply Rejection Ratio.

b. DTMOS: Dynamic Threshold MOS.

From Table I, it is evident that conventional and even moderately adaptive LDO architectures are insufficient for the extreme low-power and high-temperature operation demands of modern IoT applications. High-speed SoCs operating at frequencies exceeding 200 MHz experience significant increases in current consumption at elevated junction temperatures, resulting in increased power dissipation.

According to the power equation $P = V * I$, the temperature-induced rise in current directly contributes to increased power loss. Therefore, scaling the supply voltage of the SoC, regulated by an LDO, is an effective approach to maintain or reduce power consumption at the SoC level in IoT applications. Techniques like simple adaptive biasing, body biasing, or ripple cancellation alone cannot guarantee thermal resilience

without incurring higher static power consumption or area penalties. Consequently, the integration of a current sense circuit combined with a CTAT generator emerges as the most effective strategy. This combination enables a thermally adaptive control mechanism where the regulator dynamically adjusts its biasing based on thermal conditions, drastically minimizing quiescent current and preventing unnecessary power loss even at elevated temperatures (above 100 °C). The proposed architecture, which leverages dynamic load sensing and temperature-compensated reference generation, achieves ultra-low power operation while maintaining excellent thermal performance, making it ideally suited for next-generation battery-powered, harsh-environment IoT systems.

II. CONVENTIONAL LINEAR LOW DROPOUT REGULATOR

Linear LDO regulators are critical components in power management for analog and IoT systems, valued for their low-noise performance and simplicity [13]. The conventional LDO architecture, shown in Figure 1, comprises an Error Amplifier (EA), a pass device (M_P), a feedback resistor (R_1 and R_2), and a load (C_{OUT} and I_{LOAD}).

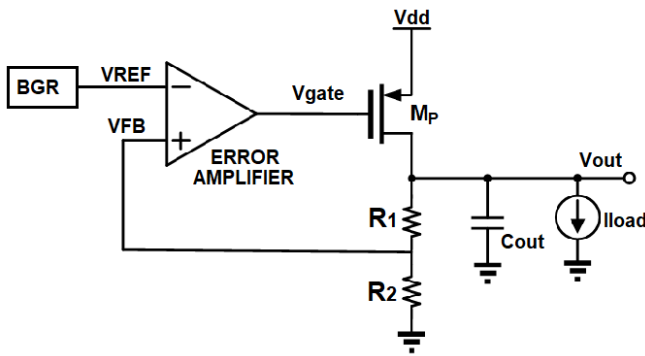


Fig. 1. Conventional LDO architecture.

The error amplifier compares the feedback voltage V_{FB} , which is obtained by scaling the output voltage through R_1 and R_2 , with a constant reference voltage V_{REF} . The amplifier regulates the internal resistance of the pass transistor M_P such that the error $V_{FB} - V_{REF}$ is minimal, or ideally zero. A PMOS transistor is preferred as the pass element due to its lower dropout voltage, reduced quiescent current, minimal headroom requirements, and superior performance at low supply voltages characteristics that align well with the demands of modern low-power IoT systems. The output voltage of the conventional LDO is defined by the below equation:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right) \quad (2)$$

While this configuration maintains stability across supply and process variations, it lacks adaptability under temperature changes [14]. As the temperature rises, both leakage and quiescent currents increase, which in turn increases power dissipation and reduces efficiency. Additionally, the fixed V_{REF} offers no mechanism for thermal compensation, making conventional LDOs unsuitable for thermally constrained

environments [15], such as battery-powered IoT devices, motivating the need for improved architectures with better thermal adaptability and power efficiency.

III. PROPOSED TEMPERATURE-ADAPTIVE LOW DROPOUT ARCHITECTURE

Emerging SoC and Application-Specific Integrated Circuit (ASIC) designs increasingly rely on battery-powered supplies operating at standard voltage levels, such as 1.2 V, 1.8 V, and 3.3 V. However, as process nodes scale down, power dissipation—particularly leakage and static, as well as dynamic switching power—becomes a critical concern. To address these issues, we propose a temperature-adaptive LDO architecture capable of dynamically adjusting its output voltage in response to die temperature. To enable temperature adaptability, the V_{REF} from the bandgap reference circuit is combined with a CTAT voltage, derived from an on-chip temperature sensor circuit, to produce a temperature-modulated reference V_{REF_T} .

As shown in Figure 2, the proposed architecture integrates a bandgap reference (BGR) for temperature-independent voltage generation, and a CTAT voltage from an on-chip temperature sensor. The combination of these two sources yields a temperature-dependent reference voltage V_{REF_T} , enabling the LDO to respond dynamically to thermal variations. The circuit uses two branches: one driven by the temperature-stable V_{REF} and the other by the CTAT voltage V_{CTAT} . Both branches employ a common-source configuration with source degeneration resistors, R_1 and R_2 , to generate the transconductance terms:

$$G_{m1} = \frac{I_1}{V_{REF}} = \frac{g_{m1}}{1 + g_{m1} \cdot R_1} \quad (3)$$

$$I_1 = \frac{V_{REF}}{R_1} \quad (4)$$

$$G_{m2} = \frac{I_2}{V_{CTAT}} = \frac{g_{m2}}{1 + g_{m2} \cdot R_2} \quad (5)$$

$$I_2 = \frac{V_{CTAT}}{R_2} \quad (6)$$

The generated V_{REF_T} is amplified by an additional gain stage. This step-up ensures that the temperature-modulated reference voltage is sufficient to drive the LDO output stage.

A. Complementary-To-Absolute-Temperature Voltage Generation

The CTAT voltage (V_{CTAT}) is generated by an on-chip temperature sensor, as shown in Figure 2. The base-emitter (V_{BE}) of the Bipolar Junction Transistor (BJT) exhibits CTAT behavior due to the variation in the intrinsic carrier concentration n_i of silicon, which is given by:

$$n_i^2 \propto T^3 e^{-E_g/KT} \quad (7)$$

As the temperature increases, n_i^2 increases rapidly, leading to a decrease in V_{BE} :

$$V_{BE} = V_{CTAT} = \frac{KT}{q} \ln \left(\frac{N_A \cdot N_D}{n_i^2} \right) \quad (8)$$

Since V_{BE} decreases with increasing temperature, it serves as a reliable CTAT reference in the proposed design.

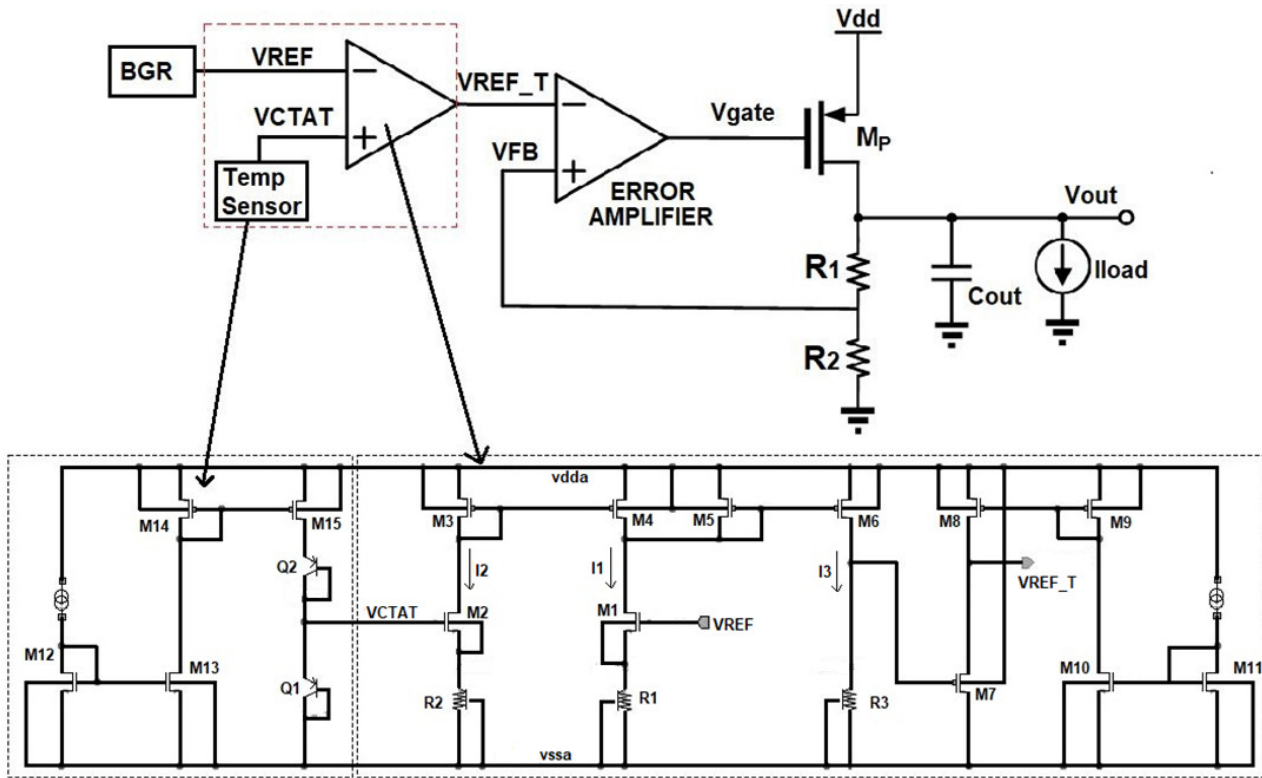


Fig. 2. Proposed temperature-adaptive LDO architecture.

B. Bandgap Reference Design

The reference voltage V_{REF} used in the proposed architecture is generated by the bandgap reference circuit, as shown in Figure 3. The bandgap voltage V_{REF} can be trimmed to get the desired temperature curvature. This trimming can be done by modifying the ratio of R_2/R_1 to achieve the right temperature coefficient. Since the V_{REF} output of BGR is also one of the sources of error for LDO output accuracy, it is important to have a high accuracy BGR with 1% variation in V_{REF} .

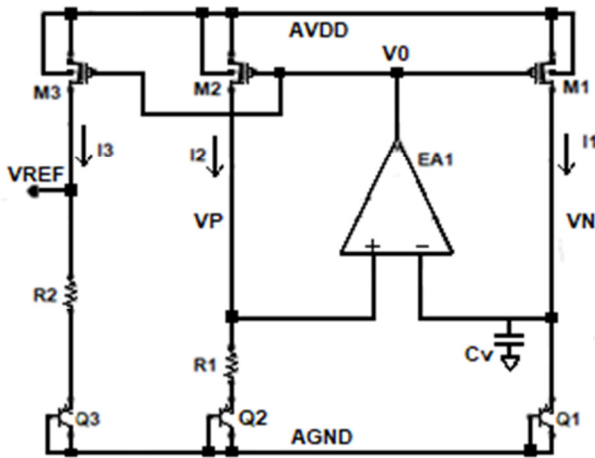


Fig. 3. Bandgap reference circuit used to generate a reference voltage V_{REF} .

In the present design, the base-emitter voltage of Q1 ($V_{EB}(Q1)$, or V_N) is made equal to voltage V_p using the error amplifier EA1. By utilizing transistors of equal dimensions, the circuit ensures that currents I_1, I_2, I_3 are equal. Under these conditions, the output of the BGR is defined as:

$$V_{REF} = V_{EB}(Q3) + \frac{R_2}{R_1} \cdot (\ln(N) \cdot V_T) \tag{9}$$

C. Mathematical Analysis of Temperature-Dependent Output Voltage

The LDO reference voltage V_{REF_T} is derived by combining the two voltages of (8) and (9):

$$V_{REF_T} = V_{REF} + A * V_{CTAT}(T) \tag{10}$$

$$V_{REF_T}(T) = V_{REF} + A * (V_{CTAT}(0) + \alpha T) \tag{11}$$

where $V_{CTAT}(0)$ is the CTAT voltage at 0 °C, α is a negative temperature coefficient, and A is a gain coefficient.

The LDO output voltage $V_{OUT}(T)$ is given by:

$$V_{OUT}(T) = V_{REF_T}(T) \left(1 + \frac{R_1}{R_2}\right) \tag{12}$$

$$V_{OUT}(T) = (V_{REF} + A * V_{CTAT}(0)) + A \alpha T * \left(1 + \frac{R_1}{R_2}\right)$$

In the above equation, the term $V_{REF} + A * V_{CTAT}(0)$ is constant:

$$V_{OUT}(T) = (\text{constant} + A \alpha T) * \left(1 + \frac{R_1}{R_2}\right) \tag{13}$$

$$\frac{dV_{OUT}}{dT} = A \alpha * \left(1 + \frac{R_1}{R_2}\right) \quad (14)$$

Since α is a negative constant, it can be deduced that V_{OUT} decreases with increasing temperature, which is beneficial for limiting leakage current and thermal stress. As the temperature rises, the internal die leakage current increases exponentially, potentially leading to thermal runaway or localized hotspots. By modulating the supply voltage downward in response to increasing die temperature, this risk is effectively mitigated, leakage power is reduced, and overall thermal reliability is enhanced, without compromising functional performance.

D. Mathematical Analysis of Power Loss in the Proposed Design

Considering (13), the $V_{OUT}(T)$ is given by:

$$V_{OUT}(T) = \text{constant} * \left(1 + \frac{R_1}{R_2}\right) + A \alpha T * \left(1 + \frac{R_1}{R_2}\right)$$

Let the term $\text{constant} * \left(1 + \frac{R_1}{R_2}\right)$ be designated as X and $\alpha A * \left(1 + \frac{R_1}{R_2}\right)$ be designated as Y. The above equation can then be written as:

$$V_{OUT}(T) = X + YT \quad (15)$$

$$\frac{dV_{OUT}}{dT} = Y \quad (16)$$

The power loss in an LDO is given by:

$$P_{LOSS}(T) = (V_{IN} - V_{OUT}(T)) * I_{LOAD}$$

Then:

$$\frac{dP_{LOSS}}{dT} = -\frac{dV_{OUT}}{dT} * I_{LOAD} \quad (17)$$

$$\frac{dP_{LOSS}}{dT} = -\alpha A * \left(1 + \frac{R_1}{R_2}\right) * I_{LOAD} \quad (18)$$

The above equation indicates that power loss decreases as temperature increases. This is beneficial, as it reduces power loss at higher temperatures, where thermal stress and leakage are usually more problematic.

Table II demonstrates that the proposed temperature-adaptive LDO exhibits superior performance in comparison to conventional LDO architectures with regard to thermal adaptability, power efficiency, and load regulation. While conventional LDOs are designed to provide a fixed output voltage, the proposed design intentionally allows the output to vary with temperature to address leakage power challenges in advanced CMOS nodes. As the temperature rises, leakage currents (subthreshold, junction, and gate) increase exponentially, especially in 45 nm technology. By allowing a controlled reduction in output voltage at higher temperatures, the LDO reduces the overdrive across transistors, thereby minimizing leakage current and improving overall power efficiency. This behavior is particularly beneficial for IoT and SoC applications, where power and thermal constraints are predominant. The use of a temperature-adaptive reference, which combines bandgap and CTAT voltages, ensures that the output variation is predictable and within safe operating limits, maintaining functionality while achieving significant power savings. It is important to note that dynamic output voltage is

not a drawback; rather, it is a deliberate strategy for thermal and power optimization.

TABLE II. COMPARISON OF CONVENTIONAL LDO WITH PROPOSED WORK

Feature	Conventional LDO	Proposed work
Thermal adaptability	No compensation for temperature variation	Adaptive reference voltage decreases slightly with temperature
Reference voltage	Constant $V_{REF}=1.2$ V	Adaptive $V_{REF,T} = V_{REF} + A * V_{CTAT}$
Power loss	Fixed power loss $P_{LOSS}=I_{LOAD} * (V_{IN} - V_{OUT})$	Power loss reduces as V_{OUT} adapts with temperature
Load regulation	Moderate; degrades with temperature	Improved due to dynamic feedback from temperature sensor
Circuit complexity	Simple design	Moderate complex

IV. SIMULATION RESULTS

The proposed LDO architecture utilizes a temperature-adaptive reference voltage ($V_{REF,T}$) to dynamically regulate the output supply, thereby enabling a reduction in active, quiescent, and leakage currents as die temperature increases without degrading performance. $V_{REF,T}$ is generated by summing a constant reference (1.225 V) with a CTAT component (V_{CTAT}) exhibiting a temperature coefficient of approximately -2 mV/°C, as shown in Figure 4. This negative slope allows the output voltage to scale down at higher temperatures, thereby minimizing power dissipation.

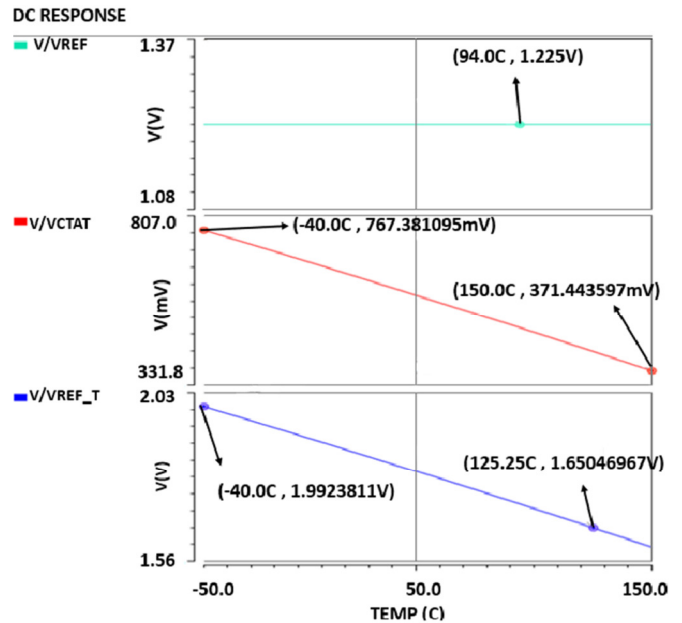


Fig. 4. Variation of the reference voltage $V_{REF,T}$ with temperature.

A. Variation of the LDO Output Voltage (1.8 V) Across Temperature

Figure 5 illustrates the variation of the LDO output V_{LDO} for a nominal 1.8 V regulated output supply under different SoC operation modes at elevated temperatures. At -40°C , the output voltage reaches 1.99 V, decreases to 1.86 V at 25°C , and further drops to 1.65 V at 125°C . This downward scaling of the supply voltage at elevated temperatures helps suppress static, switching, and leakage currents, improving power efficiency.

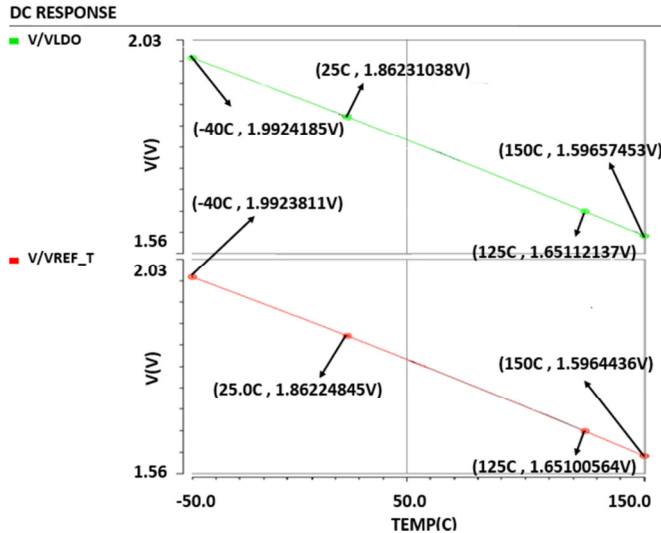


Fig. 5. Variation of the LDO output voltage V_{LDO} (nominal 1.8 V) with temperature.

B. Variation of the LDO Output Voltage (1.2 V) Across Temperature

The proposed architecture also facilitates the generation of a regulated 1.2 V output by appropriately selecting the reference voltage, as illustrated in Figure 6.

Table III shows the variation of V_{LDO} across temperature for both 1.8 V and 1.2 V supplies. The data indicate that the supply is minimum at the highest temperature. As described in (1), power dissipation is proportional to V_{DD}^2 ; therefore, reducing the supply voltage with temperature leads to meaningful energy savings. This makes the proposed LDO regulator highly suitable for always-on and thermally constrained IoT applications.

TABLE III. LDO OUTPUT VOLTAGE ACROSS TEMPERATURE FOR 1.2 V AND 1.8 V SUPPLIES

Temperature (°C)	V_{LDO} regulated at 1.8 V	V_{LDO} regulated at 1.2 V
-40	1.99 V	1.27 V
25	1.86 V	1.13 V
125	1.65 V	0.93 V

As shown in Table IV, prior works [12, 16, 17] maintain a near-constant output voltage across temperature, with minimal droop at 125°C [18]. In contrast, the proposed LDO introduces a controlled voltage drop of 0.34 V to actively reduce leakage

and quiescent currents at high temperatures. This adaptive behavior significantly improves power efficiency in advanced CMOS nodes, where leakage dominates. While earlier designs focus on voltage stability, the proposed approach prioritizes thermal-aware power savings, offering a more effective solution for always-on, low-power IoT applications.

TABLE IV. COMPARISON OF PRESENT WORK WITH PRIOR RESEARCH

Temperature (°C)	[12]	[16]	[17]	Present work
-40	1.209 V	1.2 V	1.18 V	1.27 V
25	1.208 V	1.2 V	1.17 V	1.13 V
125	1.207 V	1.19 V	1.15 V	0.93 V
Voltage drop @ 125°C	0.002 V	0.01 V	0.03 V	0.20 V

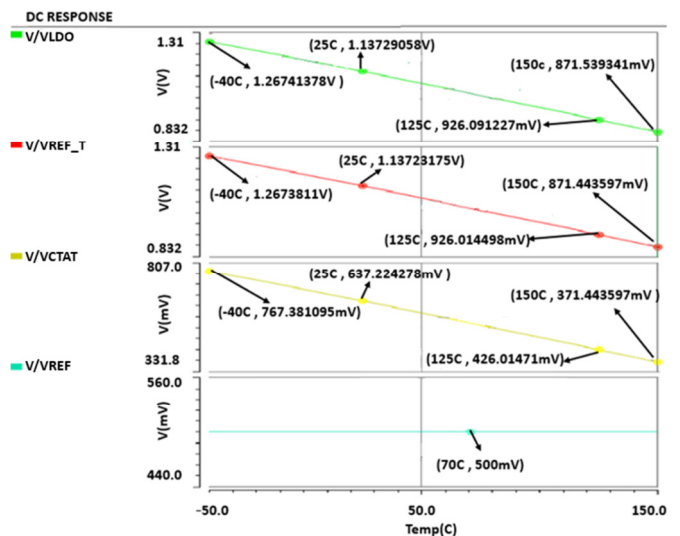


Fig. 6. Variation of the LDO output voltage V_{LDO} (nominal 1.2 V) with temperature.

V. CONCLUSION

Advanced CMOS scaling for Internet of Things (IoT) devices has intensified the need for thermally-aware power management, as elevated temperatures significantly increase leakage and quiescent currents, undermining power efficiency and reliability. This paper presents a temperature-adaptive Low Dropout (LDO) regulator tailored for low-power IoT systems. The proposed design employs a composite temperature-sensitive reference, generated by combining a tunable bandgap with a Complementary-To-Absolute-Temperature (CTAT) voltage, enabling dynamic voltage scaling with temperature. The proposed LDO regulator supports dual-mode operation, delivering regulated outputs of 1.8 V and 1.2 V from a battery supply ranging from 2 V to 3.3 V. In addition to voltage scaling, the design also adjusts the output voltage based on die temperature, thereby reducing leakage current at high temperatures. For a nominal 1.8 V output, the regulator provides 1.99 V at -40°C , 1.86 V at 25°C , and 1.65 V at 125°C . Similarly, under a nominal 1.2 V output, the regulator output varies from 1.27 V to 0.93 V across the same temperature range, with 1.13 V at room temperature. These

results validate the regulator's ability to maintain robust operation across a wide temperature spectrum. The design also achieves significant quiescent current reduction at elevated temperatures, contributing to overall power efficiency. With minimal additional circuitry, the architecture remains compact and scalable, offering reliable performance under Process, Voltage, and Temperature (PVT) variations. These features make the proposed solution highly suitable for always-on, energy-constrained IoT systems requiring low power and high thermal adaptability.

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