A Robust Induction Motor Drive Using a Cascaded H-Bridge Inverter Under Hybrid Reaching Law-Based Control

Thanh Lam Le
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Vietnam
lamlethanh@hcmute.edu.vn (corresponding author)

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ABSTRACT

A Hybrid Reaching Law (HRL)-based signal generation strategy is proposed to improve the modulation quality of a nine-level Cascaded H-Bridge (CHB) inverter-fed Induction Motor (IM) drive. The approach avoids the use of carrier-based waveforms by directly converting continuous control signals into discrete switching commands through quantization, enabling smooth voltage synthesis with reduced harmonic distortion. By combining the Sliding Mode Control (SMC) principles with a nonlinear reaching mechanism, the method enhances the robustness against the model uncertainties and external disturbances while effectively mitigating chattering. The control algorithm is designed for real-time digital implementation and is inherently compatible with modular CHB inverter architectures. Experimental validation using a Texas Instruments F28379D DSP and a 1 HP three-phase squirrel-cage IM demonstrates a stable voltage generation, acceptable Total Harmonic Distortion (THD), and reliable steady-state performance across different voltage levels. The proposed technique provides a practical and efficient solution for high-precision control in multilevel inverter-based motor drive systems.

Keywords-induction motor drive; nine-level cascaded H-bridge inverter; nonlinear control; robust control

I. INTRODUCTION

Multilevel inverters have attracted significant attention in motor drive applications due to their ability to generate high-quality voltage waveforms with reduced THD and lower dv/dt stress on motor windings [1, 2]. Among the various topologies, the CHB inverter stands out as an attractive solution due to its modular structure, scalability, fault tolerance, and seamless integration with distributed energy sources, such as battery packs and photovoltaic arrays [3-5]. These features make CHB inverters especially suitable for high-voltage industrial drive systems, where the compactness, redundancy, and waveform quality are critical [6, 7]. Although the hardware advantages of CHB inverters are well established, the overall system performance is dependent on the modulation strategy used to convert the control objectives into switching commands [8]. Traditional methods, such as sinusoidal Pulse-Width Modulation (PWM) [9] and space vector modulation [10], typically rely on carrier-based signals and face limitations in digital implementations with multiple cascaded levels [11, 12]. These limitations include increased switching losses, resolution mismatches, and control delays, particularly under dynamic loading or high-speed operation [13, 14].

IMs remain a cornerstone of industrial drive systems thanks to their robustness, cost-effectiveness, and wide availability [15]. They are widely employed across various sectors, including automation, electric vehicles, and renewable energy systems [16, 17]. However, their inherently nonlinear and coupled dynamics pose significant control challenges, particularly in the presence of parameter variations and limited sensing capabilities [18]. SMC has gained popularity in power converters and motor drive applications due to its strong robustness against the model uncertainties and external disturbances [19-22]. Nevertheless, classical SMC methods often suffer from chattering and implementation difficulties arising from the discontinuity of the control signal [23]. To overcome these issues, advanced reaching laws have been developed to enhance the convergence smoothness while maintaining robustness [24, 25]. Among them, the HRL adopted in this study is particularly well-suited for digital multilevel modulation, as it offers a favorable balance between the fast convergence and continuous control behavior.

To overcome the limitations of conventional carrier-based modulation in digital CHB inverter control, this paper presents a novel HRL-based signal generation method. By directly mapping a continuous control signal into discrete switching states via quantization, the approach eliminates the carrier waveforms, reduces the chattering, and improves the modulation resolution. Unlike existing methods, it unifies the nonlinear control and modulation in a digitally efficient structure tailored for multilevel drives. The experimental validation on a DSP-controlled nine-level CHB inverter

confirms stable voltage generation, low harmonic distortion, and robust motor performance across the voltage levels. This integrated approach, particularly in a high-level CHB setup, has been rarely explored in prior literature and is experimentally validated in this work.

II. SYSTEM DESCRIPTION AND NINE-LEVEL CASCADED H-BRIDGE INVERTER TOPOLOGY

The system under study consists of a three-phase nine-level CHB inverter supplying a squirrel-cage IM. Each phase comprises four series-connected single-phase H-bridge cells, each powered by isolated DC sources. This modular topology enables a high-resolution output voltage synthesis, making it well-suited for medium-voltage motor drives. A high-level controller generates real-valued modulation signals $u_x(t)$ for each phase $x \in (a, b, c)$, which are converted by a PWM block into gating signals for the inverter switches. The inverter output voltages are then applied to the stator terminals of the motor. The system assumes balanced three-phase conditions and uses isolated modules to enhance the fault tolerance and integration flexibility with distributed DC sources. The overall architecture of the system is illustrated in Figure 1, where the HRL-based controller generates modulation commands that are fed into a quantization-based PWM block. These signals are used to switch the nine-level CHB inverter, which in turn supplies the IM.

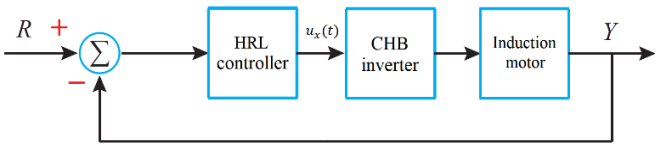


Fig. 1. HRL-based CHB inverter-fed IM drive system.

As depicted in Figure 2, the inverter's three-phase legs (a, b, c) synthesize the output voltages by summing the instantaneous outputs of their four corresponding H-bridge cells:

$$v_a(t) = v_{a1}(t) + v_{a2}(t) + v_{a3}(t) + v_{a4}(t) \quad (1)$$

$$v_b(t) = v_{b1}(t) + v_{b2}(t) + v_{b3}(t) + v_{b4}(t) \quad (2)$$

$$v_c(t) = v_{c1}(t) + v_{c2}(t) + v_{c3}(t) + v_{c4}(t) \quad (3)$$

where $v_{ai}(t)$, $v_{bi}(t)$, and $v_{ci}(t)$ denote the output voltages of the i-th H-bridge cell in phases a, b, and c, respectively, with $i = 1, 2, 3, 4$ for each phase.

Each H-bridge cell consists of four Insulated Gate Bipolar Transistors (IGBTs) and their corresponding anti-parallel diodes, enabling bidirectional current conduction and full-bridge switching functionality. The individual DC voltage sources associated with each cell are assumed to be equal and constant:

$$\begin{aligned} V_{dca1} &= V_{dca2} = V_{dcam} = V_{dc} \\ V_{dcb1} &= V_{dcb2} = V_{dcbm} = V_{dc} \\ V_{dcc1} &= V_{dcc2} = V_{dccm} = V_{dc} \end{aligned} \quad (4)$$

where V_{dc} is the nominal DC-link voltage of each power cell.

By controlling the switching states of the IGBTs, each cell is capable of producing three discrete voltage levels: $+V_{dc}$, 0, and $-V_{dc}$. Therefore, when four such cells are connected in series per phase, the inverter can generate nine output voltage levels. For each phase $x \in (a, b, c)$, this results in a discrete set of possible phase voltages given by:

$$v_x(t) \in (-4V_{dc}, -3V_{dc}, \dots, 0, \dots, +4V_{dc}) \quad (5)$$

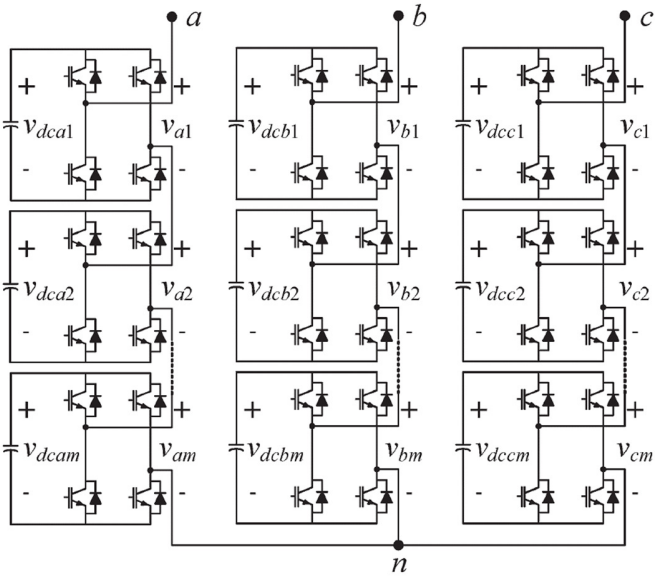


Fig. 2. Structure of the three-phase nine-level CHB inverter.

The bottom node n in Figure 2 serves as the common neutral point for all phase legs and acts as the reference for the line-to-neutral voltage. The symmetric CHB structure offers modularity, ease of implementation, fault tolerance, and high voltage quality. It supports scalable integration with isolated DC sources, like batteries or renewables. Though equal DC levels are assumed, the topology can be extended to asymmetric configurations for more voltage levels using fewer cells, at the cost of added control complexity and voltage imbalance.

III. CONTROL INTERFACE AND PWM GENERATION

The proposed strategy generates a real-valued control signal $\psi_k(t)$ for each inverter phase $k \in (a, b, c)$, produced by the outer-loop controller regulating motor speed or current. This signal serves as the primary input to the PWM block and is quantized into a discrete-level index $\Delta_k(t)$ to enable the mapping into switching states, according to the following rule:

$$\Delta_k(t) = \begin{cases} m-2, & \text{if } \psi_k(t) \geq m-2 \\ \lfloor \psi_k(t) \rfloor, & \text{otherwise} \end{cases} \quad (6)$$

where $m = 9$ is the total number of output levels per phase, and $\lfloor \cdot \rfloor$ denotes the floor function. This process ensures that the control signal is confined to a valid range of switching states available in the CHB topology. Subsequently, a comparator threshold level is defined as:

$$\Gamma_k(t) = \Delta_k(t) + \delta \quad (7)$$

where $\delta \in (0,1)$ is a tunable offset parameter used to center the PWM comparison logic. In this work, $\delta = 0.5$ is adopted to

achieve midpoint modulation symmetry and enhance the switching balance across phases.

The binary switching signal $G_{ki}(t)$ for the i-th submodule in phase k is generated by comparing the control signal with its corresponding comparator level:

$$G_{ki}(t) = \begin{cases} 1, & \psi_k(t) \geq \Gamma_k(t) \\ 0, & \text{otherwise} \end{cases} \quad (8)$$

These signals are subsequently mapped into gate pulses for the upper and lower switches of each H-bridge cell, enabling each module to contribute its corresponding voltage level. It is assumed that the controller generates $\psi_k(t)$ in normalized units within the range $\psi_k(t) \in [0, m-1]$, thereby allowing a seamless translation into the discrete switching states of a nine-level inverter.

The inverter uses gating signals $G_{ki}(t)$ to control each switch's operation, generating output voltages that closely track the reference with low switching losses and reduced harmonics. Unlike conventional methods, the proposed PWM eliminates the carrier waveforms by directly converting the controller outputs into switching actions, enabling an efficient digital implementation. This decentralized control improves flexibility and robustness for real-time motor drives. To support this objective, a nonlinear control scheme based on an HRL is designed to synthesize the modulation command $u_x(t)$ for each inverter phase $x \in (a, b, c)$. This real-valued signal serves as the direct input to the PWM generation block introduced earlier, enabling high-resolution voltage synthesis for an accurate motor control. The control objective in this study is to regulate the rotor speed $\omega_r(t)$ of the IM to track a reference trajectory $\omega_r^*(t)$, despite the model uncertainties and external load disturbances. Let the tracking error and its first derivative be defined as:

$$e_1(t) = \omega_r^*(t) - \omega_r(t), \quad e_2(t) = \dot{e}_1(t) \quad (9)$$

A first-order sliding surface is constructed to encapsulate the desired error dynamics, given by:

$$s(t) = e_2(t) + \eta e_1(t) \quad (10)$$

where $\eta > 0$ is a design parameter used to tune the convergence speed of the error towards the sliding manifold.

To drive the system trajectory toward the sliding surface $s(t) = 0$, an HRL is proposed as:

$$\dot{s}(t) = -\alpha |e_1(t)|^{\mu} - \beta e^{-\rho |e_1(t)|} \quad (11)$$

where $\alpha > 0$ is the fractional convergence gain, $\beta > 0$ is the exponential decay gain, $\rho \in (0,1)$ determines the exponential rate, and $\mu = \frac{q}{p} \in (0,1)$ with $p > q \in \mathbb{N}^+$ defines the nonlinearity level of the fractional term.

Substituting (10) into the closed-loop dynamics and enforcing the reaching condition $\dot{s}(t) = 0$, the continuous control signal $u_x(t)$ is derived from the mechanical dynamics $J\frac{d\omega_r}{dt} = T_e - T_L - B\omega_r$ as:

$$u_x(t) = -J\left(Be_2(t) + \eta B e_1(t) + \alpha |e_1(t)|^{\mu} + \beta e^{-\rho |e_1(t)|}\right) \quad (12)$$

where J is the total moment of inertia of the motor–load system, and B is the viscous friction coefficient as defined in the mechanical model. This formulation assumes that the control input $u_x(t)$ directly influences the electromagnetic torque T_e, which subsequently drives the rotor speed dynamics.

To analyze the stability of the proposed controller, a Lyapunov candidate function is introduced as:

$$V(t) = \frac{1}{2} s^2(t) \quad (13)$$

Taking the time derivative of $V(t)$ along system trajectories and substituting (11) yields:

$$\dot{V}(t) = s(t)\dot{s}(t) = -\alpha |e_1(t)|^{\mu} s(t) - \beta e^{-\rho |e_1(t)|} s(t) \quad (14)$$

The terms on the right-hand side are negative definite for $s(t) \neq 0$, as both α and β are strictly positive and $s(t)$ shares the sign of $e_1(t)$. Therefore, $\dot{V}(t) < 0$ except at the equilibrium $s(t) = 0$, establishing global asymptotic stability of the sliding surface and ensuring that the tracking error $e_1(t) \to 0$ as $t \to \infty$.

The structure in (11) combines a fractional power term for accelerating convergence in the transient phase and an exponentially decaying component to suppress chattering near the origin. This design enhances the tracking accuracy and ensures a smooth control behavior under varying operating conditions. Once generated, the continuous signal $u_x(t)$ is normalized and directly assigned to the modulation variable $\psi_k(t)$ in the PWM logic. The quantization and thresholding process therein translates $\psi_k(t)$ into discrete switching signals for each submodule in the CHB inverter. The proposed control strategy, built upon a rigorously designed HRL and supported by Lyapunov-based stability analysis, guarantees high-performance speed tracking, effective disturbance rejection, and seamless integration with modular digital implementation in multilevel inverter-fed motor drive systems.

IV. EXPERIMENTAL RESULTS

To evaluate the performance of the proposed HRL-based modulation approach, experiments are conducted on a three-phase IM system driven by a nine-level CHB inverter. The control algorithm is implemented in real-time using a Texas Instruments F28379D DSP development kit. The experimental setup employed a 1 HP three-phase squirrel-cage IM to emulate real-world drive conditions. The controller generates a real-valued modulation signal $u_x(t)$, which is directly utilized by a carrier-less PWM scheme to produce the gating signals for the inverter. Figure 3 presents the experimental setup, including the CHB inverter board, DSP hardware, oscilloscope, and the IM. The waveform measurements are recorded via oscilloscope probes at the output terminals of the inverter and motor during different test scenarios. The system operates under balanced conditions with symmetrical DC sources.

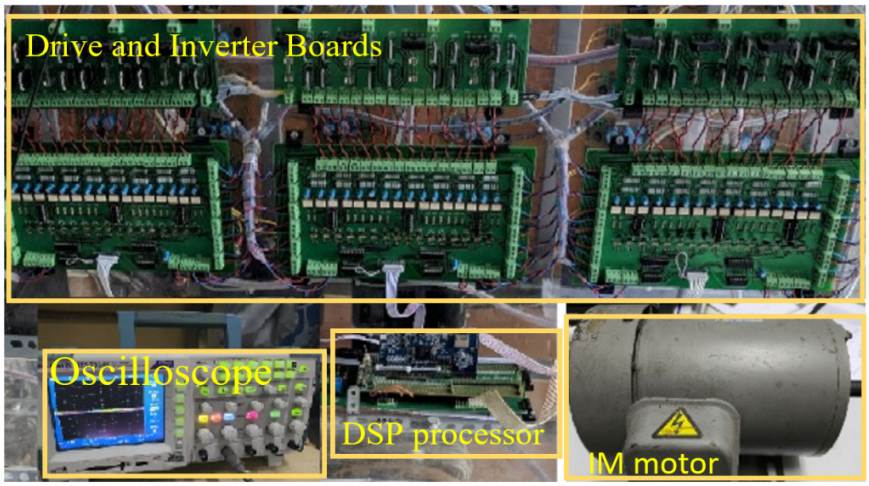
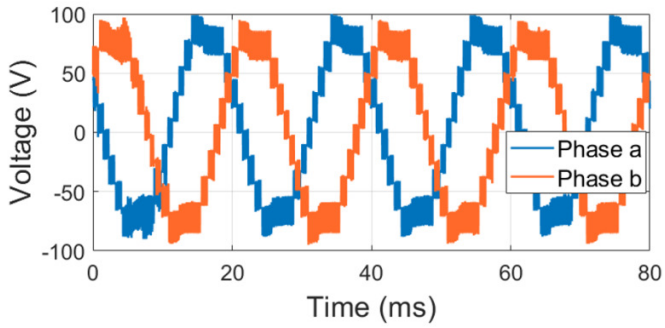
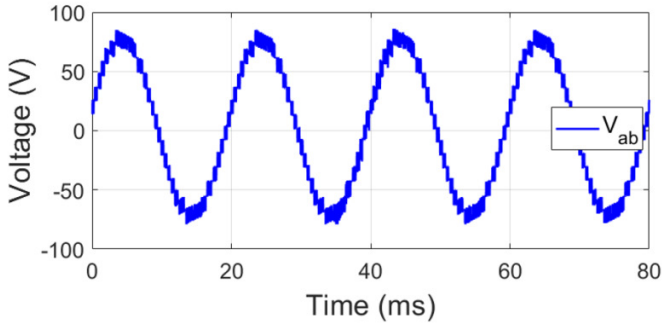


Fig. 3. Experimental testbench.



(a)



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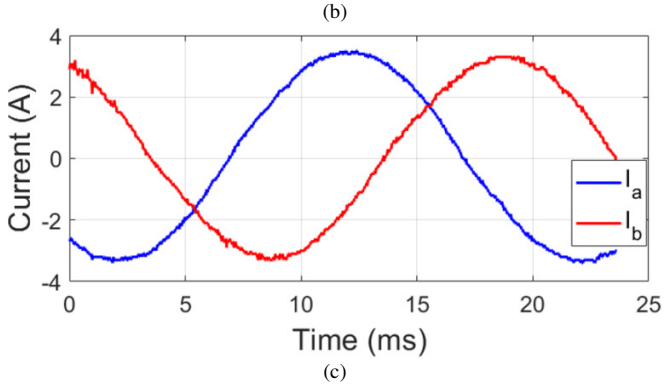
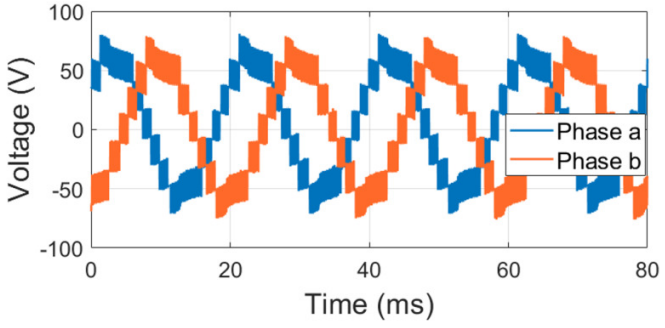
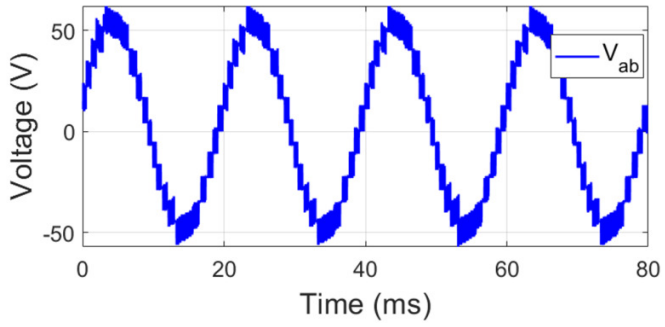


(c)

Fig. 4. Experimental results for test case A: (a) phase voltages, (b) line-to-line voltage V_{ab}, (c) phase currents i_a and i_b.



(a)



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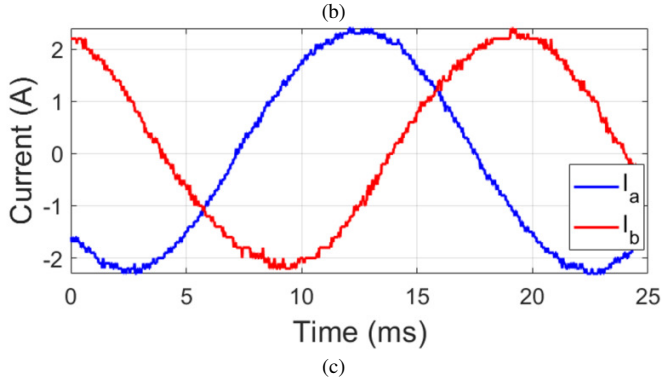

(c)

Fig. 5. Experimental results for test case B: (a) phase voltages, (b) line-to-line voltage V_{ab}, (c) phase currents i_a and i_b.

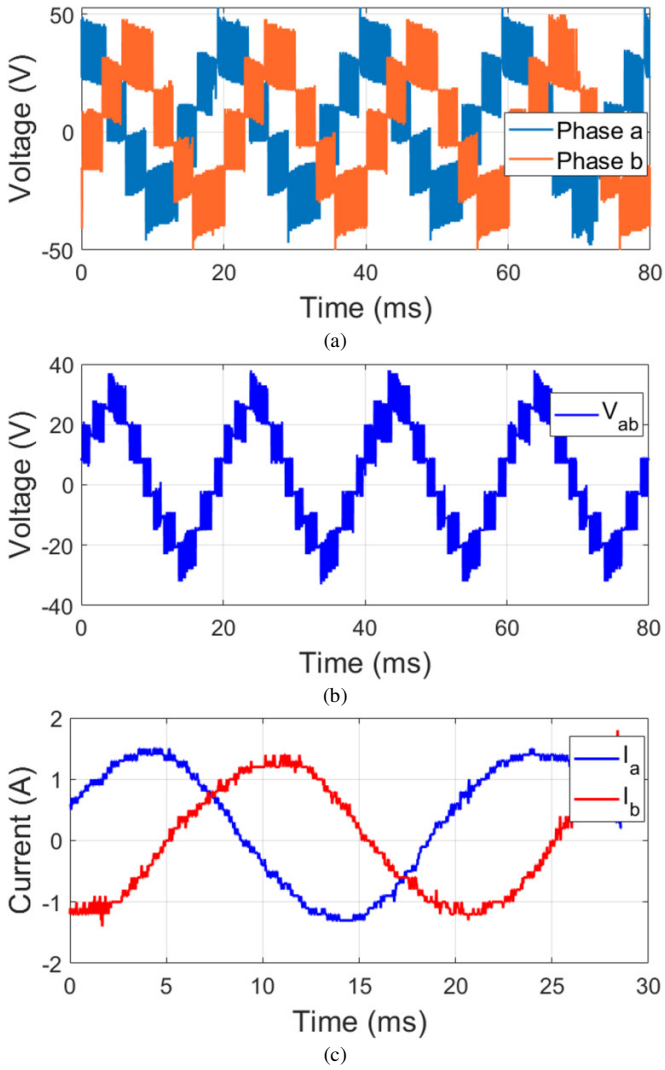

Fig. 6. Experimental results for test case B: (a) phase voltages, (b) line-to-line voltage V_{ab}, (c) phase currents i_a and i_b.

Figures 4-6 illustrate the system's performance under different voltage levels. In case A (high voltage), the phase voltages closely approximate sinusoids with clear multilevel steps, and the line voltage v_{ab} and phase currents i_a, i_b show low distortion and stable periodicity. The THD values are 20.2% (phase), 15.4% (line), and 9.6% (current), indicating high modulation fidelity. In case B (medium voltage), the output voltage decreases moderately, and the step resolution is slightly reduced. The phase voltages remain staircase-like, and the currents remain smooth. The THD rises to 22.4%, 20.2%, and 12.3%, reflecting increased but acceptable harmonic content. case C (low voltage) exhibits coarser voltage steps and slightly more distorted currents, with the THD increasing to 35%, 30.4%, and 17.9%, respectively. Despite this, the motor remains operational.

Figure 7 presents the FFT-based harmonic analysis. While case C supports operation, a prolonged exposure to high harmonic content may lead to thermal stress and torque ripple. Case A provides optimal performance, whereas case B offers a good trade-off for moderate-load conditions. Overall, the HRL-based control strategy enables accurate multilevel voltage generation and ensures stable motor performance across various voltage levels, making it suitable for motor drive applications.

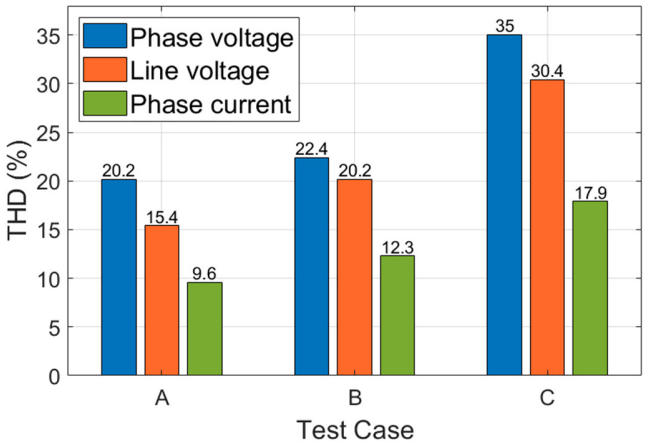

Fig. 7. THD analysis of phase voltage, line voltage, and current for test cases A-C.

V. CONCLUSION

A Hybrid Reaching Law (HRL)-based modulation technique is proposed for multilevel Cascaded H-Bridge (CHB) inverter-fed Induction Motor (IM) drives. By combining the robustness of Sliding Mode Control (SMC) with a continuous signal generation scheme, the approach eliminates the need for carrier waveforms and effectively mitigates switching chattering. The HRL formulation enables a smooth convergence and ensures reliable speed tracking under parameter variations and external disturbances. The experimental validation across multiple voltage levels confirms the stable voltage synthesis, low harmonic distortion, and consistent motor performance. The control algorithm is fully compatible with the digital implementation and is well-suited for modular CHB inverter architectures. Future research may explore extensions to asymmetric topologies, real-time fault-tolerant control, and adaptive HRL tuning for enhanced flexibility and robustness.

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