Fabrication of Si/CdTe Heterostructure via Vacuum Thermal Evaporation: Synthesis and Properties Characterization

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ABSTRACT

This study focuses on the investigation of a heterostructure fabricated using the Vacuum Thermal Evaporation (VTE) technique and presents the X-ray structural analysis of the compound obtained using the VTE method. The study also determines the optimum pressure and temperature for the production of silicon cadmium tellurium compound. The analysis showed that the Silicon–Cadmium Telluride (nSi–pCdTe) heterojunction, formed on a silicon substrate, consists of a CdTe epitaxial layer with an estimated thickness of approximately 10 μm, followed by a 2–3 μm interfacial transition region at the CdTe/Si interface. The heterostructure of nSi-pCdTe current-voltage (I–V) characteristics, capacitance-voltage (C–V), and spectral features were the main subjects of the investigation.

Keywords-CdTe; heterostructure; VTE; epitaxy; IV characteristics; spectral characteristics; heterojunction

I. INTRODUCTION

Photodetectors play a critical role in defense, industrial systems, healthcare devices, and scientific research [1-3]. These devices, which convert optical signals into electrical outputs, require fast response times, high signal-to-noise ratios, and wide linear dynamic ranges to be effective in applications, such as medical imaging, optical communication, and intrachip optical interconnections.

Among the materials used for photovoltaic devices [4-6], cadmium telluride (CdTe) is particularly promising due to its optimal bandgap of 1.51 eV and high optical absorption coefficient, making it well-suited as the active layer in photodetectors. Various techniques, including magnetron sputtering, thermal evaporation, and chemical bath deposition [7-11], are available for preparing CdTe thin films. VTE is favored for its ability to produce films under thermal equilibrium conditions with precise control over deposition parameters [12, 19]. This study focuses on the structural, optical, and electrical properties of CdTe films deposited on silicon substrates, highlighting their potential for photovoltaic manufacturing.

Efforts have concentrated on CdTe-Si heterostructures to combine the benefits of silicon solar cells with CdTe's unique properties, potentially enhancing solar energy conversion [13-22]. However, the significant lattice mismatch between CdTe and Si often introduces high defect densities at the interface. To overcome this issue, the use of intermediate transition layers as buffers has been explored. In this work, compositionally graded CdTe epitaxial layers are introduced on Si substrates—with layer thickness as a key parameter—to improve heterostructure quality [23, 24]. Additionally, the study examines the current-

voltage (I–V), capacitance-voltage (C–V), and spectral properties of CdTe epitaxial layers grown on polysilicon substrates, as well as the effects of indium (In) and silicon (Si) doping. By optimizing the deposition conditions and understanding the material crystallization process, this study aims to advance the development of high-performance Si/CdTe heterostructures for photovoltaic applications.

II. METHODS AND MATERIALS

Semiconductor thin films have predominantly been prepared by physical vapor deposition techniques [25]. The VTE method, as illustrated in Figure 1, is one of the simplest [26, 27]. The vapor is formed by heating either a solid material (sublimation, as used for As purification, while removing AsOx oxides) or a liquid melt (evaporation). With the introduction of more versatile deposition techniques, such as sputtering and CVD, VTE is now less widely used. However, VTE remains attractive for good glass-forming binary chalcogenides like As-S(Se), Ge-S(Se), because it is low-cost, relatively simple, reproducible, and capable of deposition over a large substrate area. VTE is the preferred technique for deposition of amorphous selenium (a-Se) for flat-panel X-ray detectors, nano-ionic memories (programmable metallization cell, using Ag-doped Ge-S, or Ge-Se), thin-film waveguides, and both hard and soft stamp-imprinting techniques [28, 29]. Film thicknesses are usually from tens of nanometers to hundreds of micrometers.

In this study, the Si-CdTe compound was grown using the VTE technique. Similar research has not been reported before, which demonstrates the novelty of the present work.

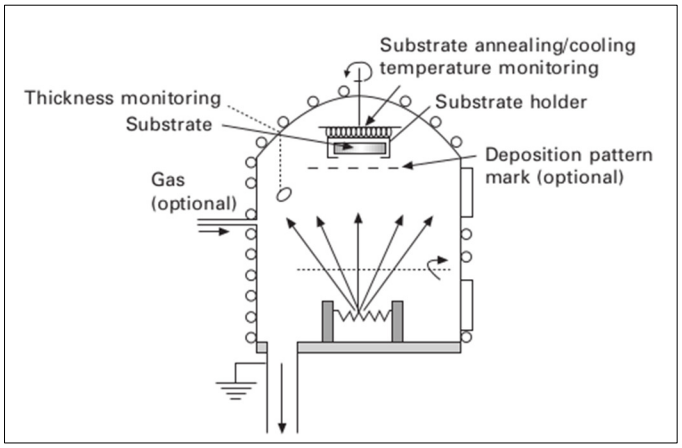

Fig. 1. Simple schematic representation of a VTE device.

The heating stage increases the mobility of species condensed on the substrate, permitting more relaxation to produce low-stress films. Cooling increases the effective quench rate of the incident species.

Figure 2 shows a simplified cosine distribution of evaporated species from a point source (bottom), and the corresponding thickness distribution of the film deposited on the substrate (top), where *dm*/*dA* is the mass *m* deposited per unit *A*, and *r* is the distance of the substrate from the source. The angles θ and φ are also depicted in Figure 2. The distribution depends on the form of the source (wire, spiral, cylinder, dimpled sheet, Al_2O_3 boat, SiO_2 crucible, etc.). The co-evaporation from two boats is possible, but is not commonly used for chalcogenide glasses. Co-evaporation has, however, been used for the deposition of some crystalline analogs. Thickness monitoring is performed by measuring a change in oscillation frequency of a quartz-crystal resonator. It is also common to use in-situ optical techniques, such as spectroscopic ellipsometry for simultaneous monitoring of the thickness and optical properties. The source-substrate distance is smaller than the mean free path *l* of the evaporated molecules: for example, for a molecule of typical 0.3 nm in diameter, l ≈ 100 m at 10^{-4} Pa.

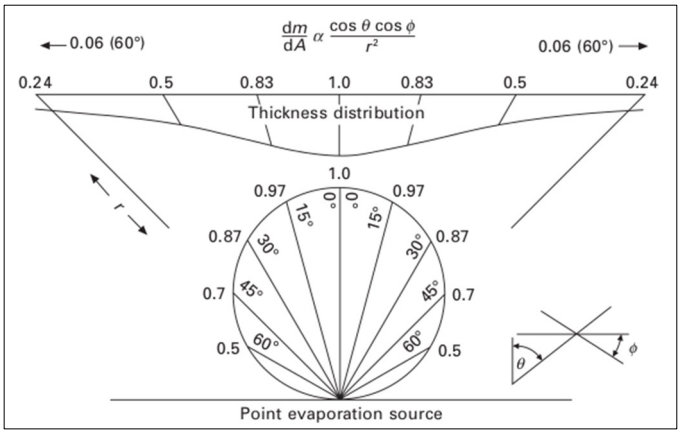

Fig. 2. Distribution of thickness for the deposited coating.

The Clausius-Clapeyron equation can be derived from the equality of the chemical potentials of two phases in thermodynamic equilibrium, describing the equilibrium vapor pressure P' at the evaporant surface, dependent on temperature T:

$$\frac{dP'}{dT} = \Delta H_v\left(v_g - v_c\right) \quad (1)$$

where ΔH_v is the latent heat of the phase transformation (vaporization), Δv_g and Δv_c are the molar volumes of the gaseous and condensed phases, respectively. The quantities ΔH_v, Δv_g, and Δv_c are functions of temperature T. The P'–T dependences are known for the elements in solid and liquid form. The vapor pressure P' increases sharply with temperature. For common metals, such as Pb, Ag, Au, Al, Cu, the temperature required for evaporation is as high as 1500 K. Materials, such as Pt, Mo, Al_2O_3, fused silica, etc., have very low vapour pressures and high melting temperatures; they can hardly be vaporized by conventional VTE, and are therefore used as materials for the boats containing the evaporant sources. At high temperatures, alloying between the material of the boat and the evaporant is a potential concern, but it can be avoided. For example, a boat made of W can withstand several depositions of Al, which otherwise alloys easily with many metals at high temperatures.

From the kinetic theory of gases, the impingement rate $N_i(m^{-2} \cdot s^{-1})$ of gas molecules on a surface is given by:

$$N_i = \frac{P}{\sqrt{2\pi mkBT}} \quad (2)$$

where m is the molecular weight, k_B is the Boltzmann's constant, and P is the gas pressure. Equation (2) applies to the residual gases and the evaporant molecules. Hertz (1882) and then Knudsen (1915) measured the evaporation rates of mercury and postulated an equation describing the net molecular evaporation rate N_e, now known as the Hertz–Knudsen equation:

$$N_e = \frac{\alpha_v(P'-P)}{\sqrt{2\pi mk_BT_e}} \quad (3)$$

where T_e is the evaporation temperature, P is the ambient pressure of the species in the evaporation chamber, and α_v is the evaporation coefficient. The quantity N_e in (3) can also be regarded as the impingement rate of the gas molecules based on the kinetic theory of gases, corrected for the returning molecules corresponding to gas pressure P and for the evaporation coefficient.

It can be observed that the maximum evaporation rate corresponds to the condition where $P = 0$ If $P = P'$i.e., under equilibrium conditions, there is no net evaporation. Evaporation is preferred only if $P \ll P'$, i.e., under non-equilibrium conditions. The evaporation coefficient α_v is defined as the ratio of the real evaporation rate in the evaporation chamber to the theoretically calculated values. The vacuum chamber in VTE usually operates at base pressures of less than 10^{-4} Pa. The crystallographic structure of the CdTe/Si heterostructures was examined using X-ray Diffraction (XRD), utilizing an Empyrean PANalytical diffractometer, as displayed in Figure 3. The instrument is equipped with a vertically mounted goniometer, a copper anode X-ray tube (λ = 1.5406 Å), and a high-resolution detector. Measurements were performed in the Bragg–Brentano geometry with a 2θ scan range of 10°–80°. This configuration allows the accurate identification of crystallographic phases, determination of lattice parameters, and evaluation of the polycrystalline nature of the deposited CdTe thin films.

The I–V characteristics of the Si/CdTe heterostructure were measured using the setup shown in Figure 4. A schematic diagram of the experimental circuit is presented in the upper left corner of Figure 4, while the corresponding laboratory arrangement is depicted in the photograph. The measurement system consisted of a regulated power supply, an ammeter, a voltmeter, a millivoltmeter (operated in conjunction with a thermocouple for potential temperature calibration), a resistance box, and a cryostat providing a vacuum level of 10^{-2} Torr, with the sample placed inside.

The Si/CdTe sample was mounted inside the cryostat, which enables measurements under controlled vacuum conditions. In the present study, however, all measurements were carried out at room temperature (300 K). The resistance box was employed to adjust the load resistance in the circuit, while the ammeter and voltmeter were used to record the current and voltage values across the heterostructure. The millivoltmeter, connected to the thermocouple, provided voltage readings that can be converted into temperature values if required.

(a) (b)

Fig. 3. (a) Empyrean PANalytical diffractometer with the protective glass doors closed, and (b) the instrument with the doors open, showing the measurement stage and goniometer assembly.

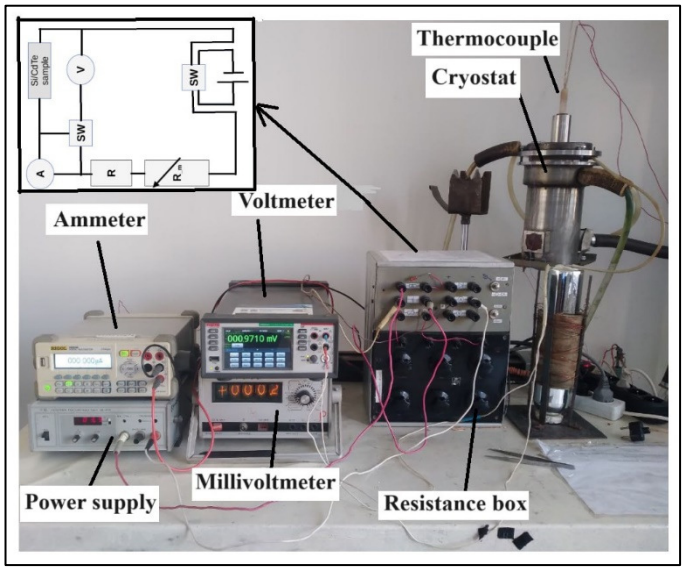

Fig. 4. Schematic diagram of the I–V measurement circuit (upper left corner) with the experimental actual setup.

The I–V characteristics were obtained by gradually sweeping the applied bias from –2 V to +2 V and simultaneously recording the corresponding current response of the heterojunction. The collected data were subsequently processed to construct the I–V curves, which form the basis for the analysis of the electrical properties of the Si/CdTe heterostructure. The C–V characteristics of the n-Si/p-CdTe heterostructure were measured at room temperature using a U2829C Precision LCR Meter, as illustrated in Figure 5. The sample was mounted in a custom-designed sample holder that ensured stable top and bottom contacts to the Si/CdTe junction. Although the sample holder is displayed in the open configuration in Figure 5, all measurements were carried out in the closed configuration to minimize the external noise and to ensure reliable contact stability.

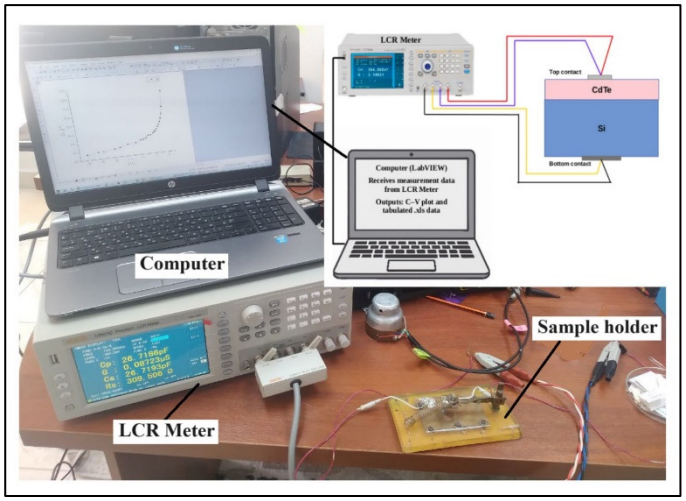

Fig. 5. Experimental setup for C–V measurements of the n-Si/p-CdTe heterostructure with U2829C Precision LCR meter, a computer for data acquisition and processing, and a sample holder.

During the measurements, the LCR meter applied a small AC test signal of 1 kHz superimposed on a DC bias sweep from –10 V to +10 V. The instrument simultaneously recorded the capacitance response of the heterojunction. The raw data were automatically transferred to a computer via LabVIEW interface and stored in tabulated Excel (.xls) files. These data were subsequently processed to obtain C–V plots used for further analysis.

The spectral photocurrent response of the n-Si/p-CdTe heterostructure was investigated using the optical setup illustrated in Figure 6. A mercury lamp served as the excitation source. The emitted light was first collimated by a lens and passed through a slit into Optical Box 1, where it was sequentially reflected by Mirror 1, dispersed by a prism, and redirected by Mirror 2 toward the entrance of the monochromator. By adjusting the monochromator angle, the wavelength of the incident radiation was systematically varied across the desired spectral range.

The monochromated beam was subsequently focused by a second lens onto the Si/CdTe sample, which was mounted in Optical Box 2 on a custom-designed sample holder. Two configurations of Optical Box 2 were utilized: the closed configuration to minimize stray light and external noise and the open configuration shown in the photographs for illustrative purposes. The device contacts were connected to an ammeter, enabling the direct measurement of the photocurrent generated under monochromatic illumination.

The internal arrangement of Optical Box 1 (comprising mirrors and a prism) is represented schematically in the lower part of Figure 6, while the actual photographs illustrate Optical Box 2 in both closed and open states. The photocurrent signals were simultaneously recorded by a computer through a LabVIEW interface, stored in tabulated form, and subsequently processed to construct the photocurrent–wavelength spectra.

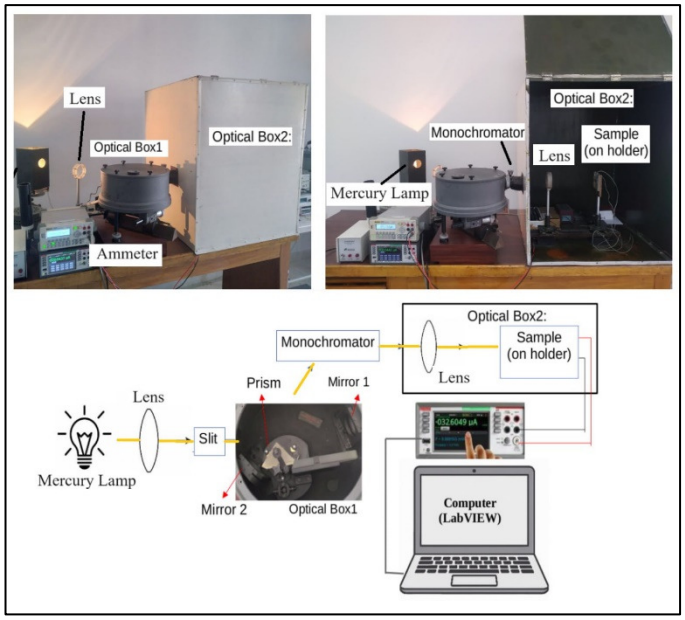

Fig. 6. Experimental setup for spectral photocurrent measurements of the n-Si/p-CdTe heterostructure.

III. RESULTS AND DISCUSSION

As illustrated in Figure 7, the proposed process began with the preparation and cleaning of n-type Si(111) wafers (thickness: 350–400 μm, resistivity: 5–10 Ω·cm) to remove the surface contaminants accumulated during prolonged storage. After cleaning, the wafers were mounted on the substrate holder, and the vacuum chamber was evacuated to about 1.3×10^{-4} Pa in a quasi-closed system. The CdTe source was then heated to 800–850 °C, while the substrate temperature was maintained at 450–480 °C. This controlled heating—facilitated by an annealing—ensured uniform film growth during rapid thermal annealing. The microstructural examinations confirmed that both the epitaxial layer thickness and the growth kinetics depended strongly on the annealing time and substrate temperature, highlighting the importance of precise thermal management at each stage of the process. The surface morphology of the CdTe epitaxial layers was examined using both Scanning Electron Microscopy (SEM) and an MII-4 optical microscope. The SEM and Energy-Dispersive Spectroscopy (EDS) analyses were performed utilizing a JEOL JXA-8900 microanalytical system equipped with an Oxford Instruments LINK ISIS energy-dispersive spectrometer. The imaging conditions were as follows: accelerating voltage V = 20 kV, beam current I = 10 nA. The reference standards included native cadmium (Cd), tellurium (Te), and silicon (Si), while synthetic FeS was used for sulfur. The measurement uncertainty was estimated at ±2.0%. These parameters ensure the accurate quantification of the elemental distributions. The updated SEM images include embedded metadata, such as magnification, Working Distance (WD), and scale bars, in accordance with the standard reporting requirements. Figures 8(a) and (b) illustrate the microstructural characteristics of the CdTe layer at different magnifications. Figure 8(a), which is an SEM image, reveals a well-defined textured surface consisting of densely packed, faceted crystallites.

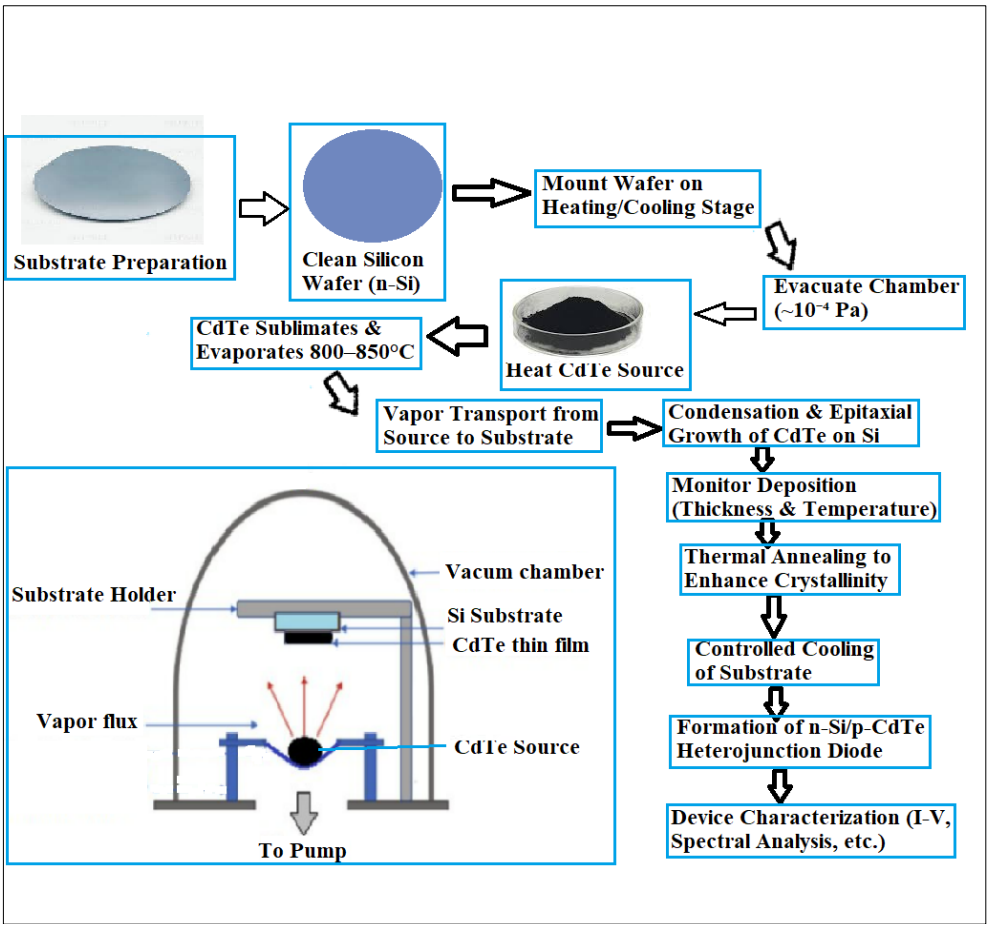

Fig. 7. Flowchart of CdTe/Si heterojunction growth using VTE.

This morphology suggests a preferentially oriented grain growth, which is likely influenced by the high annealing temperature and the epitaxial relationship with the substrate. The observed faceted grains indicate that CdTe has undergone significant grain coarsening, which can be beneficial for improving the charge carrier transport properties. Figure 8(b) (Optical microscope image) presents a broader view of the CdTe surface, showing a rougher and less uniform texture. This appearance may result from variations in the grain size, residual stress from the CdTe-substrate interaction, or minor imperfections at the grain boundaries.

The contrast in the images highlights the differences in local crystallinity and surface roughness, which may influence the material's electrical and optical performance. The surface morphology plays a crucial role in the optoelectronic behavior of CdTe-based devices. A more ordered, faceted structure, as portrayed in Figure 8(a), can enhance the carrier transport, while excessive roughness, as evidenced in Figure 8 (b), may introduce scattering effects and increase the recombination rates. The annealing conditions applied in this study contributed to the observed grain structure, suggesting that further optimization of process parameters, such as annealing duration and cooling rate, could lead to more uniform epitaxial layers with improved functional properties. The X-ray spectroscopy results presented in Figure 9 illustrate the elemental distribution within the pCdTe/n-Si heterostructure. Initially, the Si concentration on the n-Si substrate surface is significantly high. However, as the CdTe epitaxial layer grows, the Si concentration gradually decreases, while the intensities of Cd and Te increase, indicating the formation of a CdTe-rich layer. As the deposition progresses, the silicon signal reaches a minimum, confirming that the surface is predominantly covered with CdTe.

The strong dual-electron emission peaks for Cd and Te in the spectrum further validate that the topmost layer primarily consists of CdTe, ensuring a well-defined epitaxial structure. To achieve epitaxial heterostructures with minimal defects, the lattice mismatch should ideally be within 7% [30].

Despite the significant lattice mismatch of approximately 19.3% between CdTe and Si, the X-ray spectroscopy results in Figure 9 indicate successful epitaxial growth. The strong Cd and Te emission peaks, along with the gradual reduction of the Si signal, confirm that the CdTe layer has been effectively deposited. This suggests that the optimized deposition conditions have played a crucial role in achieving a high-quality heterostructure. To further improve the structural integrity and minimize the defect density, techniques such as buffer layers, strain engineering, or graded transition layers, may be implemented. These approaches could help mitigate the effects of lattice mismatch, enhancing the electronic and optical performance of the heterostructure.

(a)

(b)

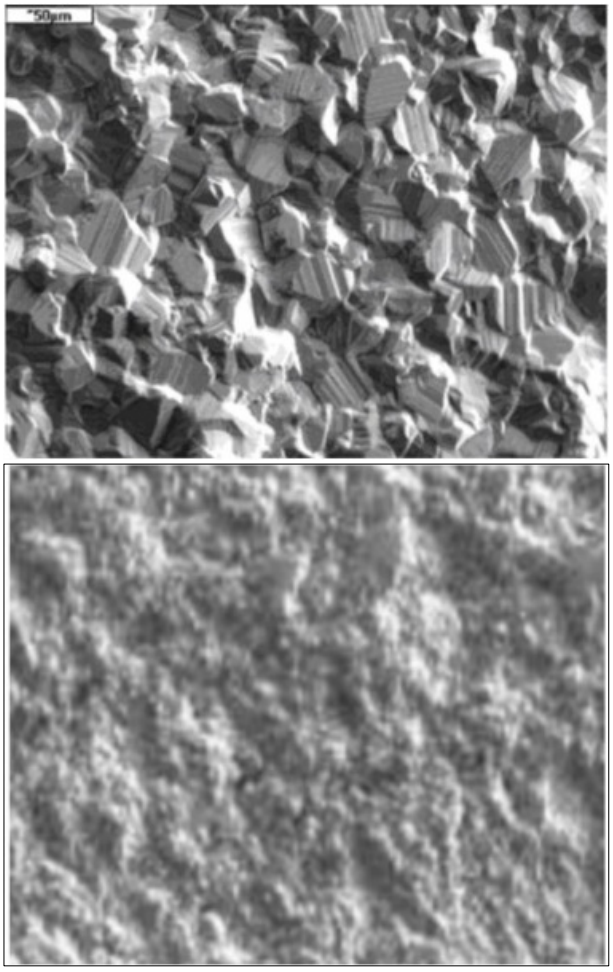

Fig. 8. Surface morphology of the CdTe thin film deposited on a silicon substrate: (a) SEM image showing the polycrystalline texture of the CdTe layer, captured with: accelerating voltage V = 20 kV, beam current I = 10 nAWD ≈ 10 mm, scale bar = 1 µm, (b) optical micrograph illustrating the broader surface topology and non-uniform roughness of the CdTe film.

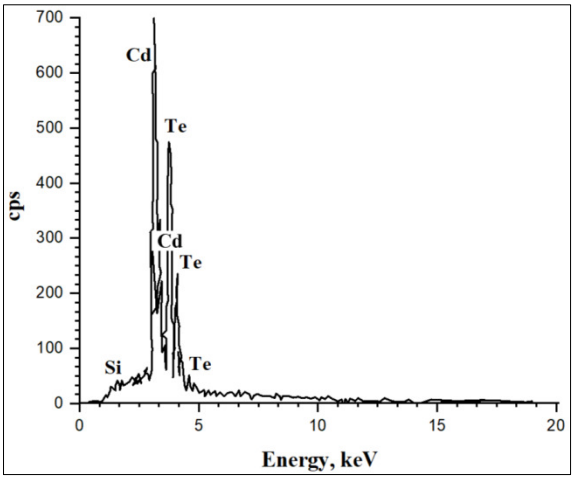

Fig. 9. EDS spectrum of the CdTe/n-Si heterostructure.

(a)

(b)

(c)

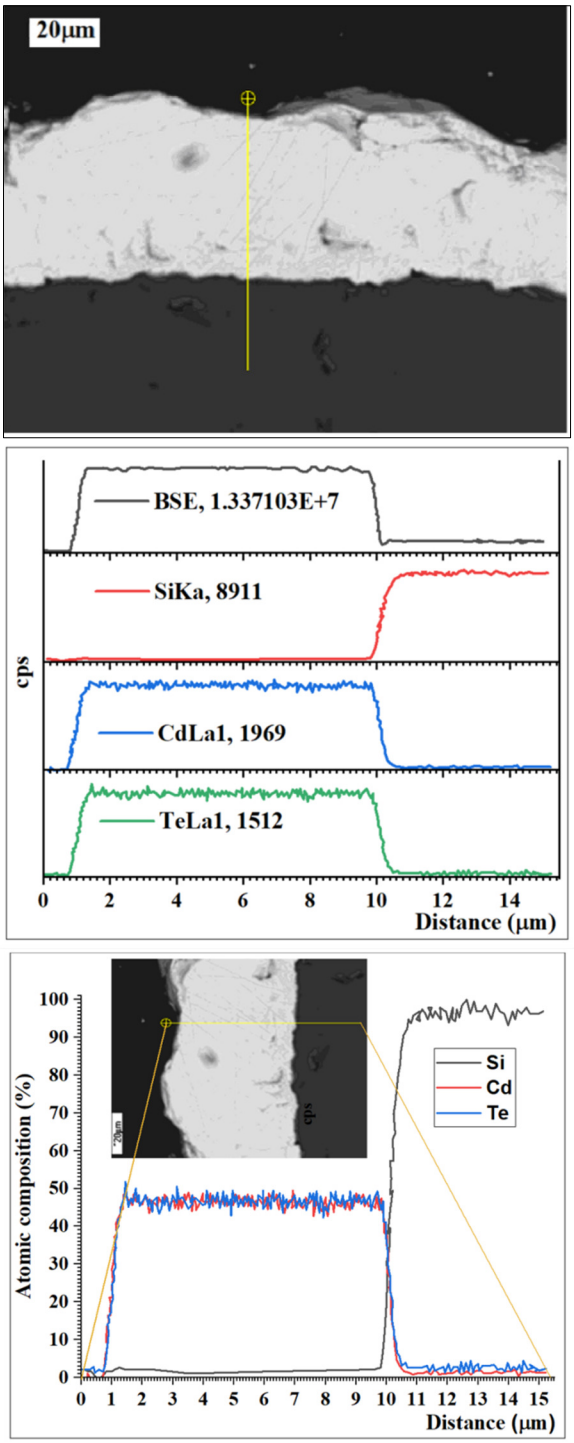

Fig. 10. Elemental distribution and interfacial quality of the CdTe/Si heterostructure based on EDS analysis: (a) Backscattered Electron (BSE) SEM image displaying the cross-sectional view of the CdTe/Si interface, (b) elemental concentration profiles of Si, Cd, and Te acquired along the scan path, showing a sharp transition across the heterointerface, (c) atomic percentage variations of Si, Cd, and Te as a function of depth.

The results shown in Figure 10 provide an understanding of the elemental distribution and interface quality of the CdTe/Si heterostructure based on the EDS analysis. In Figure 10(a), the BSE cross-sectional image reveals a uniform CdTe layer

deposited on the Si substrate, with the yellow line indicating the EDS scan path. As depicted in Figure 10(b), the silicon concentration drops sharply beyond the interface, while the cadmium and tellurium signals increase and stabilize, suggesting the formation of a stoichiometric CdTe layer. Figure 10(c) further supports this observation, showing that Cd and Te atomic percentages level off at approximately 49–50 at.%, while Si content falls to near zero within a narrow ~1 μm transition zone. The stable profiles of Cd and Te indicate a minimal interdiffusion and a well-defined interface. This sharp compositional boundary reflects an effective control over the deposition process and is crucial for enhancing the electronic quality of the heterostructure. Overall, the results confirm the successful growth of a high-quality CdTe film with a clean, abrupt junction to the underlying Si, which is essential for minimizing defect-related recombination and optimizing device performance in applications such as photovoltaics or radiation detectors.

Table I and Figure 11 illustrate the elemental distribution within the Si-CdTe heterojunction, highlighting the compositional gradient across the interface. The CdTe thin film formed on the silicon substrate exhibits a clear compositional gradient at the CdTe/Si interface, characterized by a transition region approximately 2–3 μm thick, as confirmed by the gradual decrease in Cd and Te intensities and the corresponding increase in Si signal observed in the EDS line scan, as displayed in Figure 10. Initially, the interfacial region (~1–1.5 μm) is Si-rich; however, as deposition continues, the silicon concentration decreases and the CdTe composition progressively stabilizes. This compositional evolution results in the formation of a fully developed epitaxial CdTe layer with an overall thickness of approximately 10 μm, as further illustrated schematically in Figure 11 and quantitatively supported by the elemental distributions detailed in Table I. Such controlled and graded deposition significantly reduces the interfacial defects, thereby enhancing the quality of the heterojunction.

Ensuring minimal defects and high-quality heterostructures requires careful control of the lattice mismatch and interfacial roughness during deposition. Following the elemental analysis presented in Table I and the structural schematic in Figure 11, the crystallographic quality of the CdTe layer was further assessed using XRD analysis performed with an Empyrean PANalytical diffractometer. The diffraction pattern, as shown in Figure 12, confirms the presence of mixed crystallographic phases in the CdTe thin film, including cubic, orthorhombic, and hexagonal structures. For the as-deposited CdTe film, the characteristic peaks of the cubic phase were observed at 2θ angles of 23.56°, 28.2°, 39.16°, 46.32°, 47.08°, 56.4°, and 63.00°, corresponding to the (111), (200), (220), (311), (222), (400), and (331) lattice planes, respectively.

For the orthorhombic phase, peaks at approximately 32.76° and 42.72° were attributed to the (100) and (101) planes, while the hexagonal phase exhibited peaks at 22.28°, 25.12°, 54.28°, and 66.8°, associated with the (100), (101), (104), and (107) reflections. These results are consistent with the Joint Committee on Powder Diffraction and Standards (JCPDS) reference file numbers 752086, 410941, and 800090 for the cubic, orthorhombic, and hexagonal structures, respectively.

The diffraction patterns revealed sharp and intense peaks at positions corresponding to the (111), (200), (220), (311), (222), (400), and (331) planes of the dominant crystalline phase, confirming the polycrystalline nature of the film. No significant reflections from the underlying Si (111) substrate were observed, indicating that the CdTe layer does not replicate the orientation of the substrate. The sharpness of the diffraction peaks indicates the absence of an amorphous phase.

The significant broadening of the diffraction peaks indirectly confirms the presence of considerable azimuthal surface stresses. Additionally, the diffraction peaks are shifted relative to the standard reference peaks of CdTe. This shift indicates an increase in the lattice parameter of the grown solid solution (a* CdTe = 0.6520 ± 0.00004 nm), whereas the standard lattice constant of CdTe is aCdTe = 0.6481 nm. The reason for this increase in the lattice parameter of the grown phase may be the presence of compressive stresses on the surface (within the plane of the surface).

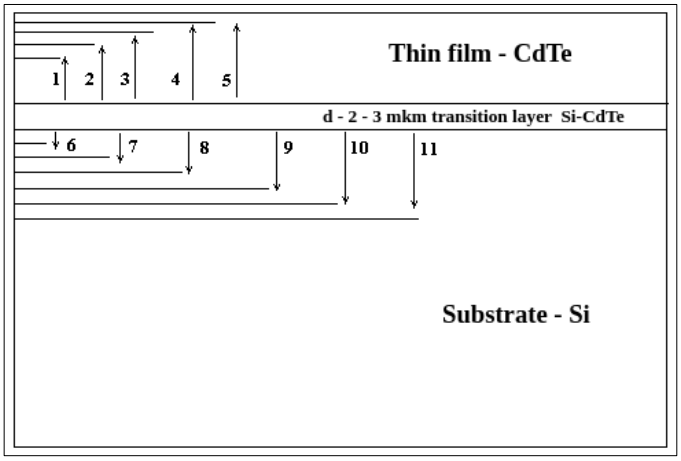

Fig. 11. Schematic cross-section of the Si–CdTe heterojunction.

TABLE I. ELEMENTAL DISTRIBUTION BY ATOMIC PERCENTAGES IN Si-CdTe HETEROJUNCTION

Distances from the Si-CdTe interface to the surface of the CdTe thin film	Atom percentages (%)	Distances from the Si-CdTe interface to the Si substrate	Atom percentages (%)
1-1.5 μm	Si-4.32, Cd-47.69, Te-47.992	0.5 μm	Si-95.07, Cd-2.43, Te-2.49
2.5-3 μm	Si-0.55, Cd-48.95, Te-49.50	0.7–1 μm	Si-98.14, Cd-0.95, Te-0.91
5 μm	Si-0.71, Cd-49.42, Te-49.87	2–2.5 μm	Si-99.67, Cd-0.16, Te-0.17
10 μm	Si-0.52, Cd-49.34, Te-50.30	3 μm	Si-99.96, Cd-0.06, Te-0.02
-	-	4 μm	Si-100.18, Cd-(-0.01), Te-(-0.01)
-	-	5 μm	Si-100.04, Cd-(-0.02), Te-(-0.02)

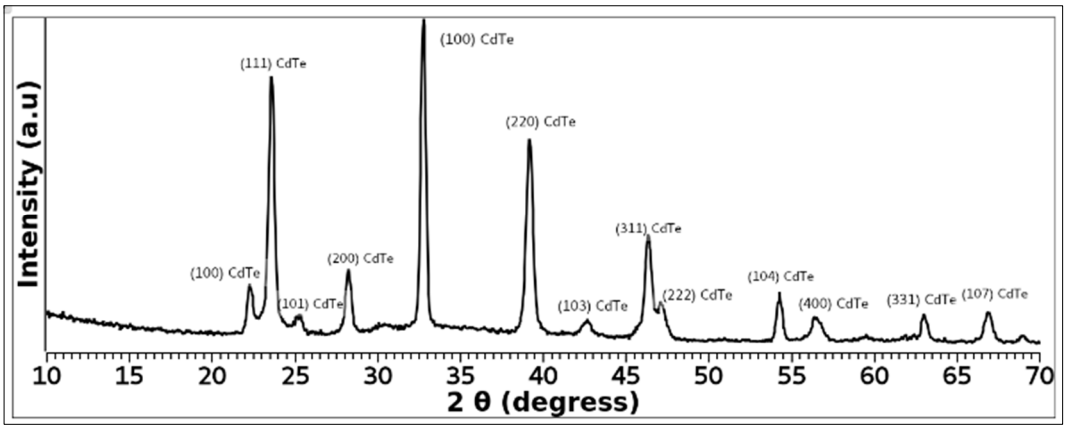

Fig. 12. XRD pattern of the CdTe thin film deposited on a silicon substrate via VTE, confirming the polycrystalline structure and mixed-phase composition.

Figure 13 shows the measured I–V characteristics of the n-Si/p-CdTe heterostructure, with error bars representing a measurement uncertainty of approximately 5%. Electrical contacts were established under vacuum conditions to minimize contact resistance and environmental influences. The I–V curve clearly exhibits rectifying diode behavior, characterized by negligible current flow under reverse bias (negative voltages) and a pronounced exponential increase in current above approximately 0.5 V forward bias. Such behavior confirms efficient carrier injection across the heterointerface via thermionic emission mechanisms. The included error bars demonstrate measurement accuracy, providing confidence in the reliability and repeatability of the obtained results.

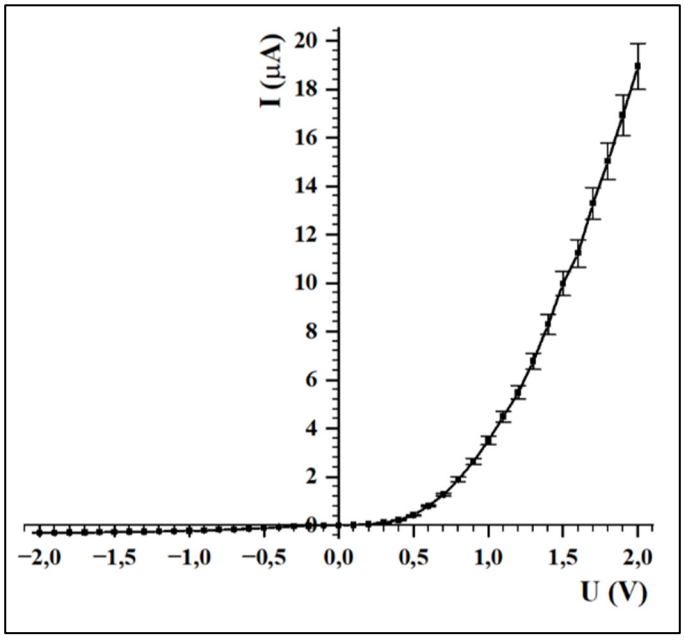

Fig. 13. I–V Characteristics of the nSi-pCdTe heterostructure.

Figure 14 illustrates the C–V response of the n-Si/p-CdTe heterostructure recorded at room temperature and a measurement frequency of 1 kHz, with error bars reflecting a ±3% uncertainty related to instrumental calibration and sample-contact geometry. The data clearly exhibit a pronounced capacitance peak near zero bias, characteristic of a depletion region typically observed in diode structures. This finding aligns closely with the rectifying (diode-like) behavior confirmed by the previously presented I–V measurements, as illustrated in Figure 13. However, caution is required when interpreting single-frequency C–V measurements. Specifically, at low frequencies, such as 1 kHz, capacitance values can be influenced by interface states and parasitic contributions, making it challenging to accurately extract doping concentrations or built-in potential (Vbi) through standard $1/C^2$ analysis. For more precise characterization—including the reliable determination of doping profiles and Vbi — measurements at multiple frequencies or at higher frequencies (typically in the MHz range) are proposed to isolate true depletion capacitance from interface-state effects. Nonetheless, the 1 kHz C–V results confirm the formation of a depletion region at the CdTe/Si interface, establishing the functionality of the n-Si/p-CdTe heterojunction. These findings validate the diode-like nature of the fabricated heterostructure, emphasizing its potential suitability for optoelectronic device applications. Further optimization of interface quality may yield additional improvements in device performance.

Figure 15 shows the spectral photocurrent response of the n-Si/p-CdTe heterostructure recorded across the 400–1300 nm wavelength range, exhibiting two prominent peaks around 850 nm and 1050 nm. The first peak at approximately 850 nm closely matches the CdTe bandgap energy (~1.45 eV), signifying efficient absorption, photogeneration, and collection of carriers within the CdTe layer. The second peak around 1050 nm corresponds well with the silicon bandgap energy (~1.12 eV), indicating that photons at longer wavelengths successfully pass through the CdTe layer and generate electron–hole pairs within the underlying silicon substrate. The observed dip between the two peaks (850–1050 nm) likely arises from increased recombination or carrier trapping at the CdTe/Si interface, where interfacial defects can reduce the carrier lifetime and impede efficient transport across the heterointerface. At wavelengths beyond approximately 1050 nm, the photocurrent sharply declines, consistent with silicon's absorption edge and confirming a minimal photogeneration beyond this limit.

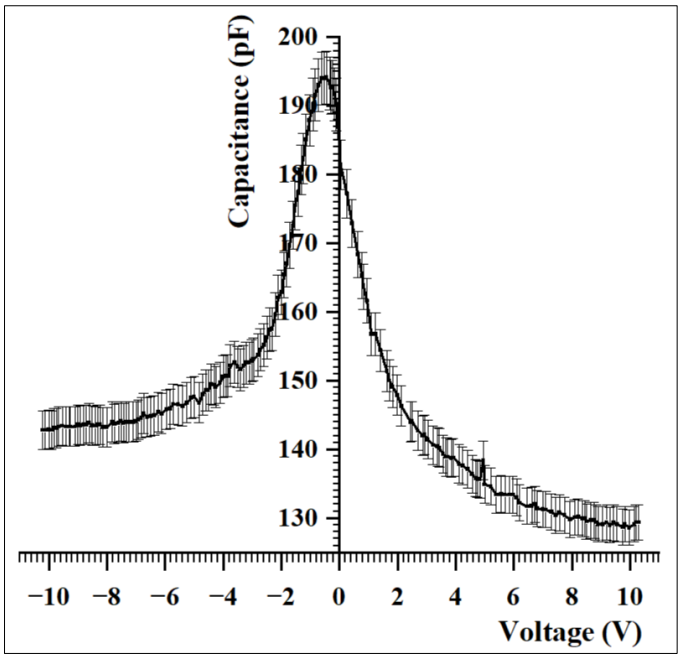

Fig. 14. Capacitance–voltage (C–V) characteristics of the n-Si/p-CdTe heterostructure.

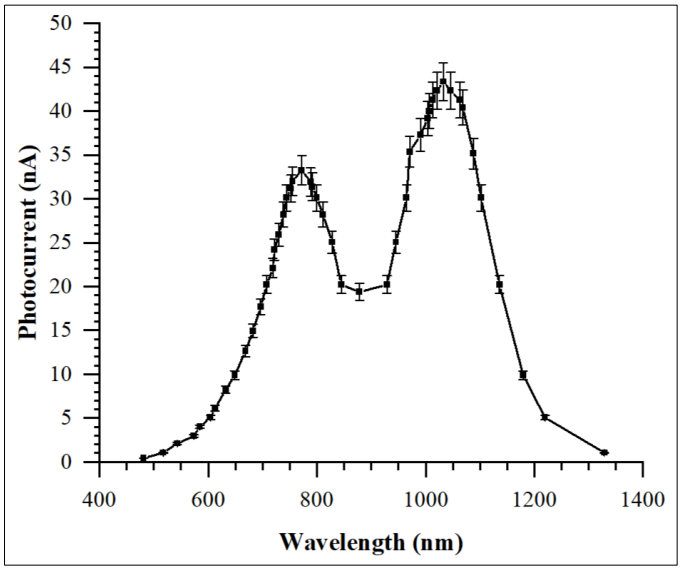

Fig. 15. Spectral photocurrent response of the n-Si/p-CdTe heterostructure measured in the wavelength range of 400–1300 nm.

Overall, this dual-peak spectral behavior highlights the broad spectral sensitivity of the n-Si/p-CdTe heterostructure, spanning the visible and near-infrared ranges. These results emphasize the importance of optimizing the interface and growth conditions of the CdTe layer, which could be achieved through improved surface passivation, strategic doping profiles, or advanced interface engineering methods. Such enhancements are crucial for improving the carrier collection efficiency and reducing recombination losses, ultimately benefiting applications such as near-infrared photodetection and tandem solar cells.

IV. CONCLUSION

This study successfully fabricates Silicon–Cadmium–Telluride (n-Si/p-CdTe) heterostructures via Vacuum Thermal Evaporation (VTE), demonstrating a low-cost, straightforward, and reproducible method, which is highly suitable for producing high-quality semiconductor heterojunctions. The Energy-Dispersive Spectroscopy (EDS) X-ray analyses confirmed the formation of a near-stoichiometric CdTe epitaxial layer with a clearly defined compositional gradient. The detailed EDS line-scan measurements revealed that the actual CdTe film thickness is approximately 10 µm, highlighting the importance of direct compositional analysis for accurate structural characterization. The microstructural characterization demonstrated the presence of a faceted surface morphology with moderate interface roughness. Although such morphological features could enhance the carrier mobility, they simultaneously indicate opportunities for further improvement through targeted interface passivation and structural optimization to reduce recombination losses.

The X-ray diffraction (XRD) analysis further confirmed the formation of a polycrystalline CdTe layer with predominant cubic phase reflections, primarily along the (111), (220), (311), and (400) crystallographic planes, in agreement with the Joint Committee on Powder Diffraction and Standards (JCPDS) card no. 75-2086. These results are consistent with those of studies that observed similar phase compositions and structural transitions in electrodeposited CdTe films, thereby further validating the presence of mixed crystalline phases under specific growth conditions. The absence of amorphous background and the presence of sharp, well-defined peaks indicate the high crystallinity and good structural quality of the deposited layer. Slight shifts in the peak positions compared to standard reference values revealed an expanded lattice constant of $a = 0.6520 \pm 0.00004$ nm, which is attributed to compressive in-plane surface stresses—common in heteroepitaxial growth on lattice-mismatched substrates such as silicon. These findings confirm the structural integrity and epitaxial nature of the CdTe film, highlighting the effectiveness of the VTE method.

The electrical characterization through the current–voltage (I–V) and capacitance–voltage (C–V) measurements clearly exhibited a diode-like rectifying behavior. Additionally, the spectral analysis of the fabricated heterostructure showed dual-band photocurrent sensitivity with distinct peaks at around 850 nm and 1050 nm, corresponding closely to the bandgap energies of CdTe (~1.45 eV) and Si (~1.12 eV), respectively. The observation of this dual-peak response underscores the structure's capability for broadband optoelectronic applications, especially in near-infrared photodetection and tandem photovoltaic configurations.

The experimental results obtained in this work closely align with prior experimental research and the theoretical modeling of CdTe/Si heterojunctions [31, 32], where initial empirical parameters derived from VTE-grown films were employed to guide the numerical simulations. This synergy between the experimental measurements and theoretical predictions highlights the potential of leveraging initial experimental data to refine the computational models, ultimately reducing the need for extensive experimentation.

When compared to previous research employing sophisticated deposition methods, such as Molecular Beam Epitaxy (MBE) or Close-Spaced Sublimation (CSS)—often necessitating buffer layers, specialized substrate conditioning, or extensive interfacial engineering [33–37]—the results of the present study highlight significant advantages. Specifically, authors in [37] required the use of ZnTe and Ge buffer layers during MBE to achieve abrupt CdTe/Si interfaces, whereas the current study demonstrates similarly abrupt interfaces achieved directly via simpler and buffer-free VTE processing. Such simplicity not only reduces production complexity and cost but also maintains a competitive optoelectronic performance.

The novelty of this work lies in its accurate determination of the epitaxial film thickness through direct compositional profiling, the confirmation of dual-band spectral sensitivity, and the demonstration of superior interface control achievable by VTE without additional complex processing steps. Furthermore, the successful identification of the crystalline phase composition and lattice parameter variation through the XRD analysis adds structural insights into the film quality. These findings position VTE as a highly promising and scalable method for fabricating efficient dual-band photodetectors and advanced tandem photovoltaic devices. Future research will focus on further optimizing the interface quality, thermal processing conditions, and film uniformity to enhance device efficiency and operational stability.

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