Design and Development of Three-Phase Two-Level Unidirectional Rectifiers for EV Chargers Using SVPWM and a Voltage-Oriented Controller

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ABSTRACT

The rapid increase in Electric Vehicles (EVs) and the subsequent rise in demand for fast charging infrastructure has emphasized the need for high-performance, efficient rectifiers that adhere to the Power Quality (PQ) standards. This study's primary objective is to design and develop Three-Phase, Two-Level, Unidirectional Rectifiers (3P-2L-URs) for 800V EV chargers. These rectifiers are available in Wye, Delta, and Bridge topologies. To enhance the input PQ and assess the output performance, a control strategy that integrates Voltage-Oriented Control (VOC)-based decoupled controllers with Space Vector Pulse Width Modulation (SVPWM) is proposed. Analytical expressions were used for three-phase modulation signals for each topology and the switching control was designed to minimize the switching losses using a five-segment switching sequence technique. MATLAB/Simulink was deployed to verify the performance of each topology. All topologies met the IEEE 519 and IEC 61000-3 standards, attaining sinusoidal input currents with Total Harmonic Distortion (THD) below 5% and Power Factors (PF) above 99.90%. The Three-Phase, Two-Level, Wye-type, Unidirectional Rectifier (3P-2L-Wye-UR) exhibited the greatest output performance with the lowest voltage and current ripples, making it the most promising solution for high-efficiency EV fast charging applications.

Keywords-three-phase rectifier; SVPWM; voltage-oriented control; electric vehicle charger; power quality

I. INTRODUCTION

The global demand for EVs - 13.7 million units in 2023 [1] - has raised the demand for efficient, high-capacity EV chargers. The number of slow and fast charging stations worldwide has grown over 1.77 million in 2021—an 865.80% increase since 2015. Fast charging, especially using Direct Current (DC) systems, is important as it significantly reduces the charging time and improves the energy efficiency [2, 3], with the operating voltage increasing from 600 V to 800 V [4]. Furthermore, the reduced current, due to high operating voltage allows for smaller conductor dimensions, thereby reducing the weight of the EV charger, increasing the charging system's overall efficiency [5, 6]. EV chargers depend on AC-DC power converters (rectifiers), can affect the PQ in electrical distribution systems, and can lead to current harmonics and reduced PF [7]. This study categorizes the rectifiers into three main types: passive, hybrid, and active. The three-phase active rectifiers deliver improved PQ performance through Power Factor Correction (PFC) and low THD [8] and they can function in unidirectional and bidirectional power flow modes. The unidirectional three-phase topology is used for EV chargers due to its simpler architecture, reduced battery degradation, and ease of installation [9, 10]. The unidirectional three-phase rectifiers can be categorized as two-level or three-level topologies. Three-Phase, Three-Level Unidirectional Rectifiers (3P-3L-URs) benefit from the lower voltage stress on the power switches, which decreases the risk of failure. Many EV charging stations have examined and used the Vienna rectifier [11, 12], which offers significant advantages, including an input current THD below 5%, a high PF, and an efficiency above 95%. However, a significant constraint lies in the neutral-point voltage balancing method, which requires two split capacitors connected across the DC link. Maintaining real-time voltage balance among these capacitors is essential for steady and reliable operation. Integrating supplementary voltage balancing control loops into the system increases the control complexity and may affect the overall system robustness and long-term reliability. The semiconductor technology has enabled the power switches to provide higher voltage and current ratings, increased reliability, and reduced costs [13]. As a result, simpler and more compact 3P-2L-URs require only one DC-link capacitor, which effectively resolves the voltage imbalances and simplifies the control system complexity. The main types are Wye-, Delta-, and Bridge-type rectifiers are presented in Figure 1. However, despite the existence of numerous 3P-2L-UR topologies, a comprehensive assessment of their suitability for fast EV charging applications is still needed [8]. Most research on AC–DC power converters used in EV chargers emphasizes the grid-side PQ. Nevertheless, insufficient focus has been given to the attributes of the DC output, which directly affect the battery lifespan and the efficacy of the connected devices, especially with regard to the thermal stress caused by the voltage and current ripples. To address these gaps, this study proposes designing and developing switching control algorithms for 3P-2L-URs to facilitate an 800 V EV fast-charging system that complies with the IEEE 519 and IEC 61000-3 standards. The study also includes a thorough analysis of the voltage and current ripple characteristics associated with each 3P-2L-UR topology. The proposed methodology combines SVPWM with a decoupled controller that uses a VOC technique to achieve accurate regulation and improved performance.

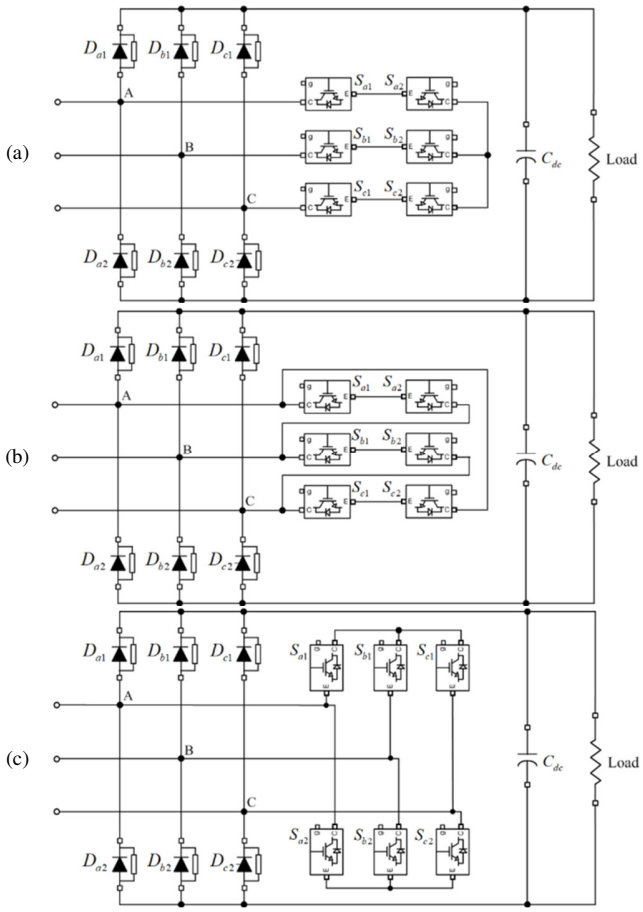

Fig. 1. Topologies of 3P-2L-URs: (a) Wye-type, (b) Delta-type, and (c) Bridge-type.

II. WORKING ANALYSIS OF 3P-2L-URS BASED ON SPACE VECTOR MODULATION

The switching states of the vectors in the traditional Space Vector Modulation (SVM) diagram are initially designed to produce balanced three-phase AC voltages. When applied to 3P-2L-URs, which emphasize the transfer of maximum instantaneous input line current to the output, the switching states must be appropriately modified based on the current direction routes specific to each rectifier topology. Each 60° Voltage Sector (VS) is subdivided into two 30° intervals to accommodate the alternating dominant phase currents, as shown in Figure 2. For instance, the highest input currents transition between phase C (negative) and phase A (positive) in VS1, thereby necessitating distinct switching states for each interval. The objective of this study is to obtain tailored switching states for three rectifier topologies.

A. Wye-Type Rectifier

The operational analysis of the 3P-2L-Wye-UR during the initial 30° interval of VS1 was performed, employing the non-

null vectors $\vec{V}_1$ and $\vec{V}_2$. During this period, the switching states [1 0 0] and [1 1 0] for vectors $\vec{V}_1$ and $\vec{V}_2$, respectively, correspond to those in the traditional SVM diagram. In the event that the reference voltage vector (V_{ref}) falls within the second 30° interval, it is necessary to invert the switching states to [0 1 1] for V_1 and [0 0 1] for V_2. The null vectors $\vec{V}_0$ and $\vec{V}_7$ are used to maintain a zero voltage across the load. This configuration enables the internal current flow within the rectifier, thereby preventing the power transfer to the load. Among the available options, vector $\vec{V}_7$ [1 1 1] has been determined to be the optimal choice for achieving the stated objective.

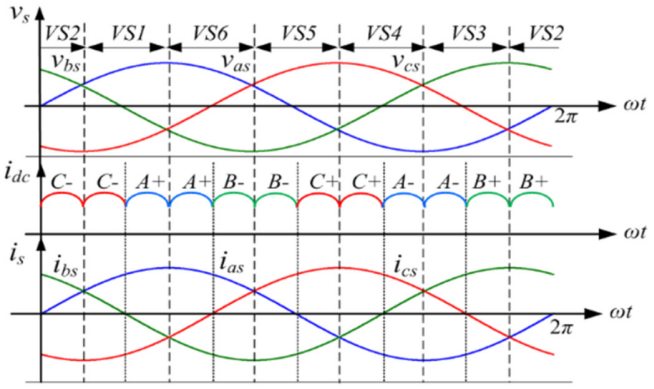

Fig. 2. Voltage and current waveforms segmented by VS intervals.

B. Delta-Type Rectifier

The present study uses vectors $\vec{V}_1$ and $\vec{V}_2$ to analyze the operational behavior of the 3P-2L-Delta-UR during the initial 30° of VS1. However, given the distinct conduction characteristics inherent in this topology, it is important that each non-null vector containing a logic '1' be converted to '0'. Consequently, the switching states $\vec{V}_1$ and $\vec{V}_2$ are altered from [1 0 0] and [1 1 0] to [0 0 0] and [1 0 0], respectively. In the 30–60° range, further adjustments are necessary: the switching states $\vec{V}_1$ and $\vec{V}_2$ should be altered from [0 1 1] and [0 0 1] to [0 1 0] and [0 0 0], respectively. The null vector $\vec{V}_7$ remains in use, with its switching states being defined by the angular location of $\vec{V}_{\text{ref}}$, transitioning from [1 1 1] to [1 0 1] during the initial 30°, and to [0 1 1] during the subsequent 30°.

C. Bridge-Type Rectifier

The switching states of the 3P-2L-Bridge-UR diverge significantly from the traditional SVM diagram. In the initial 30° of VS1, the switching states $\vec{V}_1$ and $\vec{V}_2$ must be altered from [1 0 0] and [1 1 0] to [0 0 0] and [0 1 0], respectively. In the following 30°, the switching states continue to diverge in accordance with the established pattern documented in the 3P-2L-Delta-UR. It is important to note that, despite the fact that vector $\vec{V}_7$ is the assigned null vector, its switching state must undergo an alteration from [1 1 1] to [0 1 1] during the initial 30°, and then to [1 1 0] for the subsequent 30°. The analytical approach employed for the three topological types of the 3P-2L-URs can be systematically extended to other VSs. Table I presents an extensive list of the switching states for the Nearest Three Vectors (NTVs) corresponding to all VSs.

TABLE I. APPROPRIATE SWITCHING STATES OF THE 3P-2L-URS BASED ON THE SVM DIAGRAM

VSs	Angle of $\vec{V}_{\text{ref}}$	SVM vectors	Appropriate switching states		
			Wye-type	Delta-type	Bridge-type
1	0°-30°	$\vec{V}_1$[1 0 0]	[1 0 0]	[0 0 0]	[0 0 0]
		$\vec{V}_2$[1 1 0]	[1 1 0]	[1 0 0]	[0 1 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 0 1]	[0 1 1]
	30°-60°	$\vec{V}_1$[1 0 0]	[0 1 1]	[0 1 0]	[0 1 0]
		$\vec{V}_2$ [1 1 0]	[0 0 1]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[0 1 1]	[1 1 0]
2	60°-90°	$\vec{V}_2$[1 1 0]	[0 0 1]	[0 0 0]	[0 0 0]
		$\vec{V}_3$[0 1 0]	[1 0 1]	[0 0 1]	[1 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[0 1 1]	[1 1 0]
	90°-120°	$\vec{V}_2$[1 1 0]	[1 1 0]	[1 0 0]	[1 0 0]
		$\vec{V}_3$[0 1 0]	[0 1 0]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 1 0]	[1 0 1]
3	120°-150°	$\vec{V}_3$[0 1 0]	[0 1 0]	[0 0 0]	[0 0 0]
		$\vec{V}_4$[0 1 1]	[0 1 1]	[0 1 0]	[0 0 1]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 1 0]	[1 0 1]
	150°-180°	$\vec{V}_3$[0 1 0]	[1 0 1]	[0 0 1]	[0 0 1]
		$\vec{V}_4$[0 1 1]	[1 0 0]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 0 1]	[0 1 1]
4	180°-210°	$\vec{V}_4$[0 1 1]	[1 0 0]	[0 0 0]	[0 0 0]
		$\vec{V}_5$[0 0 1]	[1 1 0]	[1 0 0]	[0 1 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 0 1]	[0 1 1]
	210°-240°	$\vec{V}_4$[0 1 1]	[0 1 1]	[0 1 0]	[0 1 0]
		$\vec{V}_5$[0 0 1]	[0 0 1]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[0 1 1]	[1 1 0]
5	240°-270°	$\vec{V}_5$[0 0 1]	[0 0 1]	[0 0 0]	[0 0 0]
		$\vec{V}_6$[1 0 1]	[1 0 1]	[0 0 1]	[1 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[0 1 1]	[1 1 0]
	270°-300°	$\vec{V}_5$[0 0 1]	[1 1 0]	[1 0 0]	[1 0 0]
		$\vec{V}_6$[1 0 1]	[0 1 0]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 1 0]	[1 0 1]
6	300°-330°	$\vec{V}_6$[1 0 1]	[0 1 0]	[0 0 0]	[0 0 0]
		$\vec{V}_1$[1 0 0]	[0 1 1]	[0 1 0]	[0 0 1]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 1 0]	[1 0 1]
	330°-360°	$\vec{V}_6$[1 0 1]	[1 0 1]	[0 0 1]	[0 0 1]
		$\vec{V}_1$[1 0 0]	[1 0 0]	[0 0 0]	[0 0 0]
		$\vec{V}_7$[1 1 1]	[1 1 1]	[1 0 1]	[0 1 1]

III. COMMAND SIGNAL GENERATION USING THE SVPWM TECHNIQUE

The present study uses a control method to minimize the number of commutations in the Controllable Power Switches (CPSs) of the 3P-2L-URs. This is achieved by reducing the switching losses and improving the overall rectifier efficiency.

A. Five-segment Switching Sequence Technique

A five-segment switching sequence technique is used to minimize the switch commutations per phase leg. This method organizes the switching states of the NTVs within each VS, as specified in Table I, with the objective of enhancing the commutation pattern. Specifically, when the $\vec{V}_{\text{ref}}$ is situated within the initial 30° of VS1, the designated switching

sequence for the 3P-2L-Wye-UR is: $\vec{V}_7 \rightarrow \vec{V}_2 \rightarrow \vec{V}_1 \rightarrow \vec{V}_2 \rightarrow \vec{V}_7$, as shown in Figure 3 (a). The corresponding sequences for the 3P-2L-Delta-UR and 3P-2L-Bridge-UR are presented in Figures 3 (b) and 3 (c), respectively.

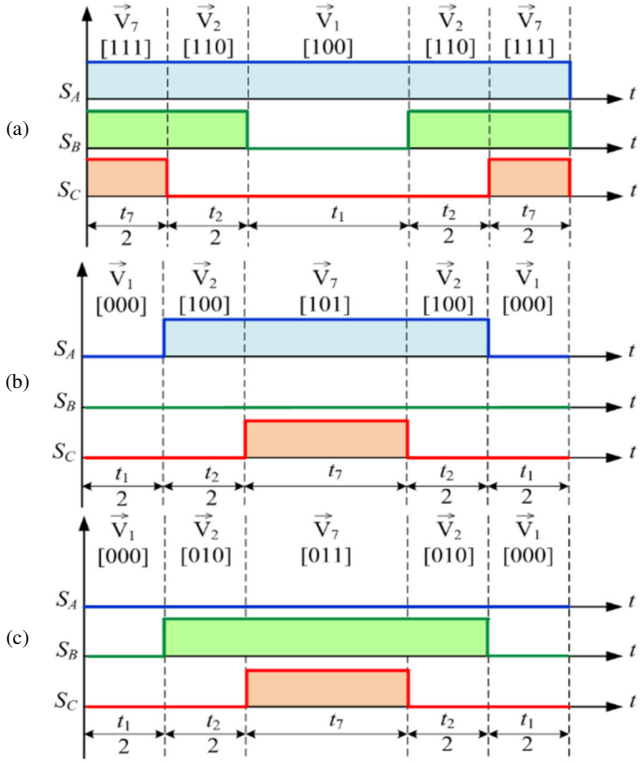

Fig. 3. The switch driving signal sequence diagram within the first 30° of VS1 for different rectifier topologies: (a) the 3P-2L-Wye-UR, (b) the 3P-2L-Delta-UR, and (c) the 3P-2L-Bridge-UR.

B. Expressions for Three-Phase Modulation Signals

The mean value of $\vec{V}_{\text{ref}}$ is determined by means of the SVM approach, which is predicated on the volt–second balance and the switching period (T_s). For instance, when the $\vec{V}_{\text{ref}}$ is positioned within the VS1, its volt-second balance and T_s equations are:

$$\vec{V}_{ref} T_S = \vec{V}_1 t_1 + \vec{V}_2 t_2 + \vec{V}_0 T_0 \quad (1)$$

$$T_S = t_1 + t_2 + T_0 \quad (2)$$

where T_0 is the dwell time of the null vector, including the total duration of t_0 and t_7, and t_1 and t_2 are the dwell periods for vectors $\vec{V}_1$ and $\vec{V}_2$, respectively. The dwell periods of non-null vectors for each VS are:

$$\begin{bmatrix} t_{VS} \\ t_{VS+1} \end{bmatrix} = m_a T_S \begin{bmatrix} \sin\frac{\pi VS}{3} & \cos\frac{\pi(3-VS)}{3} \\ \sin\frac{\pi(1-VS)}{3} & \cos\frac{\pi(VS-1)}{3} \end{bmatrix} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \quad (3)$$

where m_a is the modulation index, which often fluctuates between 0 and 1, while θ specifies the angle of $\vec{V}_{\text{ref}}$. The present study calculates the modulation signal equations as the ratio of the entire conduction duration of the CPSs in each phase leg to the switching period. The conduction time is derived by calculating the mean of the dwell periods of the synthesized NTVs. Due to the varying switching states present in the 3P-2L-UR topologies, it is necessary to calculate the modulation signal expressions independently to ensure their accurate representation. For instance, when the $\vec{V}_{\text{ref}}$ is located inside the initial 30° of VS1, and the five-segment switching sequence is implemented, the modulation signal equations for the phases A, B, and C (m_A, m_B, and m_C) can be obtained for the Wye, Delta, and Bridge topologies using:

$$m_A = (t_1 + t_2 + t_7)/T_S, m_B = (t_2 + t_7)/T_S, m_C = t_7/T_S \quad (4)$$

$$m_A = (t_2 + t_7)/T_S, m_B = 0/T_S, m_C = t_7/T_S \quad (5)$$

$$m_A = 0/T_S, m_B = (t_2 + t_7)/T_S, m_C = t_7/T_S \quad (6)$$

In the advancement of the SVM methodology for the 3P-2L-URs, the dwell time t_7 is equivalent to T_0 and this formulation can be generalized to derive modulation signal expressions for various intervals across all VSs. This can be accomplished by modifying the dwell time equations in accordance with the five-segment switching sequence pertinent to each sector.

C. Generation of Switch Control Signals

The generation of switch driving signals for the CPSs of the 3P-2L-URs across all three proposed topologies in this work relies on the comparison of the produced modulation waveforms with a triangular carrier waveform, adhering to the SVPWM approach. For instance, when the m_a was set to 80%, the resultant A-phase modulation waveforms were compared with a 1 kHz triangular carrier waveform, as portrayed in Figure 4. The results indicate that the resulting switch driving signals display discontinuities; specifically, for the 3P-2L-Wye-UR topology, the switch driving signal remains clamped at '1' for two 60° intervals within each cycle. In contrast, the switch driving signals are restricted to '0' for two 60° intervals in the 3P-2L-Delta-UR and 3P-2L-Bridge-UR models.

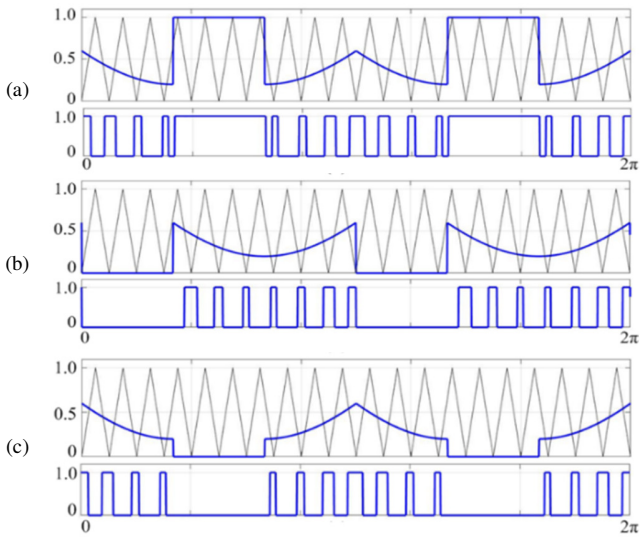

Fig. 4. Example of proposed switch driving signals in the A-phase of the 3P-2L-URs: (a) the 3P-2L-Wye-UR, (b) the 3P-2L-Delta-UR, and (c) the 3P-2L-Bridge-UR.

D. Decoupled Controller Based on VOC Techniques

As depicted in Figure 5 (a), the VOC technique is a widely employed method for regulating the voltage and enhancing PQ in AC-connected power converters. The system operates through the conversion of variables from the three-phase stationary reference frame (abc) to the rotating reference frame (dq), thereby reducing the three control parameters to two. This simplification enhances both the control design and converter integration. This study uses the VOC approach to manage the active and reactive power on the AC side of the proposed 3P-2L-URs [14]. This method ensures consistent output voltage regulation and enhanced input PQ. However, the presence of input inductance leads to disparities between the grid-side and rectifier-side parameters, hence inducing coupling between the d- and q-axis currents:

$$\frac{di_{ds}}{d_t} = \left(v_{ds} - v_{di} + \omega_s L_s i_{qs}\right)/L_s \quad (7)$$

$$\frac{di_{qs}}{d_t} = \left(v_{qs} - v_{qi} + \omega_s L_s i_{ds}\right)/L_s \quad (8)$$

This cross-coupling has the potential to hinder dynamic performance, so a decoupled controller is used, as displayed in Figure 5 (b). The proposed architecture includes three PI controllers, which regulate the DC-link voltage (v_{dc}) by contrasting the measured voltage with its reference (v_{dc}*) and producing the reference d-axis current (i_{ds}*). The secondary PI controller functions as a current regulator, overseeing the d-axis current component (i_{ds}) through the management of the discrepancy between the measured and reference values (i_{ds} and i_{ds}*) to yield the associated reference voltage (v_{ds}*). The third PI controller is responsible for regulating the current loop by adjusting the q-axis current component (i_{qs}) to a value of zero. This process ensures the functionality of the PFC by generating the q-axis voltage reference (v_{qs}*). The equations providing the delineation of the attributes of the PI controllers are:

$$i_{ds}{}^{*} = K_{p1}(v_{dc}{}^{*} - v_{dc}) + K_{i1}\int(v_{dc}{}^{*} - v_{dc})dt \quad (9)$$

$$v_{ds}{}^{*} = v_{ds} + \omega L_s i_{qs} - \left[K_{p2}(i_{ds}{}^{*} - i_{ds}) + K_{i2}\int(i_{ds}{}^{*} - i_{ds})dt\right] \quad (10)$$

$$v_{qs}{}^{*} = v_{qs} + \omega L_s i_{qs} - \left[K_{p2}(-i_{qs}) - K_{i2}\int(i_{qs})dt\right] \quad (11)$$

The gains of the PI voltage controller, K_{p1} and K_{i1}, are determined through the usage of the DC-link capacitance (C_{dc}) and angular frequency (ω_s), with the damping factor (ξ) set at 0.707 [12, 15], as:

$$K_{p1} \geq C_{dc}\xi\omega_s \; and \; K_{i1} \geq 0.5C_{dc}\xi\omega_s \quad (12)$$

The present controllers are characterized by two key parameters: K_{p2} and K_{i2}. These parameters are derived from the input resistance (R_s), inductance (L_s), and a control bandwidth (α_i):

$$K_{p2} = \alpha_i L_s \; and \; K_{i2} = \alpha_i R_s \quad (13)$$

IV. RESULTS AND DISCUSSION

A series of simulation tests was performed using MATLAB/Simulink to assess the feasibility of the proposed control approach and evaluate the reliability and performance of the 3P-2L-URs. The critical simulation parameters employed for both the rectifier topology and the control strategy are presented in Table II.

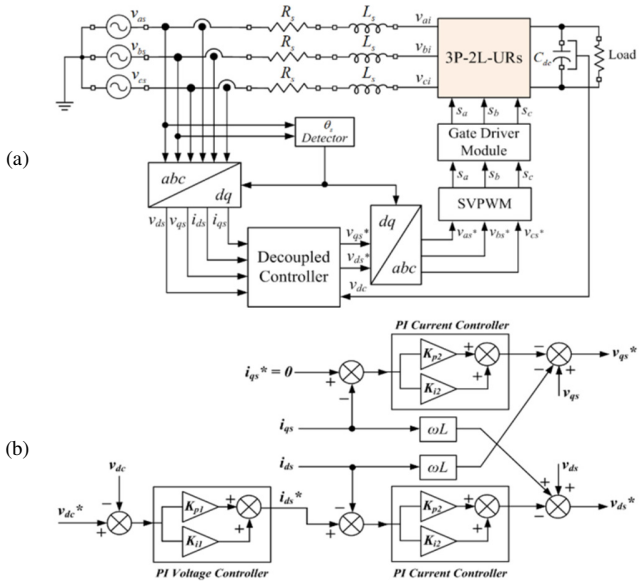

Fig. 5. Overall circuit architecture of the proposed 3P-2L-URs: (a) a decoupled controller with SVPWM on a proposed rectifier, (b) the control structure of the decoupled controller based on VOC techniques.

TABLE II. SPECIFICATIONS OF PARAMETERS USED IN THE SIMULATION

Parameters	Symbols	Value
Output power	P_{out}	60 kW
Source voltage (RMS)	V_{as}, V_{bs}, V_{cs}	230 V
Grid frequency	f	50 Hz
Switching frequency	f_s	12 kHz
DC-link voltage	V_{dc}	800 V
Input inductance	L_s	5 mH
Input resistance	R_s	5 Ω
DC-link capacitance	C_{dc}	2200 μF
Voltage controller	K_{p1}	0.00027
Voltage controller	K_{i1}	0.017
Current controller	K_{p2}	67
Current controller	K_{i2}	1.7×10^4

In Figure 6 (a), the A-phase input current waveform of the 3P-2L-Wye-UR exhibits an almost ideal sinusoidal shape, with a peak amplitude of 160.40 A and a THD_i of the input current measured at 3.89%. The present waveform is in phase with its associated phase voltage, signifying PFC operation. In Figures 6 (b) and 6 (c), the A-phase input current waveforms for the 3P-2L-Delta-UR and 3P-2L-Bridge-UR topologies are presented, respectively. In both topologies, the input currents are sinusoidal, in phase with their respective phase voltages, and exhibit peak values of 160.30 A and 160.40 A, respectively. The relative THD_i results are 3.76% and 3.92%, respectively. Figure 7 presents the DC-link voltage and current waveforms derived from the three topologies of the 3P-2L-URs. In Figure 7 (a), the 3P-2L-Wye-UR configuration generates an average DC-link voltage of 801 V, accompanied by a ripple (Δv_{dc}) of 15.50 V. The resulting average current is

75.50 A, with a ripple (Δi_{dc}) of 1. According to Figure 7 (b), the 3P-2L-Delta-UR generates an average DC-link voltage of 797 V, displaying a ripple (Δv_{dc}) that is 4.00 V greater than that of the 3P-2L-Wye-UR. Notwithstanding the mean current of 75.50 A, the heightened voltage ripple gives rise to a marginally augmented current ripple (Δi_{dc}) of 1.75 A. As illustrated in Figure 7 (c), the 3P-2L-Bridge-UR demonstrates a noteworthy performance, attaining an average DC-link voltage of 804 V, accompanied by a ripple (Δv_{dc}) of 17.55 V. The average current registered at 75.20 A, while the ripple current (Δi_{dc}) was recorded at 1.70 A.

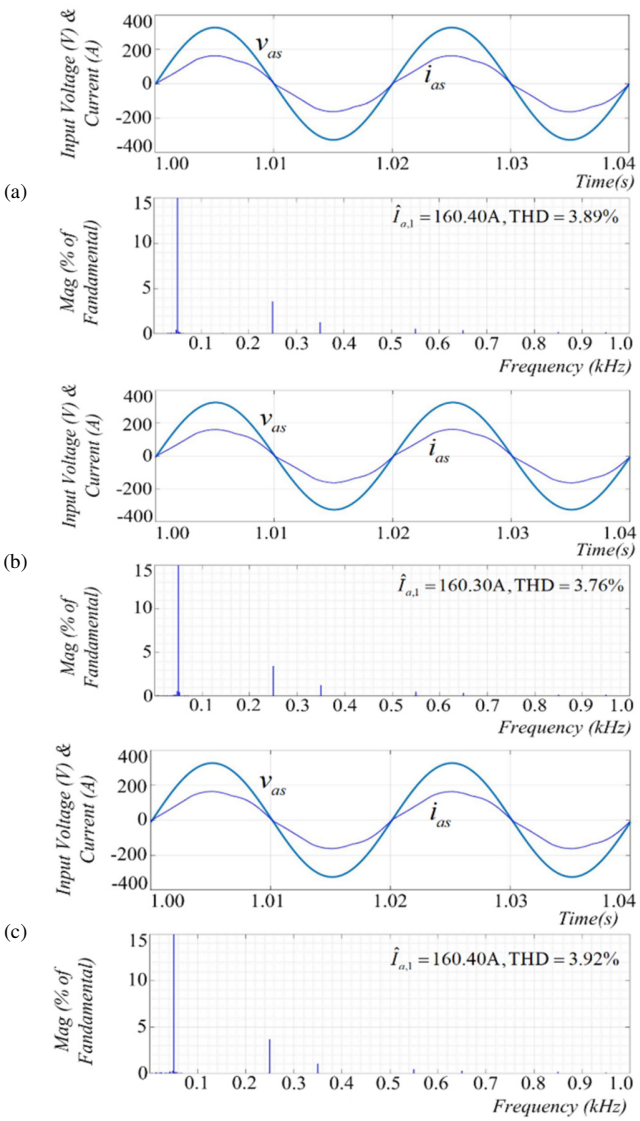

Fig. 6. Comparison of input voltage and current characteristics of the 3P-2L-URs operated under the proposed control scheme: (a) the 3P-2L-Wye-UR, (b) the 3P-2L-Delta-UR, and (c) the 3P-2L-Bridge-UR.

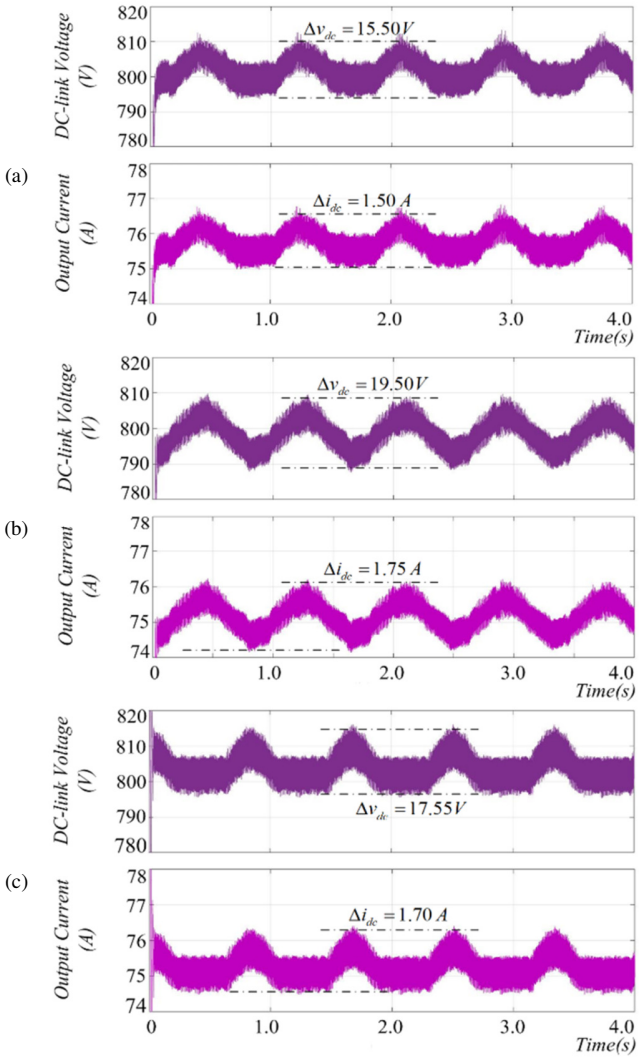

Fig. 7. Comparison of output voltage and current waveforms of the 3P-2L-URs operated under the proposed control scheme: (a) the 3P-2L-Wye-UR, (b) the 3P-2L-Delta-UR, and (c) the 3P-2L-Bridge-UR.

Table III shows all three topologies of 3P-2L-URs in accordance with the international PQ standards. The THD of the input current is maintained below 5%, while the input currents are in phase with their corresponding phase voltages, thereby achieving a unity displacement factor (cosφ = 1.00) and a high overall PF of 99.90%. In the context of EV fast-charging applications, specifically 800 V EV chargers, the 3P-2L-Wye-UR displays the highest VR accuracy, attaining a negligible deviation of 0.13%. Considering factors, such as the battery longevity and the efficacy of the connected devices, which are significantly influenced by the DC voltage and current ripples, the Wye-type topology also exhibits enhanced performance. The configuration produces minimal voltage ripple (Δv_{dc}=15.50 mV) and current ripple (Δi_{dc}=1.50 mA), succeeded by the Bridge-type and Delta-type topologies, in that order. The findings indicate that the 3P-2L-Wye-UR topology is a viable solution for high-performance, grid-connected DC fast-charging systems.

TABLE III. COMPARISON OF INPUT PQ AND OUTPUT CHARACTERISTICS FOR THE PROPOSED 3P-2L-URS

Symbols	**Meaning of symbols**	**3P-2L-URs**		
		Wye-type	Delta-type	Bridge-type
THD_i	THD of input current (%)	3.89	3.76	3.92
cos(ϕ)	Displacement factor	1.00	1.00	1.00
PF	PF (%)	99.92	99.93	99.92
VR	Voltage regulation (%)	0.13	0.38	0.50
Δv_{dc}	DC voltage ripple (*V*)	15.50	19.50	17.55
Δi_{dc}	DC current ripple (*A*)	1.50	1.75	1.70

V. CONCLUSIONS

The present study offers an examination of the design and development of 3P-2L-URs for 800 V Electric Vehicles (EV) fast-charging applications. This examination uses a combination of Space Vector Pulse Width Modulation (SVPWM) and a decoupled controller based on the Voltage-Oriented Control (VOC) technique. A thorough investigation was conducted on three topologies: Three-Phase, Two-Level, Wye-type, Unidirectional Rectifier (3P-2L-Wye-UR), 3P-2L-Delta-UR, and 3P-2L-Bridge-UR. The focus of this study was on three key areas: operational functionality, modulation signal formulations, and control strategies. The control technique efficiently enables the production of proper switching signals through active and reactive power regulation in the dq-axis frame. The simulation results indicate that all three rectifier topologies comply with the IEEE 519 and IEC 61000-3 standards, maintaining Total Harmonic Distortion (THD_i) below 5% and achieving PFC. Among the three topologies, the 3P-2L-Wye-UR demonstrates the most superior overall performance, producing minimal voltage and current ripples and exhibiting improved voltage regulation. These characteristics are crucial for enhancing the battery lifespan and the reliability of connected devices. The proposed 3P-2L-URs exhibit significant advantages over their 3P-3L-UR counterparts, which require a dual-capacitor voltage balancing system. The 3P-2L-URs use a single DC-link capacitor, leading to a reduction in the component count, decreased manufacturing costs, and diminished maintenance requirements. The five-segment switching sequence technique has reduced the switching losses, thereby enhancing the energy efficiency and consequently decreasing the operational costs over time. The rectifier topology and control strategy that have been proposed can be considered technically reliable and economically viable for extensive implementation in the EV charging infrastructure. Furthermore, the proposed methodology enhances the Power Quality (PQ) and reduces the thermal stress on the Charging Point Systems (CPSs), thus fostering grid stability and prolonging the equipment lifespan. These advantages contribute to the long-term sustainability of the public charging stations. The proposed 3P-2L-URs topology is a viable, scalable, and advantageous approach to address the increasing need for high-efficiency EV fast chargers in contemporary smart grid scenarios.

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