Design of a Discontinuous SVPWM Strategy-Based Current Controller in DQ Synchronous Frame for the Grid-Connected 3L-T-Type Inverter

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ABSTRACT

This study proposes an innovative discontinuous Space Vector Pulse Width Modulation (SVPWM) technique integrated with a DQ-based current control scheme for a three-level T-type (3L-T-Type) inverter running in grid-connected mode. The discontinuous modulation technique employs the Nearest Three Vectors (NTVs) from the space vector diagram to provide appropriate switching signals, which substantially decreases the commutation of the Controllable Power Switches (CPSs), thus reducing switching losses. To enhance the output power quality prior to grid injection, a transformation from standard DQ current control to active and reactive Power Control (PQ) is implemented. The proposed method allows for separate control of the d-axis and q-axis components while keeping them in sync with the grid voltage. A mathematical model was developed to compute the stay time of each switching state across different regions and sectors, facilitating the generation of discontinuous modulation waves for each phase leg. The simulation results in MATLAB/Simulink demonstrate improved performance with a 33% reduction in switching commutations, a Total Harmonic Distortion (THD) of 4.67% for the current, proper alignment with the grid voltage at the main frequency of 50 Hz, and effective balancing of the DC-

link voltage. These findings confirm the proposed controller's efficacy and its appropriateness for high-performance grid-connected applications, including renewable energy integration and electric vehicle infrastructure.

Keywords-3L-T-Type inverter; SVPWM; DQ control; grid-connected inverter; harmonic distortion

I. INTRODUCTION

The integration of electricity produced by renewable energy resources, such as photovoltaic systems, wind farms, synchronous generators, rectifier topologies, and fuel cells, has accelerated. This trend is driven by the global pursuit of cleaner, more sustainable, and efficient energy sources [1]. Renewable energy sources offer many advantages, such as no greenhouse gas emissions, easy access and implementation, and a high return on investment, making them increasingly attractive for both large-scale and small-scale energy generation [2]. Nevertheless, the electricity produced by renewable energy sources cannot be immediately consumed by electrical loads or the grid because of the unpredictable and intermittent characteristics of these sources [3]. Consequently, power electronic converters are important components that operate as connectors between renewable energy systems and electrical equipment. These converters include DC–AC inverters that help connect renewable energy to the grid and supply power, as well as DC–DC converters utilized for regulating voltage, connecting to energy storage, and optimizing power output. When considering the load or grid side, the system-side converter must perform several tasks, including (a) synchronization with the grid, (b) regulating reactive (Q) and active power (P), (c) regulating the DC-link voltage, and (d) supplying high-quality power [4, 5].

In grid-tied inverter applications, it is desirable to deliver a completely sinusoidal waveform to the utility grid rather than injecting current or voltage waveforms with diminished harmonic content. The traditional two-Level Voltage Source Inverters (2L-VSIs) are commonly utilized for small-scale applications because of their structural simplicity and ease of control. However, this topology has significant disadvantages that make it unsuitable for medium- and large-scale systems. These involve higher voltage stress on the switching devices and significant heat loss. These problems result in diminished overall system efficiency and reliability [5]. Three-Level Voltage Source Inverters (3L-VSIs) have been developed to overcome the limitations of conventional inverter topologies and are now extensively utilized in industrial applications [6, 7]. 3L-VSIs offer many advantages over traditional 2L-VSIs, including better performance with harmonics, higher efficiency, lower voltage stress on switching devices when loads change, and lower electromagnetic interference. These characteristics render 3L-VSIs exceptionally appropriate for medium- and high-power grid-connected applications, where power quality and efficiency are important [8]. Two types of 3L-VSI designs have been found that are often used in modern power electronics: the three-Level Neutral-Point-Clamped (3L-NPC) inverter and the 3L-T-Type inverter. These inverter designs can produce three different output voltages, resulting in reduced THD, slower voltage change rate (dv/dt), and better performance at lower switching frequencies. Moreover, the voltage ratings necessary for both the power switches and capacitors represent the DC-link voltage, which is only half of its total, providing substantial benefits for both device selection and system stability.

There are significant differences between the 3L-NPC and 3L-T-Type inverter topologies. The 3L-T-Type inverter employs four CPSs per inverter leg and neglects clamping diodes, therefore simplifying the topology design and improving the overall efficiency [9]. However, even though the 3L-T-Type inverter has lower conduction losses than the 3L-NPC, it usually has higher switching losses. The voltage imbalance of the two input-side DC-link capacitors is a significant problem that must be addressed [10]. To fully harness the 3L-T-Type inverter in high-performance power conversion applications, these challenges must be resolved. A study of the relevant literature shows that two main methods are commonly used for 3L-VSI: carrier-based Space Vector Modulation (SVM) and Pulse-Width Modulation (PWM) [11]. Carrier-Based Pulse-Width Modulation (CB-PWM) is a widely used method for 3L-VSI, which includes methods, like carrier Phase-Shifted PWM (PS-PWM) and carrier Level-Shifted PWM (LS-PWM) that are easy to implement digitally. Additionally, complex carrier-based approach implementations require adjusting the harmonic composition and carrier frequency of the reference signal. This results in minimized switching losses and improved output waveform quality. Nevertheless, the available DC-link voltage at the VSI cannot be fully utilized by this method, and the algorithm does not facilitate continuous power advancement. The SVM uses a DC-link voltage that is 15% higher than the CB-PWM, which improves the use of the DC bus [12, 13]. Moreover, it reduces the THD and switching losses through proper switching patterns. Most previous studies emphasize continuous SVM methodologies, which require high switching frequencies and lack the proper utilization of the topology-specific switching capabilities of the 3L-T-Type inverter [14, 15]. Currently, there is an absence of thorough modulation techniques that are both topology-aware and loss-minimizing for 3L-T-Type inverter functioning in grid-connected applications. Despite the recognized advantages of the 3L-T-Type inverter topology, few studies have explored discontinuous modulation techniques that minimize switching losses while preserving grid synchronization and power quality [16, 17]. To address these gaps, this study proposes a new discontinuous SVPWM method for a 3L-T-Type inverter in grid-connected applications. The proposed approach utilizes the NTVs from the SVM diagram to minimize the number of switching commutations per phase leg, thereby considerably lowering the switching losses. The hybrid control method integrates the CB-PWM principles with the SVM technique to produce the switching signals. The method, embedded with a d–q synchronous reference frame, facilitates the accurate regulation of active and reactive power while ensuring a minimal THD. Topology-specific switching control combined with current regulation in the d–q synchronous reference frame provides a pragmatic and efficient method for achieving high-performance

3L-T-Type inverter systems for next-generation renewable energy applications.

II. WORKING PRINCIPLE OF 3L-T-TYPE GRID-CONNECTED INVERTER

The circuit of the 3L-T-Type inverter shown in Figure 1 has 4 CPSs for each inverter leg, labeled $S_{a1\text{-}a4}$ for the *a*-phase, $S_{b1\text{-}b4}$ for the *b*-phase, and $S_{c1\text{-}c4}$ for the *c*-phase, resulting in a total of 12 CPSs for all three phases. Each inverter leg operates in three particular switching states: -1, 0, and 1. A voltage level of 0.5 V_{dc} represents 50% of the input DC-link voltage, facilitating the generation of three output voltage levels (+0.5 V_{dc}, 0, and -0.5 V_{dc}). Table I lists the switching states and corresponding output levels for the *a*-phase leg as a representative example, whereas the *b*- and *c*-phases correspond to the same operational principle.

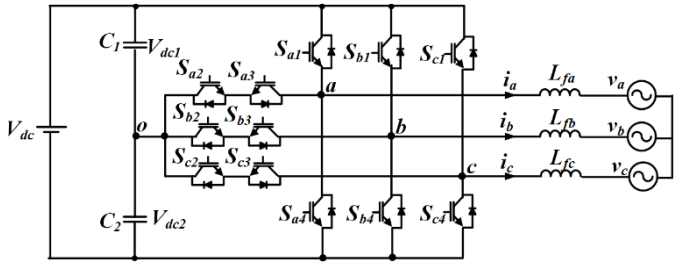


Fig. 1. Topology of 3L-T-Type grid-connected inverter.

TABLE I. SWITCHING STATES AND OUTPUT LEVELS OF THE A-PHASE LEG

switching state	CPSs for the a-phase leg				Output voltage levels
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	
1	ON	ON	OFF	OFF	+0.5 V_{dc}
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	-0.5 V_{dc}

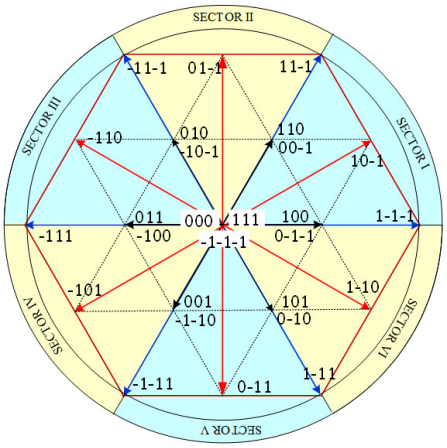
When connecting the 3L-T-Type inverter to the grid, L_{fa}, L_{fb}, and L_{fc} are the AC-side filter inductors for the *a*-, *b*-, and *c*-phases, respectively, and v_a, v_b, and v_c are the corresponding grid voltages for each phase. The mathematical model of a grid-connected inverter with a balanced three-phase AC power supply, represented in the three-phase stationary reference frame (abc), can be formulated using Kirchhoff's current law, as expressed in:

$$\begin{cases} \frac{di_a}{d_t} = -\frac{r}{L_{fa}} i_a - \frac{1}{L_{fa}} v_{ao} + \frac{1}{L_{fa}} v_a \\ \frac{di_b}{d_t} = -\frac{r}{L_{fb}} i_b - \frac{1}{L_{fb}} v_{bo} + \frac{1}{L_{fb}} v_b \\ \frac{di_c}{d_t} = -\frac{r}{L_{fc}} i_c - \frac{1}{L_{fc}} v_{ao} + \frac{1}{L_{fc}} v_c \end{cases} \quad (1)$$

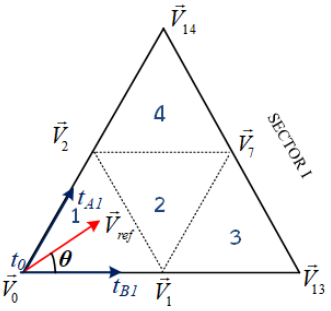
The parameters i_a, i_b, and i_c represent the grid-connected currents for the *a*-, *b*-, and *c*-phases, respectively, *r* indicates the equivalent resistance of the AC-side inductors in the 3L-T-Type inverter, and v_{ao}, v_{bo}, and v_{co} denote the voltage drops between each inverter leg's neutral point and the grid's neutral point.

III. DESIGN OF DISCONTINUOUS SWITCH CONTROL SIGNAL BASED ON SVPWM

As depicted in Figure 2(a), the space vector diagram of the 3L-VSI is split into six triangular sectors (I to VI), each of which is further split into four smaller triangular regions (1-4). The complete set of switching states yields 27 possible switching combinations, corresponding to 19 distinct voltage vectors, labeled V_0-V_{18}. The voltage vectors are categorized into four groups according to their magnitudes. The zero vector (V_0) is associated with three switching states that produce zero output voltage: [+1 +1 +1], [0 0 0], and [–1 –1 –1]. The small vectors (V_1 to V_6) possess a magnitude of 0.33 V_{dc} and are each linked to two separate switching states, either [+1] or [–1]. These switching states categorize small vectors into P- and N-types. The medium vectors (V_7-V_{12}) exhibit a magnitude of 0.58 V_{dc}, while the large vectors (V_{13}-V_{18}) demonstrate a magnitude of 0.67 V_{dc}.



(a)



(b)

Fig. 2. Space vector diagram for the 3L-VSI inverter. (a) Sector and region segmentation, (b) region boundary and dwell time of sector I.

A. Simplified Dwell Time Calculation

The basic concept of the SVM technique is based on the selection of the NTVs to generate the V_{ref}. The instantaneous value of V_{ref} and the sampling period (T_s) are obtained from the combined effect of the NTVs linked to the specific triangular region, with each one multiplied by its corresponding dwell time. This method complies with the volt-second balancing principle. For example, if V_{ref} rotates within region 1 of sector I, the volt-second balancing equation can be expressed as:

$$\vec{V}_{ref}T_S = 2[t_{A1}\vec{V}_2 + t_0\vec{V}_0 + t_{B1}\vec{V}_1] \quad (2)$$

$$T_S = 2[t_{A1} + t_0 + t_{B1}] \quad (3)$$

were t_0 denotes the dwell time of the null vector ($\vec{V}_0$), while t_{A1} and t_{B1} are the dwell time for the non-null vectors $\vec{V}_1$ and $\vec{V}_2$, respectively. However, the SVM technique for the 3L-T-Type inverter determines the magnitudes of the three voltage vectors by projecting the input DC-link voltage (V_{dc}) onto the two-phase stationary reference frame (αβ). Thus, the magnitudes of the voltage vectors $\vec{V}_0$, $\vec{V}_1$, and $\vec{V}_2$ for this case can be expressed as:

$$\vec{V}_0 = 0,\ \vec{V}_1 = \frac{V_{dc}}{3}\ and\ \vec{V}_2 = \frac{V_{dc}}{3}(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}) \quad (4)$$

The three dwell time expressions required for switching a 3L-T-Type inverter are derived by substituting (3) and (4) into (2), which are dependent on the instantaneous reference voltage vector, the input DC-link voltage, and the reference voltage angle (θ), as detailed in:

$$\begin{cases} t_0 = \frac{1}{2}\left[T_S - \sqrt{3}m_aT_S\cos\theta - m_aT_S\sin\theta\right] \\ t_{B1} = \frac{1}{2}\left[\sqrt{3}m_aT_S\cos\theta - m_aT_S\sin\theta\right] \\ t_{A1} = m_aT_S\sin\theta \end{cases} \quad (5)$$

where m_a is the modulation index for the SVM technique, which ranges from 0 to 1 and is expressed as:

$$m_a = \sqrt{3}\frac{V_{ref}}{V_{dc}} \quad (6)$$

However, the dwell time expressions derived in (5) are applicable only when V_{ref} falls within region 1 of sector I. If V_{ref} moves into region 1 of a different sector, the same analytical technique must be repeated using the NTVs relevant to that sector. Moreover, as described in (6), the magnitude of V_{ref} may fluctuate based on the modulation index and input DC-link voltage. Consequently, V_{ref} may surpass region I and encroach upon regions 2, 3, and 4 of a specified sector, as depicted in Figure 2(b). This situation requires for the calculations for the dwell time in each case to be redone, which complicates the SVM implementation. This paper presents a mathematical model to compute dwell time expressions for each voltage vector using the 3L-SVM method. The model categorizes the analysis into three cases according to the magnitude of V_{ref}:

Case 1: If the reference vector rotates within region 1 of any sector (i.e., a miniature vector), the applicable dwell time equation can be calculated using (7), where n is the sector number (n = 1, 2, …, 6):

$$\begin{bmatrix} t_{An} \\ t_{Bn} \end{bmatrix} = m_aT_s\begin{bmatrix} \sin(1-n)\frac{\pi}{3} & \cos(1-n)\frac{\pi}{3} \\ \sin(3-n)\frac{\pi}{3} & \cos(3-n)\frac{\pi}{3} \end{bmatrix}\begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \quad (7)$$

Case 2: If the reference vector lies within region 2 of any sector (i.e., a medium vector), the identical dwell time equation is utilized:

$$\begin{bmatrix} t_{An} \\ t_{Bn} \end{bmatrix} = m_aT_s\begin{bmatrix} \sin(6-n)\frac{\pi}{3} & \cos(6-n)\frac{\pi}{3} \\ \sin(4-n)\frac{\pi}{3} & \cos(4-n)\frac{\pi}{3} \end{bmatrix}\begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} + 0.5T_s \quad (8)$$

Case 3: If the reference vector is located within region 3 or region 4 of any sector (i.e., a large vector), the same equation is employed:

$$\begin{bmatrix} t_{A1n} \\ t_{B1n} \\ t_{A2n} \\ t_{B2n} \end{bmatrix} = m_aT_s\begin{bmatrix} \sin(n-2)\frac{\pi}{3} & -\cos(n-2)\frac{\pi}{3} \\ \sin(3-n)\frac{\pi}{3} & \cos(3-n)\frac{\pi}{3} \\ \sin(1-n)\frac{\pi}{3} & \cos(1-n)\frac{\pi}{3} \\ \sin(5-n)\frac{\pi}{3} & \cos(5-n)\frac{\pi}{3} \end{bmatrix}\begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} + T_s\begin{bmatrix} 1 \\ -0.5 \\ -0.5 \\ -1 \end{bmatrix} \quad (9)$$

B. Discontinuous Control Signal Generation Based on the Switching Sequence of NTVs

This study employs a five-segment switching sequence technique to reduce the number of switching commutations in each phase leg of the 3L-T-Type inverter. This approach strategically arranges the discrete switching states of the NTVs within each region to minimize switching commutations. For example, when the V_{ref} rotates within region 2 of sector I, the associated switching sequence is displayed in Figure 3. Only two of the three inverter legs experience two switching transitions, whereas the third leg remains fixed. This diagram illustrates the generation of discontinuous switching control signals, which decreases the total number of switching commutations by approximately one-third compared to traditional switching methods.

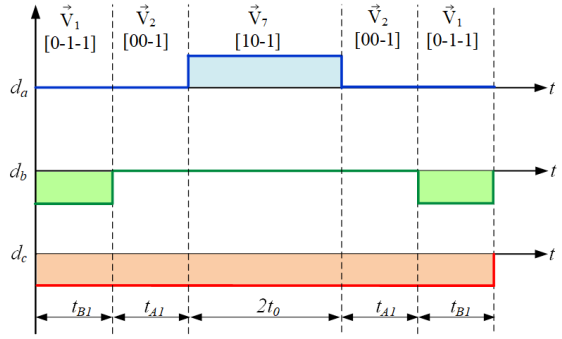


Fig. 3. Switching signal sequence diagram for region 2 of sector I.

C. Three-Phase Duty Cycle Analysis

This study uses a method for calculating the duty cycle determined by the ratio of the total conduction period for the three successive voltage vectors in each phase leg to the sampling period (T_s). The conduction period for each phase leg was determined by summing the times when the switching states were on, which created the NTVs. For example, as illustrated in Figure 3, the duty cycle equations for the three-phase legs d_a, d_b, and d_c can be expressed as:

$$\begin{cases} d_a = \frac{2t_0}{T_s} \\ d_b = \frac{-2t_{B1}}{T_s} \\ d_c = \frac{-2t_0 - 2t_{B1} - 2t_{A1}}{T_s} \end{cases} \quad (10)$$

By using the dwell time equations t_0, t_{A1} , and t_{B1} from (8) in (10), the duty cycle equations for the three-phase legs (d_a, d_b, and d_c) can be rewritten as:

$$\begin{cases} d_a = -1 + \sqrt{3} m_a \cos\theta + m_a \sin\theta \\ d_b = -1 + 2 m_a \sin\theta \\ d_c = -1 \end{cases} \quad (11)$$

This mathematical method can be further expanded to determine modulation expressions for other regions within the remaining sectors, which simplifies the generation of discontinuous three-phase modulation waveforms. The waveforms were compared with two triangular carrier signals by applying the two-level shifted PWM (2LS-PWM) approach. The switching signals generated by after the comparison with the upper triangular carrier directly control CPS 1 and work as the opposite signals for CPS 3 in each inverter leg. Similarly, the signals from the comparison with the lower triangular carrier are used to directly control CPS 2 and act as opposite signals for CPS 4. Similarly, the signals derived from the comparison with the lower triangular carrier are utilized to control CPS 2 immediately and serve as the inverse logic for CPS 4.

IV. TRANSFORMATION OF DQ CURRENT CONTROL INTO PQ CONTROLLER

This study modifies the traditional d–q current control into an active and reactive power management technique to improve power regulation and achieve decoupled control in grid-connected inverter systems, as shown in Figure 4. In the Synchronous Rotating Reference Frame (SRRF), the three-phase AC variables are converted into the d–q axis by the park transformation. This approach directly correlates the d-axis current (i_d) with the active power (P) and the q-axis current (i_q) with the reactive power (Q) [18]. The correlations between these variables are expressed as:

$$P = \frac{3}{2}\left(v_d i_d + v_{gq} i_q\right) \quad (12)$$

$$Q = \frac{3}{2}\left(v_d i_q - v_{gq} i_d\right) \quad (13)$$

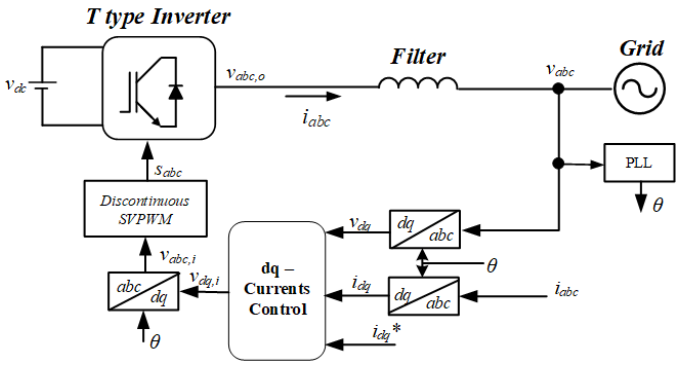


Fig. 4. Overall control structure of the d-q current controller with the SVPWM technique applied to a 3L-T-Type inverter.

The d-q components of the grid voltage are represented by v_d and v_q. By autonomously controlling i_d and i_q, the inverter can precisely control the flow of active and reactive power. However, the effect of grid-side inductance causes a difference between the current and voltage on the grid side and those on the inverter side. A d-q decoupled control technique is proposed to address this problem, as presented in Figure 5. The control equation for each axis is defined as:

$$v_{di} = v_d + \omega L_f i_q - v_d^* \quad (14)$$

$$v_{qi} = v_q - \omega L_f i_d - v_q^* \quad (15)$$

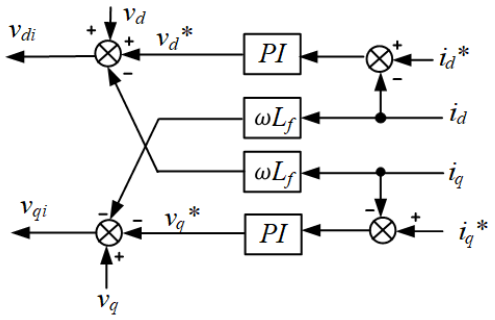


Fig. 5. The control structure of the d-q decoupled control strategy.

The control system utilizes a cascaded structure, as defined in (16) and (17), wherein the P–Q controllers establish the reference values for the d–q current control loops. Proportional-Integral (PI) controllers are used in both loops to manage the voltage command signals on the d- and q-axes:

$$v_d^* = K_p(i_d^* - i_d) + K_i \int (i_d^* - i_d) dt \quad (16)$$

$$v_q^* = K_p(i_q^* - i_q) + K_i \int (i_q^* - i_q) dt \quad (17)$$

where K_p and K_i are the proportional and integral gains of the PI controllers, respectively. This control approach not only improves the dynamic response of the system under transient conditions, but also ensures compliance with grid code requirements related to power factor regulation, voltage support, and reactive power compensation.

V. RESULTS AND DISCUSSION

To ascertain the effectiveness of the proposed discontinuous SVPWM-based current control strategy for the 3L-T-Type grid-connected inverter, a series of simulated tests were performed using MATLAB/Simulink. The simulation parameters are summarized in Table II.

TABLE II. SYSTEM PARAMETERS FOR SIMULATION

Parameters	Symbol	Value
DC bus voltage	V_{dc}	600 V
Grid voltage (RMS)	v_a, v_b, v_c	220 V
Input capacitors	C_1, C_2	2200 µF
Switching frequency	f_s	2 kHz
Grid frequency	f	50 Hz
Filter inductors	L_f	20.7 mH
Filter capacitors	C_f	20 µF

A. Switching Loss Reduction Analysis

Figure 6 illustrates the discontinuous modulation signal and associated gate signals for the 4 CPSs (S_{a1}–S_{a4}) that constitute

the *a*-phase leg of the proposed 3L-T-Type inverter during grid-synchronized operation. The top waveform shows the modulation signal along with two triangular carrier signals, and the bottom lines show the gate signals for each CPS in the leg. The switching signals indicate that the S_{a1} and S_{a3} operate complementarily to regulate the output voltage's positive half-cycle. Similarly, S_{a2} and S_{a4} regulate the negative half-cycle during complementary operation. Each CPS shows a switching pattern that is not continuous, with a pause of approximately 60 electrical degrees during each half-cycle, either at the positive rail or at the midpoint (zero potential). These intervals significantly decrease the number of commutations for each CPS inside a single cycle. The same modulation waveform and switching logic are used for the CPSs in the *b*- and *c*-phase legs, with appropriate laggings of 120° and 240° to maintain the necessary three-phase balance. The quantitative assessment of the commutation frequency indicates a 33.0% decrease in switching commutation per switching device compared to the traditional continuous PWM methodologies. This significant reduction directly leads to fewer switching losses and thermal stress, improving the overall inverter efficiency and reliability.

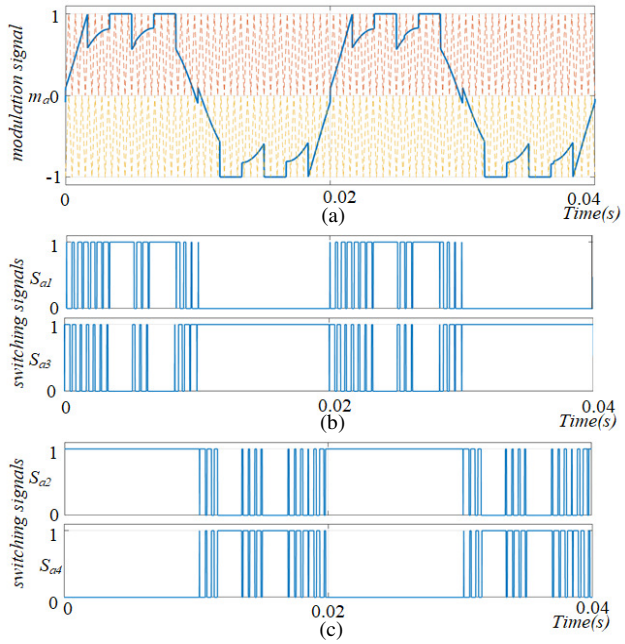


Fig. 6. Example of proposed switch driving signals for CPSs in a-phase leg: (a) modulation signal for a-phase, (b) switching signals for S_{a1} and S_{a3}, and (c) switching signals for S_{a2} and S_{a4}.

B. Steady-State Performance Evaluation

Figure 7 demonstrates that the system operates at a nominal frequency of 50 Hz with an almost unity power factor (pf > 0.99) and is synced to the specific grid voltage. In Figure 7a, the grid current demonstrates a high-quality sinusoidal shape and is precisely in phase with the corresponding grid voltage waveform, signifying efficient synchronization and Power Factor Correction (PFC). The harmonic analysis reveals that the total THD of the grid current is 4.67 %, which is much lower than the limit set by IEEE 519 (THD_i < 5%), showing that the inverter successfully provides low-distortion current. In Figure 7(b), the line-to-line PWM output voltage waveform indicates a distinct five-level stepped pattern with separate voltage levels at ±600 V, ±300 V, and 0 V, resulting from the adoption of a three-level modulation technique. Both waveforms exhibit robust synchronization at the fundamental frequency of 50 Hz. Moreover, the peak amplitude of the filtered PWM line-to-line voltage corresponds to that of the grid-side line-to-line voltage, measured at 537.40 V. This correlation signifies accurate voltage control and validates the efficacy of the control approach in preserving voltage uniformity throughout the interface. Figure 7(c) illustrates the DC-link voltage in conjunction with the voltages across two DC capacitors. The voltage profiles demonstrated excellent voltage balance, with each capacitor sustaining a consistent voltage of approximately 50% of the DC source voltage, as necessary for the effective functioning of the 3 L-T-Type inverter. The ripple content is negligible, guaranteeing reliable capacitor performance and uniform neutral-point potential.

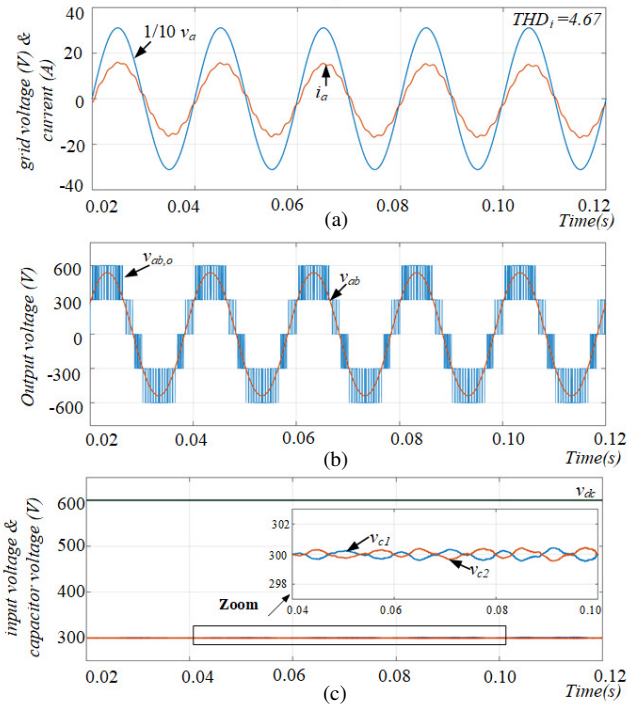


Fig. 7. Steady-state simulation waveforms of the proposed 3L-T-Type inverter under grid-connected conditions: (a) grid voltage and current of phase-a, (b) line-to-line PWM output voltage and the corresponding grid voltage, and (c) input DC-link voltage and individual capacitor voltages.

The simulation results validate that the proposed 3L-T-type inverter can provide a smooth sinusoidal voltage and current to the grid, maintain a balanced DC-link voltage, and significantly reduce switching commutations. In comparison, previous studies[14-17] have predominantly concentrated on continuous SVM techniques for both generic 3L-VSI and specialized 3L-T-type inverters, which require high switching frequencies. This results in significant switching losses and inadequate usage of the topology-specific switching capabilities of the 3L-T-Type inverter. This work addresses these gaps by proposing

a modulation strategy that decreases switching commutations per phase leg by 33%, reducing switching losses, and improving reliability and efficiency. The system incorporated a d–q synchronous frame controller with P–Q regulation, enabling precise control of active and reactive power. This design ensures grid synchronization and compliance with the electricity quality requirements, maintains a low THD of the output current (THD_i = 4.67%), achieves excellent DC-link voltage balance, and sustains a unity power factor ($pf > 0.99$) throughout steady-state operation. This methodology rectifies a notable deficiency by combining modulation efficiency with topology-aware control, in contrast to prior studies that neglect the structural benefits of the 3L-T-Type topology, thereby facilitating advanced renewable power systems, electric vehicle systems, and high-efficiency energy conversion platforms.

VI. CONCLUSIONS

This study presents a discontinuous Space Vector Pulse Width Modulation (SVPWM)-based current control method designed for a 3L-T-Type inverter functioning under grid-connected conditions. The modulation method used the Nearest Three Vectors (NTVs) from the space vector diagram to create discontinuous modulation waves compared to using two triangular carrier signals, which led to four switching signals for each Controllable Power Switches (CPS) in the inverter topology. The method significantly reduced switching commutations by approximately 33% relative to traditional continuous SVPWM techniques, lowering switching losses and thermal strain on power components. Additionally, by changing the DQ current control to a P–Q control method. The system effectively managed active and reactive power independently, which improved the inverter's steady performance and compliance with grid standards. The simulation results confirmed that the proposed control strategy can produce a low Total Harmonic Distortion (THD) sinusoidal output, establish robust synchronization with the grid voltage, and maintain balanced capacitor voltages. These benefits validate the applicability of this control technology for implementation in contemporary renewable energy systems and high-efficiency power conversion platforms.

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