Design of a High-Gain, Low-Noise CMOS LNA for Compact Front-End Ground Penetrating Radar Systems

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ABSTRACT

This paper presents the design and simulation of a high-performance cascoded common-source degenerated Low-Noise Amplifier (LNA) using standard 180-nm CMOS technology and the Cadence Virtuoso platform. The proposed LNA provides excellent Radio Frequency (RF) performance while maintaining low power consumption and a compact layout, making it ideal for integration into portable Ground Penetrating Radar (GPR) systems. The amplifier has an input return loss of –20 dB across the ultra-wideband frequency range, ensuring effective impedance matching, while delivering a high peak gain of 28.5 dB and exhibiting a low minimum Noise Figure (NF) of 0.666 dB. This improves the signal sensitivity and overall system performance. The linearity metrics include a 1-dB compression point (P1 dB) of –18 dBm and a third-order intercept point (IIP3) of –17 dBm, indicating a good dynamic range for wideband applications. The circuit operates at 1.5 V power supply with a total power consumption of only 1.67 mW. The combination of low noise, high gain, and low power consumption makes the proposed LNA ideal for modern UWB receiver front ends in radar and communication systems.

Keywords-common source topology; Ground Penetrating Radar (GPR); gain; Low Noise Amplifier (LNA); noise figure;RF front end

I. INTRODUCTION

GPR is one of the most adaptable sensing technologies used today for remotely detecting buried objects. Using Electromagnetic (EM) wave propagation and reflection, GPR is sensitive to changes in subsoil EM parameters, especially the dielectric constant and electrical conductivity. GPR operates by transmitting an incident field through a transmitting (T_x) antenna, which hits a target (buried or embedded) and backscatters a field. This field is then collected by a receiving (R_x) antenna. Designing LNAs that simultaneously achieve high gain, low noise figure, wide bandwidth, and minimal distortion remains a persistent challenge in RF front-end development. Early efforts, such as wideband co-design approaches that coupled active antennas with LNAs, exhibited only limited improvement in linearity. To overcome challenges, such as poor linearity, weak impedance matching, and high noise levels, this paper presents a refined LNA design for advanced RF receiver systems. A design implemented in 65-nm CMOS technology demonstrated peak gains of 19.98 dB and minimum noise figures of 1.94 dB, while it achieved compact area efficiency for Ku-band applications [1]. Recent LNA designs have adopted large-transistor techniques in the input stage and differential Class-AB configurations in the output stage to achieve high linearity and low noise. This methodology improves the 1-dB compression points of both the input and output while maintaining low-power operation. One recent design uses a low-power, high-gain, low-noise CMOS RF front end with a Gmax-driven active mixer and a two-stage LNA to enhance performance [2]. Authors in [3] proposed a 65-nm CMOS VG-LNA with a high-order transformer-based matching network and dual-phase compensation. This design achieved a wide 3-dB bandwidth of 19 GHz–45 GHz with low NF and phase error. Building on the

specific approach, this study explores enhanced gain control and noise optimization in wideband LNA design. Authors in [4] proposed a novel design that uses a tri-coupled transformer for GM boosting and improved noise cancellation, achieving a 3-dB bandwidth of 22.1 GHz and a minimum NF of 3.8 dB. Authors in [5] proposed a 40-nm CMOS NC-LNA that uses a GM-boosted common-gate stage and transformer coupling to enhance gain and bandwidth while minimizing NF and power consumption. Authors in [6] introduced a 28 GHz low-power Variable-Gain LNA (VGLNA) designed specifically for fifth-generation millimeter-wave applications. When measured at 28 GHz with a 1.2 V supply, the VGLNA delivers a peak gain of 21.2 dB, a gain-control range of 13.8 dB, an NF ranging from 3.7 to 6.8 dB, and an IP1dB spanning from −20 to −7 dBm. It also consumes only 5 mW of DC power. Cognitive Radio (CR) is an ultra-wideband system that operates from 50 MHz to 10 GHz and is designed to enhance spectrum efficiency through dynamic monitoring. An ultra-wideband differential LNA using Cascaded Flipped-Active Inductors (CASFAI) was developed, with each stage using a gyrator-capacitor structure with a feedback PMOS. The capacitor cross-coupling improves transconductance, gain, and noise performance while lowering power consumption [7]. Designed in a 0.18-µm CMOS process and verified through post-layout simulation, the circuit achieves input matching better than −10 dB, a maximum gain of over 10.6 dB, a minimum NF of 2.24 dB, a stability factor greater than 2.8, an III-point (IIP3) of −2.3 dBm, and consumes 6.12 mW from a 1.8-V supply [8]. Authors in [9] proposed a 38 GHz LNA for satellite communications that uses a three-stage, common-source, inductive-degeneration topology. This design achieves 27 dB of gain and a 1.78 dB NF using 0.1 µm gallium arsenide (GaAs) pHEMT devices. The design's innovation lies in integrating inductive loads in series with resistors, which improves gain performance compared to conventional resistive loads. Authors in [10] introduced dual Q/V-band LNAs using a SiGe BiCMOS process that integrates Q-enhanced metamaterial transmission lines, enabling efficient operation across the 33–50 GHz and 50–75 GHz bands. These innovative metamaterial lines increase the resonator Q, resulting in improved gain flatness and a lower NF than conventional millimeter-wave LNA topologies. Authors in [11] explored a compact, electrically small antenna using SRR for RFID applications, highlighting space-efficient solutions for wireless systems. Authors in [12] proposed a funnel-shaped Multiple-Input Multiple-Output (MIMO) antenna for radar applications, achieving enhanced isolation and bandwidth. Additionally, authors in [13] introduced a low-profile, reconfigurable, wideband BPF that employs RF-MEMS switches for 5G and satellite use. This design showcases tunability and compactness in modern RF front ends. Authors in [14] presented a two-stage LNA that covers 22–47 GHz and uses coupled L-type interstage matching inductors to achieve a peak gain of 22.2 dB, broadening the amplifier's bandwidth and flattens its gain response while maintaining stability. This compact design offers a high-performance, broadband solution for millimeter-wave receiver front ends [15, 16].

II. PROPOSED LOW-NOISE AMPLIFIER DESIGN

A common-source configuration is employed, using the NMOS transistor NM0, including characteristics, such as inductive source degeneration and resonant load matching. These elements contribute to ensuring high performance at elevated frequencies. The input signal is AC-coupled through the capacitor C1 and enters the gate of the MOSFET. At this point, the gate inductor L0 assists in input matching by resonating with the gate capacitance. The source inductor L1 is used to facilitate inductive degeneration, a process that enhances linearity, noise performance, and contributes to impedance matching. The drain of the MOSFET is connected to a resonant load formed by the inductors L2 and L3, as shown in Figure 1. This load is tuned to the desired operating frequency in order to present a high impedance, thereby maximizing voltage gain. The DC bias for the gate is provided through a separate bias network, known as VBIAS, ensuring that the transistor operates in the saturation region for optimal gain and NF. The amplified output is AC coupled through capacitor C0 with the objective of isolating the DC component prior to signal transmission to subsequent stages.

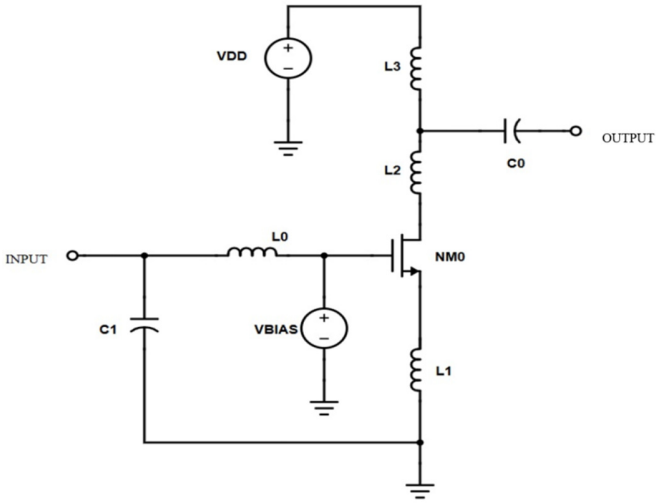

Fig. 1. Common source LNA.

The objective of this work is the design of a cascode configured LNA for RF front-end applications, using two NMOS transistors (NM11, NM12) in a stacked arrangement to enhance gain and suppress noise. The input stage of the circuit uses AC coupling through a gate side capacitor C8, supported by a bias stabilization setup that includes a series resistor R0 and a DC voltage feed V1, as displayed in Figure 2. In order to enhance linearity and stabilize gain, source degeneration is implemented using an inductor-resistor L9-R3 network at the lower transistor. The biasing for the upper NMOS transistor is achieved through the usage of a dedicated supply V3, which interfaces with an output matching circuit composed of high-Q passive elements, allowing for effective impedance conversion and minimized signal reflection. The high-frequency disturbances at bias nodes are decreased through the use of RF chokes, thereby maintaining a clean spectral profile. The extraction of amplified signals from the drain terminal of the upper transistor yields a symmetrical layout, thus ensuring gain consistency, power efficiency, and operational stability.

III. SMALL SIGNAL BEHAVIOR ANALYSIS OF THE PROPOSED LNA ARCHITECTURE

The Kirchhoff's Current Law (KCL) source node is the gate-to-source path through the c_{gs}, g_m current, and source inductor:

$$j\omega c_{gs}(v_g - v_s) + g_m(v_g - v_s) = \frac{v_s}{Z_{L9}} \quad (1)$$

with gate current:

$$i_g = j\omega c_{gs}(v_g - v_s) + \frac{v_g}{R_g} \quad (2)$$

It was observed that the signal gain:

$$\frac{v_d}{v_1} = \left(\frac{Zin(\omega)}{R_s + Zin(\omega)}\right)\left(\frac{-g_m R_L \frac{1}{Z_{L9}}}{g_m + j\omega c_{gs} + \frac{1}{Z_{L9}}}\right) \quad (3)$$

where $v_d = -g_m R_L\ v_{gs}$.

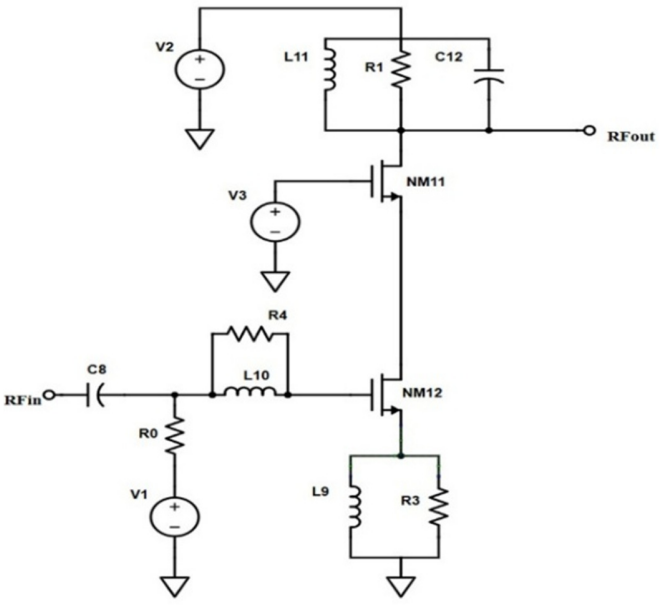

Fig. 2. Cascode LNA.

The input impedance $Z_{in}(\omega)$ of the circuit is determined by the inductive and capacitive elements at the input matching network, as depicted in Figure 3:

$$Z_{in}(\omega) = \omega_t L_9 + j\left[(L_9 + L_{10})\omega - \frac{1}{\omega(C_8 + C_e)}\right] \quad (4)$$

where $\omega_t = \frac{gm}{cgs}$ is the transit frequency, which can be written as the ratio of g_m to the $(C_8 + C_e)$, C_e is the CMOS (NM12) capacitance, g_m is the transconductance of the input transistor, c_{gs} is the gate source capacitance, and Ls and Lg are the source and gate inductances. The resonant frequency is:

$$\omega_0 = \frac{1}{\sqrt{(L_9 + L_{10})(C_8 + C_e)}} \quad (5)$$

Therefore, the quality factor Q_{in} of the overall circuit can be written as:

$$Q_{in} = \frac{1}{\omega_0\left((R_0 + R_s) + g_m\left(\frac{L_{10}}{C_8 + c_e}\right)\right)(c_8 + c_e)} = \frac{1}{2\omega_0(R_0 + R_s)(C_8 + C_e)} \quad (6)$$

The transconductance g_d and g_m of the circuit can be written as:

$$g_d = \frac{\mu_{eff} C_{ox}\left(\frac{W}{L}\right)\left[V_{ov} - mV_{ds} - \left(\frac{m}{2}\right)\left(\frac{\mu_{eff}}{2v_{sat}L}\right)V_{ds}^2\right]}{\left(1 + \frac{\mu_{eff} V_{ds}}{2v_{sat}L}\right)^2} \quad (7)$$

$$g_m = \frac{\mu_0 C_{ox} W v_{sat}(1 + \lambda V_{ds}[4mv_{sat}LV_{ov} + (2mv_{sat}L\theta + \mu_0 V_{ov}^2]}{(2mv_{sat}L + (2mv_{sat}L\theta + \mu_0)V_{ov})^2} \quad (8)$$

where $\mu_{eff} = \frac{\mu_0}{1 + \theta V_{ov}}$, W is the gate width of CMOS, L is the gate length of CMOS, μ_0 is the electron mobility, C_{ox} is the oxide capacitance, m is the body effect coefficient, V_{ds} is the drain to source voltage of CMOS, and v_{sat} is the saturation velocity. The output conductance, g_{d0} can be written as:

$$g_{d0} = \mu_{eff} C_{ox}\left(\frac{W}{L}\right) V_{ov} \quad (9)$$

The NF can be written as:

$$NF = 1 + \frac{\frac{1}{4}\gamma g_{d0} + g_m^2\left(\frac{C_{gs}}{C_{tot}}\right)^2\left(Q_{in}^2 + \frac{1}{4}\right)\left(\frac{\beta}{5g_{d0}}\right) + \frac{g_m C_{gs}}{C_{tot}}\sqrt{\frac{\gamma\beta}{20}} + \frac{1}{R_{out}}}{g_m^2 R_0 Q_{in}^2} \quad (10)$$

where $C_{tot} = (C_8 + C_e)$, γ is the white noise constant, β is the gate induced noise, and $R_0 = \frac{g_m}{C_{tot}} L_{10} - R_4$.

$$C_{gs} = \frac{2}{3} C_{ox} W \times L \quad (11)$$

The Output frequency can be determined as:

$$\omega_{out} = \frac{1}{L_{11} C_{10}} \quad (12)$$

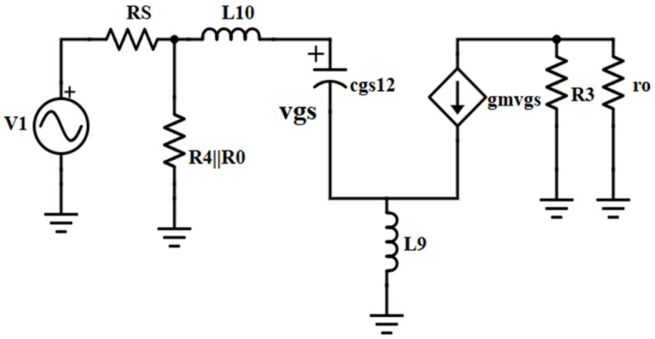

Fig. 3. Small signal equivalent model of a common source MOSFET amplifier with source degeneration.

IV. CHARACTERIZATION AND SIMULATION

A. S-Parameter

The S-parameter analysis of the proposed single-stage LNA offers key insights into its performance across the 1 to 5 GHz frequency range, as portrayed in Figure 4. The forward gain parameter S_{21} peaks at approximately 2.4 GHz with a magnitude of 28.5126 dB (M1), confirming optimal amplification near the design frequency. The input reflection coefficient S_{11} (red) exhibits a dip below –20 dB at this frequency, suggesting optimal input impedance matching and

minimal signal reflection. Concurrently, the output reflection coefficient S_{22} (pink) exhibits minimal values, thereby reinforcing stable output matching. The reverse isolation parameter S_{12} (blue) remains suppressed throughout the band, hence demonstrating effective signal containment and isolation between the input and output nodes.

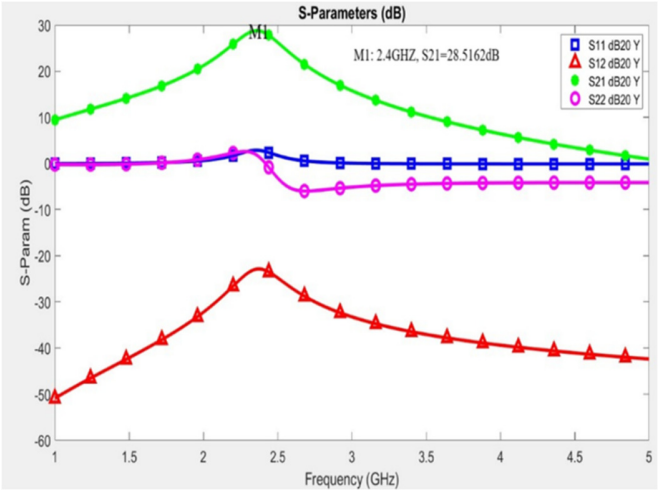

Fig. 4. S-parameter response of the LNA, showing a peak gain of 28.51 dB at 2.4 GHz with good input and output matching.

B. Harmonic Distortion

The harmonic balance response is a diagnostic tool that reveals the compression characteristics of the LNA, with a particular emphasis on the 1 dB input compression point (P1dB). As presented in Figure 5, the input-referred P1dB level is -18.5 dBm, indicating the maximum input power level at which the LNA maintains linear gain within a 1 dB deviation. The third-order input intercept point (IIP3) analysis of the LNA, shown in Figure 6, reveals its linearity performance under non-ideal signal conditions. As demonstrated in the harmonic compression plot, the IIP3 value attains a nadir of -17 dBm at a frequency of approximately 1.6 GHz, thus underscoring the amplifier's capacity to suppress intermodulation distortion at the intended operating frequency.

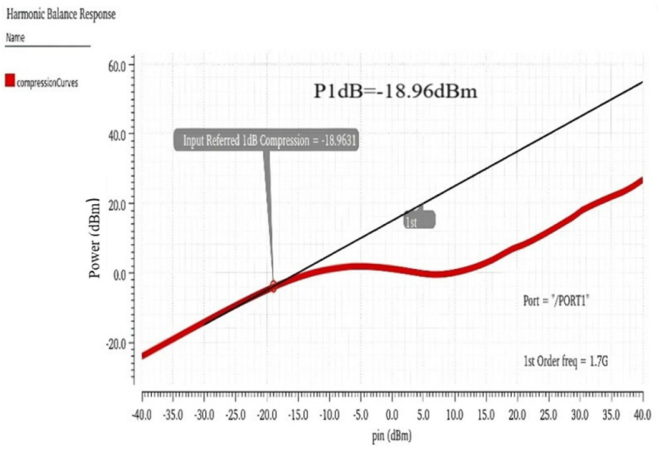

Fig. 5. Input referred 1dB compression.

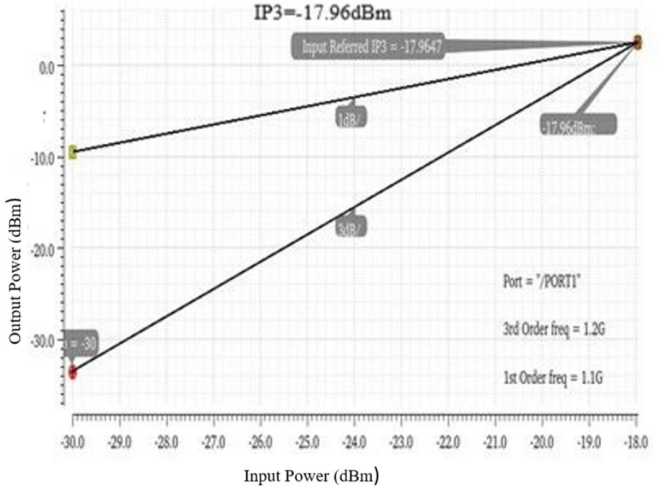

Fig. 6. Third order input intercept ioint calculated using input power versus output power with fundamental and third harmonics.

C. Power

The power spectrum response of the LNA is evaluated across a frequency span of 0 to 6 GHz in Figure 7, reflecting its energy distribution and output strength under harmonic balance conditions. The primary peak is indicative of the amplified input signal, while the additional peaks are the result of harmonics and intermodulation components generated by transistor nonlinearity and parasitic elements. The maximum recorded power density is approximately 15 dBm, suggesting considerable output capacity and robust frequency selectivity.

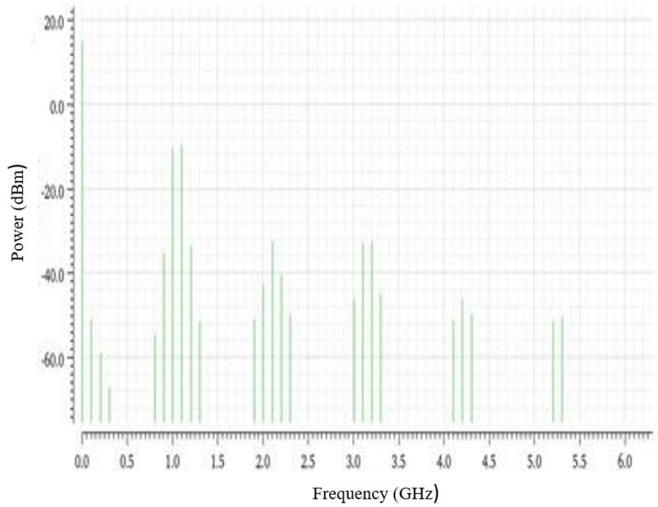

Fig. 7. The power spectrum response of the LNA is evaluated across a frequency.

D. Noise Figure

The frequency-dependent NF profile of the single-stage LNA determines its suppression characteristics across the 1 GHz–4 GHz spectrum. As illustrated in Figure 8, the simulation data exhibit a consistent decline from approximately 2 dB at 1 GHz to a minimum of approximately 0.66 dB around

2.5 GHz, followed by a notable increase exceeding 5 dB at 4 GHz.

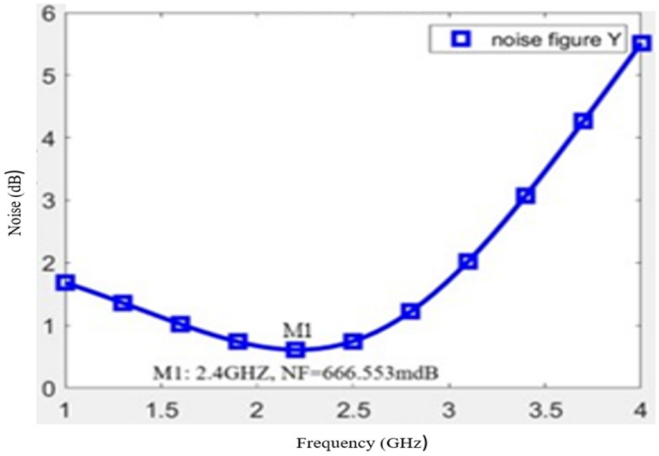

Fig. 8. NF of the proposed LNA, achieving a minimum value of 0.66 dB at 2.4 GHz, demonstrating low noise performance in the operating band.

E. Layout of LNA

The proposed LNA offers targeted amplification of weak reflections while maintaining low-noise operation, which is essential for accurate imaging. The final layout integrates a densely packed configuration of spiral inductors (L1–L4) and coupling capacitors (C1, C2), engineered to maximize EM efficiency while maintaining compact silicon usage, as seen in Figure 9.

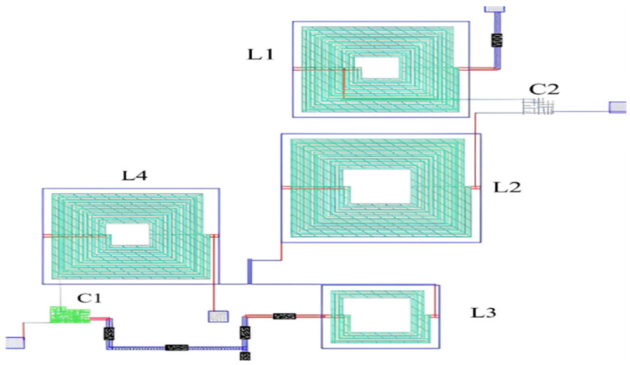

Fig. 9. Layout view of the LNA showing on-chip spiral inductors (L1–L4) and capacitors (C1–C2) used for impedance matching and resonance tuning in the designed circuit.

These passive elements are meticulously calibrated to establish resonance within the designated ultra-wideband spectrum, facilitating minimal insertion loss and sustained signal amplification. The addition of cascaded flipped-active inductive stages has been demonstrated to enhance high-frequency performance by reducing parasitic resistance and reinforcing inductive loading characteristics. The proposed LNA is manufactured using a 180-nm CMOS process, occupying an area-efficient footprint of 0.0685 mm², supporting high levels of integration for compact RF front-end systems.

V. CONCLUSIONS

The cascode common source Low-Noise Amplifier (LNA) with source degeneration was designed and validated using 180 nm CMOS technology and the Cadence Virtuoso environment. The circuit achieves superior Radio Frequency (RF) performance by using inductive source degeneration, cascoded gain boosting, and impedance matching. The simulations indicate an input return loss below -20 dB, a maximum gain of 28.5 dB, and a minimum Noise Figure (NF) of 0.666 dB across the UWB spectrum. The amplifier maintains acceptable linearity with a P1dB of –18 dBm and an IIP3 of –17 dBm. With a supply voltage of only 1.5 V, the design consumes 1.67 mW and requires a compact chip area of just 0.0685 mm², confirming its suitability for integration into portable GPR systems.

This study's main contribution is the combined use of cascode topology, inductive degeneration, and matching networks, which allows for the simultaneous optimization of gain, noise, and impedance matching in a compact CMOS architecture. The main results are: the realization of an ultra-low noise and high-gain LNA in 180 nm CMOS technology optimized specifically for UWB GPR applications and the development of a design methodology that balances gain, noise performance, linearity, and power efficiency. The demonstration of a compact, low-cost, energy-efficient solution directly addresses the stringent requirements of next-generation radar front ends. The proposed 180-nm CMOS LNA exhibits superior performance, offering a high gain of 28.5 dB and an ultra-low NF of 0.6 dB. These specifications surpass those of previously reported designs, including the ones based on more advanced technology nodes, as presented in Table I.

TABLE I. PERFORMANCE COMPARISON OF THE PROPOSED LNA WITH LITERATURE-BASED DESIGNS

Ref	Technology (nm)	Frequency (GHz)	Gain (dB)	NF (dB)	Supply voltage (V)	IIP3 (dBm)	P1dB (dBm)
[1]	65	8.6 - 13.6	19.98	1.94	1	N/A	-7.8
[2]	65	151 - 156	N/A	7.5	N/A	N/A	-32
[3]	65	19 - 45	15.8	3 - 5	N/A	N/A	N/A
[4]	40	51.6 - 73.7	22.4	3.78	1	N/A	-14.2
[5]	40	21.9 - 33.7	12.3	2.8 - 4.2	0.6	-0.2 to 3	-11 to -7
[6]	90	28	21.2 to 7.4	3.7 to 6.8	N/A	-9 to 4.5	-20 to -7
[7]	180	2.4	10	3	0.45	-11	N/A
[8]	180	0.05 - 10.8	10.6	2.24	N/A	-23	N/A
[9]	100	38	27	1.78	1	N/A	N/A
Proposed work	180	2.4	28.5	0.6	1.8	-17	-18

(N/A) Not Applicable

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