A Comparison of the SPWM Method and the Modified SVM Modulation Technique for the T-Type RB-IGBT PFCs for Vehicle-to-Grid Application

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ABSTRACT

The Vehicle-to-Grid (V2G) technology utilizes electric vehicle batteries to store surplus electricity and supply it back to the grid when necessary. The V2G is an effective and economical solution, as well as a strong research direction for power electronics laboratories. In the onboard charger system of electric vehicles, the Power Factor Corrections (PFCs) are a Multi-Level Inverter (MLI) and are primarily modulated using the Sinusoidal Pulse Width Modulation (SPWM) method. However, Space Vector Pulse Width Modulation (also known as Space Vector Modulation (SVM)) is a superior technique. However, implementing SVM for MLIs is challenging as the total number of levels increases. This study introduces a modified SVM method for PFC to enhance the output voltage quality and compares this modified technique with the SPWM. The experimental outcomes demonstrate the benefits of the proposed technique.

Keywords-SVPWM; SPWM; T-type RB-IGBT; PFC; V2G

I. INTRODUCTION

Power Factor Correction (PFC) is a power correction device used to improve the power factor and adjust the voltage and current waveforms in the charger. In the V2G technology, the PFCs are MLIs. Various MLIs have been introduced, including the Flying Capacitor (FC) [1, 2], Neutral Point Clamp (NPC) [3], and Cascaded H-Bridge (CHB) inverter [4-6]. Photovoltaic systems are compatible with CHBs [7]. However, one drawback of this kind of inverter is the need for numerous DC sources. Despite using only one DC supply, NPC and FC inverters have a large number of semiconductor valves and significant conduction losses [8]. Therefore, the introduced Type T inverter, which employs Reverse Blocking Insulated Gate Bipolar Transistors (RB-IGBTs), presents substantial advantages, such as a simplified structure requiring only one DC source, a reduced number of semiconductor switches, which contributes to lower conduction losses, and improved output waveform quality characterized by low Total Harmonic Distortion (THD) [9, 10]. A main challenge of the T-type RB-IGBT inverter lies in maintaining the voltage balance between the two DC-link capacitors. If unbalanced, it causes overvoltage on the semiconductor valves and a high THD of the output voltage. In MLI control, SPWM and SVPWM, also known as SVM, are commonly employed techniques, with SVM being regarded as the more advanced and efficient method. With a similar modulation index, SVM gives a lower THD of the output voltage than SPWM. Additionally, SVM is superior to SPWM when used in conjunction with the input DC source. SVM also uses switching states to reduce the switching frequency and THD [11-18]. However, conventional SVM entails intricate mathematical operations to identify the sector of the reference voltage vector and compute the corresponding switching durations. The implementation of SVM is particularly challenging for higher-level inverters due to the large number of redundant commutation states and auxiliary triangles [19]. These computational demands necessitate complex hardware architectures and expensive microcontroller units.

In response to these limitations, the current study presents the design of a three-phase, three-level T-type inverter incorporating RB-IGBTs and an optimized SVM technique. This modified modulation technique has a switching sequence

that is directly compared to a 5 kHz triangular pulse. Therefore, it is simple to implement on a Texas Instruments F28379D DSP card [20]. The experiments on TI's DSP processor (TMS320F28335), along with the Xilinx Spartan-6 chip used in [19], demonstrated the advantages of the proposed technique. At the same time, it helps reduce the cost and complexity of the control circuit compared to utilizing the d-SPACE RTI 1103 system, as shown in [13].

II. THREE-LEVEL T-TYPE RB-IGBT INVERTER

The circuit topology of the proposed three-level T-type inverter employing RB-IGBTs is illustrated in Figure 1. The input DC-link voltage is split by two series-connected capacitors, thereby establishing three levels of phase voltage and 5 levels of line voltage. Valves Sx1 and Sx2 must block all DC supply voltage, while valves Sx2 and Sx3 must only block half.

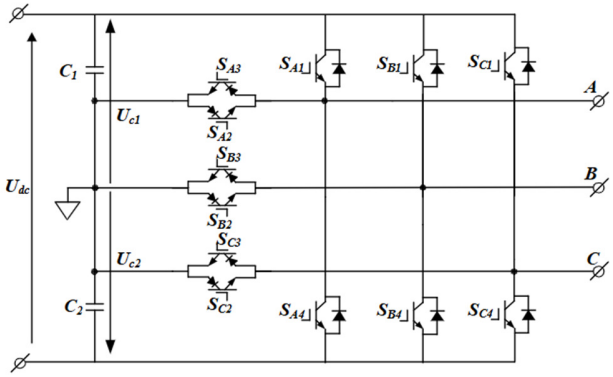

Fig. 1. Three-level T-type RB-IGBT converter.

By properly activating the T-type RB-IGBT inverter ON and OFF, three output phase voltage levels will be created: $V_{DC}/2$ (P), 0 (O), and $-V_{DC}/2$ (N). Voltage levels P, O, and N are obtained at the output by closing and cutting off two semiconductor valves simultaneously. Table I describes the semiconductor valves for the desired phase A output voltage.

TABLE I. SWITCHING STATUS FOR PHASE A

Status	V_{out}	S_{A1}	S_{A2}	S_{A3}	S_{A4}
P	$\frac{V_{DC}}{2}$	ON	OFF	ON	OFF
O	0	OFF	OFF	ON	ON
N	$-\frac{V_{DC}}{2}$	OFF	ON	OFF	ON

III. SPACE VECTOR MODULATION METHOD FOR A THREE-LEVEL INVERTER

The switching scheme of the three-phase, three-level inverter comprises 27 possible switching states, which correspond to 19 distinct voltage vectors, as depicted in Figure 2. This set includes zero vectors (*V0*), small vectors (*V1→V6*) classified as P-type and N-type, medium vectors (*V7→V12*), and large vectors (*V13→V18*). As portrayed in Figure 2, the space vector diagram is partitioned into six sectors (I-VI), each further partitioned into four triangular sub-regions (from Δ1 to Δ4) associated with their respective switching states.

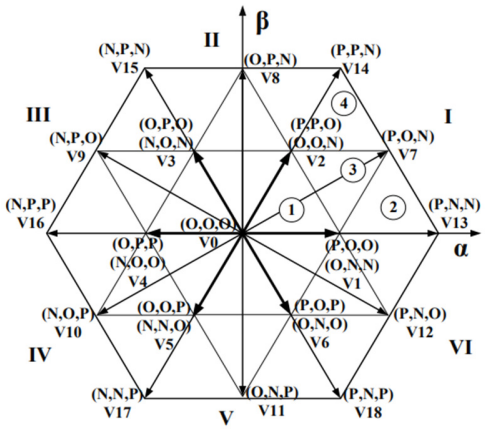

Fig. 2. Three-level T-type RB-IGBT inverter space vector diagram.

A. ABC to αβ Transformation

For the three-phase voltage, we have:

$$\begin{cases} v_A = V_m \sin \omega t \\ v_B = V_m \sin(\omega t - 2\pi/3) \\ v_C = V_m \sin(\omega t + 2\pi/3) \end{cases} \quad (1)$$

According to [21], using the Clarke transformation to (1):

$$\begin{cases} v_\alpha = v_A \\ v_\beta = \frac{1}{\sqrt{3}}(v_B - v_C) \end{cases} \quad (2)$$

From (2) to the equation of resultant voltage phasor:

$$V_{ref} = v_\alpha + j v_\beta \quad (3)$$

B. 0◦ αβ to 60◦ Transformation

Figure 3 illustrates that three coordinate systems represent the vector space (Z_{1x}, Z_{1y}), (Z_{2x}, Z_{2y}), and (Z_{3x}, Z_{3y}) with:

$$\begin{cases} Z_{1x} = v_\alpha - v_\beta/\sqrt{3} \\ Z_{1y} = 2.\frac{v_\beta}{\sqrt{3}} \end{cases}$$

$$\begin{cases} Z_{2x} = v_\alpha + v_\beta/\sqrt{3} \\ Z_{2y} = -v_\alpha + v_\beta/\sqrt{3} \end{cases} \quad (4)$$

$$\begin{cases} Z_{3x} = 2.v_\beta/\sqrt{3} \\ Z_{3y} = -v_\alpha - v_\beta/\sqrt{3} \end{cases}$$

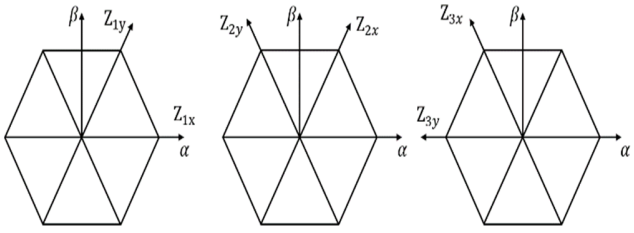

Fig. 3. 0◦ αβ to 60◦ transformation.

C. Determination of Sector Location

The sector location can be determined according to Table II.

TABLE II. SECTOR LOCATION TABLE

$Z_{1x}.Z_{1y}>0$		$Z_{1x}.Z_{1y}<0$			
$Z_{1x}>0$	$Z_{1x}<0$	$Z_{2x}.Z_{2y}>0$		$Z_{2x}.Z_{2y}<0$	
		$Z_{2x}>0$	$Z_{2x}<0$	$Z_{3x}>0$	$Z_{3x}<0$
I	IV	II	V	III	VI

D. Determination of Sub-Triangle Position

To identify the position of the triangle within a given sector, two coefficients, m_1 and m_2, are first computed, representing the projection ratios of the output voltage vector onto the two vectors that define the sector (Figure 4):

$$m_1 = \frac{V_{Zix}}{|V_j|}, m_2 = \frac{V_{Ziy}}{|V_j|} \ (i=1\text{-}3, \ |V_j| = \frac{V_{dc}}{3})$$

In sector I, $\vec{V}_{ref}$ lies the sub-triangle following:

- If $m_1 < 1, m_2 < 1, m_1 + m_2 < 1$, then $\vec{V}_{ref}$ is in $\Delta 1$.
- If $1 \le m_1 \le 2, 1 < m_1 + m_2 \le 2$, then $\vec{V}_{ref}$ is in $\Delta 2$.
- If $m_1 \le 1, m_2 \le 1, m_1 + m_2 \ge 1$, then $\vec{V}_{ref}$ is in $\Delta 3$.
- If $1 \le m_2 \le 2, 1 < m_1 + m_2 \le 2$, then $\vec{V}_{ref}$ is in $\Delta 4$.

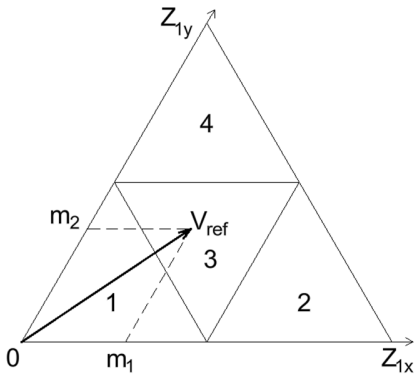

Fig. 4. Locate the triangle in sector I.

E. Dwell Time Calculation

The three nearest vectors (Nearest Vector Modulation (NVM)) were combined to create $\vec{V}_{ref}$. For instance, $\vec{V}_{ref}$ is situated in triangle 3 of the sector I (Figure 4), and $\vec{V}_2, \vec{V}_1, \vec{V}_7$ are three nearest vectors $\vec{V}_{ref}$ (Figure 5).

$$\begin{cases} T_S.\vec{V}_{ref} = T_1.\vec{V}_2 + T_2.\vec{V}_1 + T_3.\vec{V}_7 \\ T_S = T_1 + T_2 + T_3 \end{cases} \quad (5)$$

$$\vec{V}_{ref} = \frac{T_1}{T_S}.\vec{V}_2 + \frac{T_2}{T_S}.\vec{V}_1 + \frac{T_3}{T_S}.\vec{V}_7 \quad (6)$$

$$\vec{V}_{ref} = d_1.\vec{V}_2 + d_2.\vec{V}_1 + d_3.\vec{V}_7 \quad (7)$$

where d_1, d_2, d_3 are the dwell times of the corresponding vectors, respectively.

$$\vec{V}_{ref} = (1-m_1)\vec{V}_2 + (1-m_2)\vec{V}_1 + (m_1+m_2-1)\vec{V}_7 (8)$$

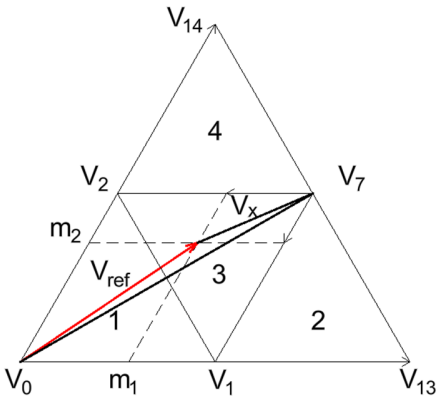

Fig. 5. Dwell time calculation for $\vec{V}_2, \vec{V}_1, \vec{V}_7$.

F. DC Capacitor Voltage Equalization Algorithm

For T-type RB-IGBT inverters, maintaining DC capacitor voltage balance represents a significant challenge. This balance can be achieved by exploiting the redundant switching states within space vector modulation. Notably, only the small vector switching states influence the voltage distribution across the two capacitors. The P-type state discharges the capacitor C_1, while the N-type state discharges the capacitor C_2. Figure 6 shows the DC capacitor voltage balancing algorithm based on the small vectors.

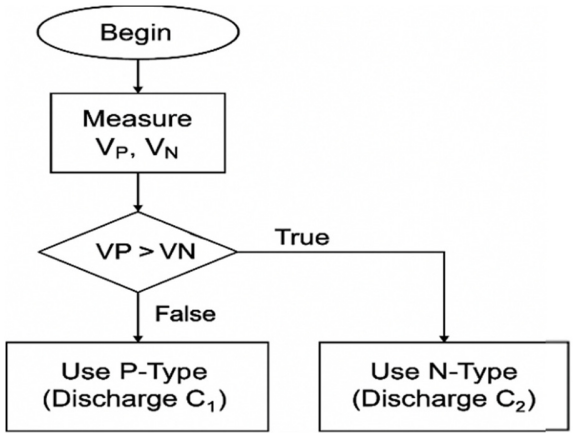

Fig. 6. DC capacitor voltage equalization algorithm.

G. Commutation Sequence and Activation Duration Calculation

The two-branch modulation technique switching sequence requires only two valves to change states throughout each modulation cycle. The main advantage of this technique is its ability to enhance the performance of the DC capacitor voltage

balancing algorithm, albeit at the expense of increased voltage THD. This sequence uses one of the two states of the small vectors according to the principle, and the states are represented in Table III (specifically for triangle 3 in sector I).

- If m=1 ($V_P > V_N$), P-type switching states are utilized.
- If m=0 ($V_P < V_N$), N-type switching states are used.

This switching sequence creates regular pulses:

- Pulse supply to switches S_{x1} will be located on the sides ($S_{x3} = \overline{S_{x1}}$).
- Pulse supply to switches S_{x2} will be located in the middle ($S_{x4} = \overline{S_{x2}}$).

TABLE III. COMMUTATION SEQUENCE FOR TRIANGLE 3, SECTOR I

m	Commutation state
m=0	PON - OON - ONN - ONN - OON - PON
m=1	PPO - POO - PON - PON - POO - PPO

The activation durations are computed in Table IV according to the following rule:

- Switches S_{x1}: d_{sx1} > triangular pulse.
- Switches S_{x2}: d_{sx2} < triangular pulse.

TABLE IV. SWITCHING ON TIME FOR SWITCHING SEQUENCE, TRIANGLE 3, SECTOR I

m	Switching on-time	
m=1	$d_{SA1} = 1$	$d_{SA2} = 1$
	$d_{SB1} = d_1$	$d_{SB2} = 1$
	$d_{SC1} = 0$	$d_{SC2} = d_1 + d_2$
m=0	$d_{SA1} = d_3$	$d_{SA2} = 1$
	$d_{SB1} = 0$	$d_{SB2} = d_1 + d_3$
	$d_{SC1} = 0$	$d_{SC2} = 0$

From Figures 7 and 8, a table of switching-on times for the valves was obtained according to the two-branch modulation technique.

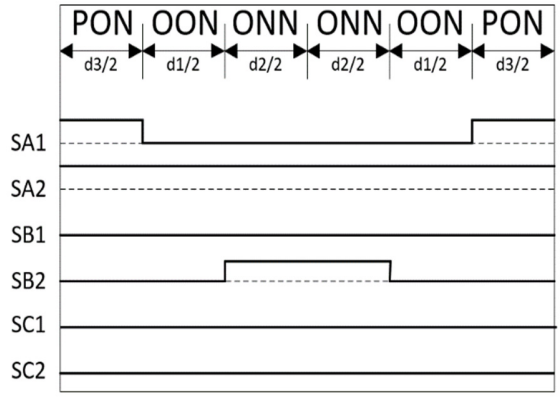

Fig. 7. The pulses for triangle 3, sector I, *m*=0.

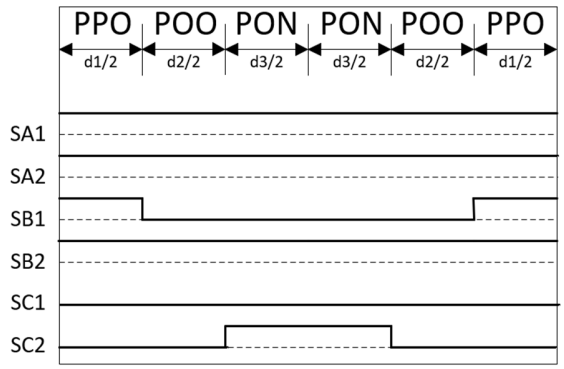

Fig. 8. The pulse for triangle 3, sector I, and *m*=1.

IV. EXPERIMENTAL RESULTS

The SVM technique was implemented in real-time using an F28379D card and a HIL Typhoon 402 system. The HIL Typhoon Control Center created the T-type inverter power circuit using RB-IGBT valves, together with the LC filter and R load. The control algorithm was implemented using the Code Composer Studio (Figure 9).

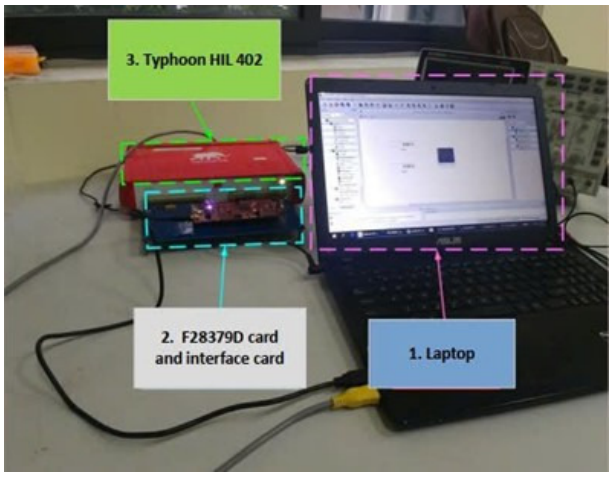

Fig. 9. The experimental setup.

The parameters and operating conditions used for the proposed modulation techniques were compared. Specifically, the results about the output voltage, DC capacitor voltage, and THD will be presented. The experimental coefficients are summarized in Table V.

TABLE V. EXPERIMENTAL PARAMETERS

Parameter	Description	Value
V_{DC}	DC voltage	700 V
C	DC capacitance	950 µF
L_f	Filter inductance	1.5 mH
C_f	Filter capacitance	21 µF
R_{load}	Load resistance	9.7 Ω
f_s	Switching frequency	5 kHz
T_s	Sampling time	0.2 ms

Figures 10 and 11 illustrate the phase-to-phase voltage and the resulting phase voltage for a pair of modulation methods.

Each phase-to-phase voltage exhibits five levels, indicating the proper functioning of the control algorithm.

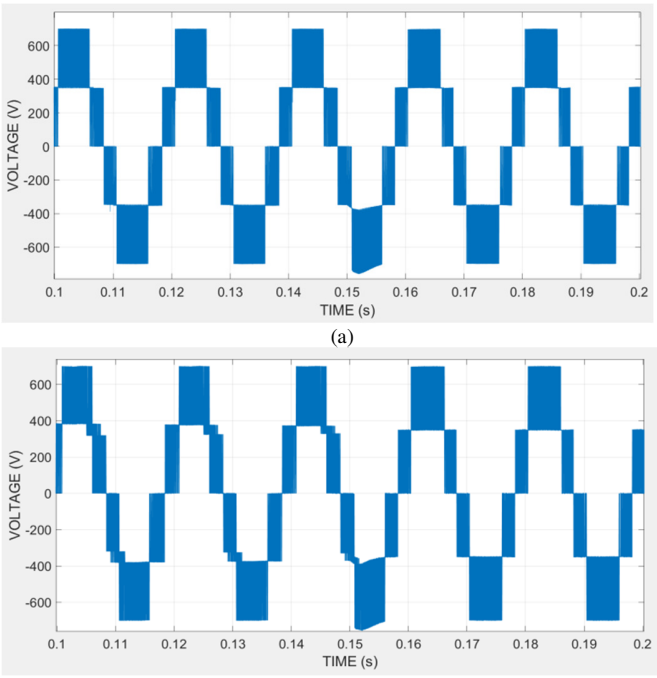

Fig. 10. The phase to phase output voltage: (a) SPWM, (b) two-branch SVM.

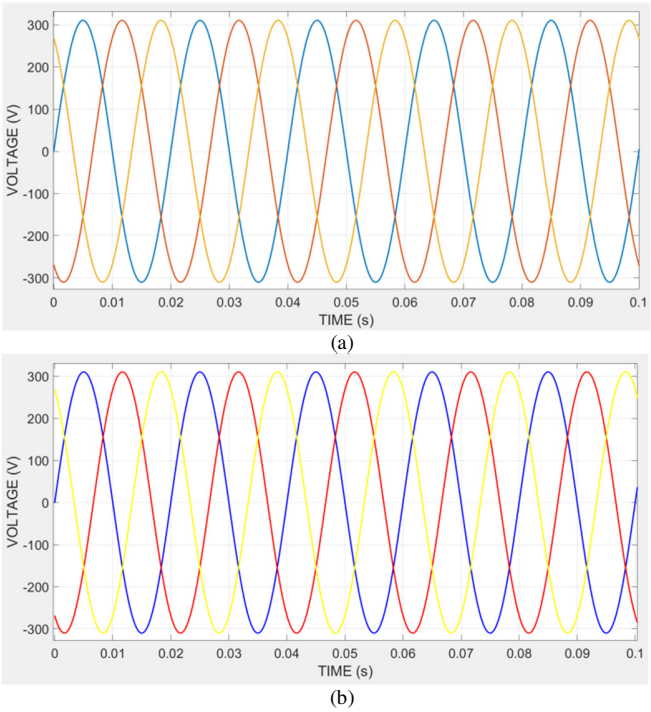

Fig. 11. The output phase voltage: (a) SPWM, (b) two-branch SVM.

Figure 12 presents the DC capacitor voltages for the two modulation methods. Using P-type or N-type states in the case of m=1 or m=0, respectively, the two-branch SVM technique allows for better DC capacitor voltage balancing (maximum difference of about 9V). The SPWM method exhibits the difficulty of the DC capacitors in voltage balancing.

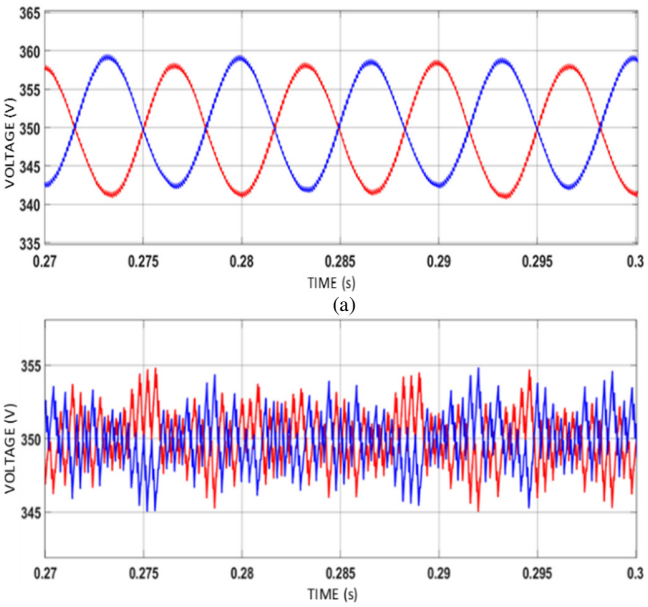

Fig. 12. The DC capacitors voltage: (a) SPWM, (b) two-branch SVM.

Figure 13 displays the output phase voltage THD of SPWM and two-branch SVM. The two-branch SVM technique achieves superior output voltage quality, with a THD of 2.12%.

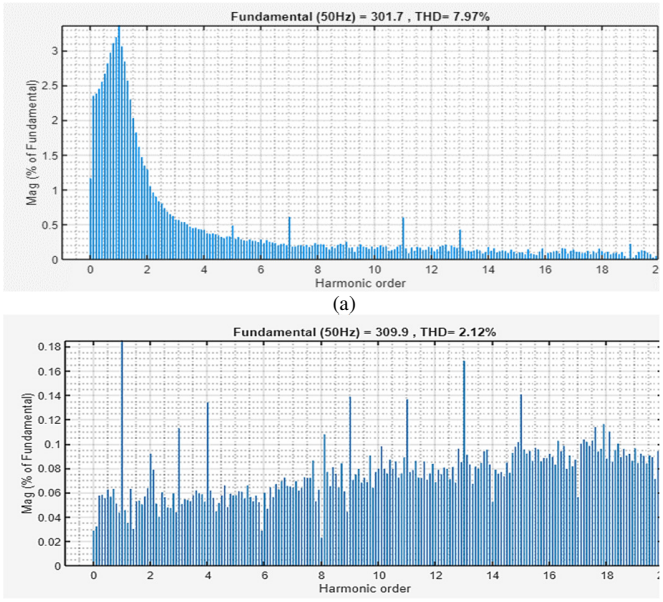

Fig. 13. The output voltage THD of modulation methods: (a) SPWM, (b) two-branch SVM.

V. CONCLUSIONS

This study introduces a modified Space Vector Modulation (SVM) method for a T-type Reverse Blocking Insulated Gate Bipolar Transistors (RB-IGBT) Power Factor Correction (PFC) implemented in Vehicle-to-Grid (V2G) applications, offering better DC capacitor voltage balancing and improved quality of output voltage. The proposed two-branch SVM technique demonstrates enhanced system performance when compared to the conventional Sinusoidal Pulse Width Modulation (SPWM) method. The experimental validation using a Texas Instruments F28379D DSP card not only confirmed the theory's correctness but also offered a cost-effective and less complex control circuit design. The results confirm that the two-branch SVM technique successfully achieved excellent DC capacitor voltage balancing, with a maximum difference of approximately 9V(≈ 1.2%), which is lower than the 19V(≈ 2.71%)of SPWM. In addition, the proposed method simultaneously enhanced the output voltage quality by reducing the Total Harmonic Distortion (THD) to about 2.12% (< 5% according to the IEEE 519-2014 standard), from that of 7.97% of SPWM.

ACKNOWLEDGEMENTS

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