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Design of High-speed Data Transmission System Based on Fiber-PCIE

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Abstract: In this paper, a high-speed data transmission system based on optical fiber and PCIE is proposed. The system is implemented on the platform of Xilinx's FPGA. The Transceiver IP core in the FPGA is used to design the GTX high-speed interface, and the optical module with high-speed data transmission communication performance is selected for data transmission, and then the data is stored in DDR3. On the software side, PCIE communication logic is configured through embedded (SDK) development and exemplified XDMA IP core to achieve dynamic speed allocation, data receiving and sending, and data transmission. The reconfigurable technology of FPGA is used to configure different transmission rates of optical fiber communication by switching QPLL and CPLL during system operation, which increases the flexibility of the system. The physical test shows that the proposed system is effective in data transmission, has high data accuracy, and the transmission rate can be switched at any time.

Keywords: FPGA, PCIe, Optical fiber, DDR3, Dynamic pace.

1. Introduction

High-speed data transmission is widely used in satellite communication system[1] telemetry system[2], unmanned aerial vehicle (UAV) system[3] and other fields.The high-speed data transmission system needs to transmit the collected data to users for control and monitoring.Due to different use scenarios, the data transmission rate requirements are also different, some as high as several Gbps, which requires the diversity of different data transmission rates.At present, the main high-speed data transmission methods used are optical fiber, PCIE, USB, Ethernet, etc[4][5][6][7]. The optical fiber communication design implemented by Yang Chunling and others corresponds to the effective data rate of 1.6Gb/s on the optical fiber communication link[8].Literature [9] uses the LVDS transceiver built in FPGA to receive LVDS data[8].And write it to the USB3.0 control transmission chip through DDR3 cache to complete the high-speed data transmission from the LVDS interface to the USB3.0 interface. The actual transmission rate remains at 250MB/s.Document [10] proposes a high-speed data transmission system based on Ethernet, with data transmission rate of 91.21Mb/s[10].Document [11] is a design of high-speed data acquisition and transmission circuit for the on-board measurement and control system[11]. The system can collect data stably and for a long time, and can realize high-speed transmission of 3.6Gbit/s.Cai Weijie and others have designed a high-speed data transmission system using daughter and daughter cards, with a transmission rate of 10 Gbps[12].However, the high-speed data transmission system studied in literature [8-11] has a relatively low data transmission rate, and literature [9] uses USB3.0 for data transmission, which is less stable than PCIE bus interface; Although the speed of the system studied in document [12] can reach 10Gbps, it adopts the mode of daughter and mother card, which is relatively complex in design and high in cost.

Optical fiber communication has the advantages of fast transmission speed, high bandwidth, low cost and low delay[13].It is very suitable for high-speed data transmission; PCIE bus adopts point-to-point serial connection mode and uses high-speed differential signal line to transmit data[14]

2. Hardware Design

2.1. System Scheme Design

In this paper, XC7K325T-2FGG900 of Xilinx Company is selected as the main control chip of FPGA. This chip integrates GTX high-speed interface and can support rich peripheral interface, logic configuration and other functions. The high-speed data transmission system is composed of DDR3 memory module, power module, clock module and flash configuration. The system structure diagram is shown in Figure 1.In this system, XC7K325T-2FGG900 is the control core of the system, which is used to control the GTX high-speed interface to complete the enabling control of optical transceiver module, optical transmission link management and data transmission; When the data is received by the four-way optical fiber, it is written to the DDR3 storage module for data caching, and then transmitted through PCIE. Similarly, reverse data transmission can also be realized.

2.1.1. Power Module Design

The power supply voltage of each part of the system is inconsistent. It requires+3.3V,+2.5V,+1.8V,+1.5V,+1.0V and other voltages to supply power for DDR3, FPGA and other components. In this paper, the power step-down chip is used to convert the voltage required by each module. The designed power structure topology is shown in Figure 2.

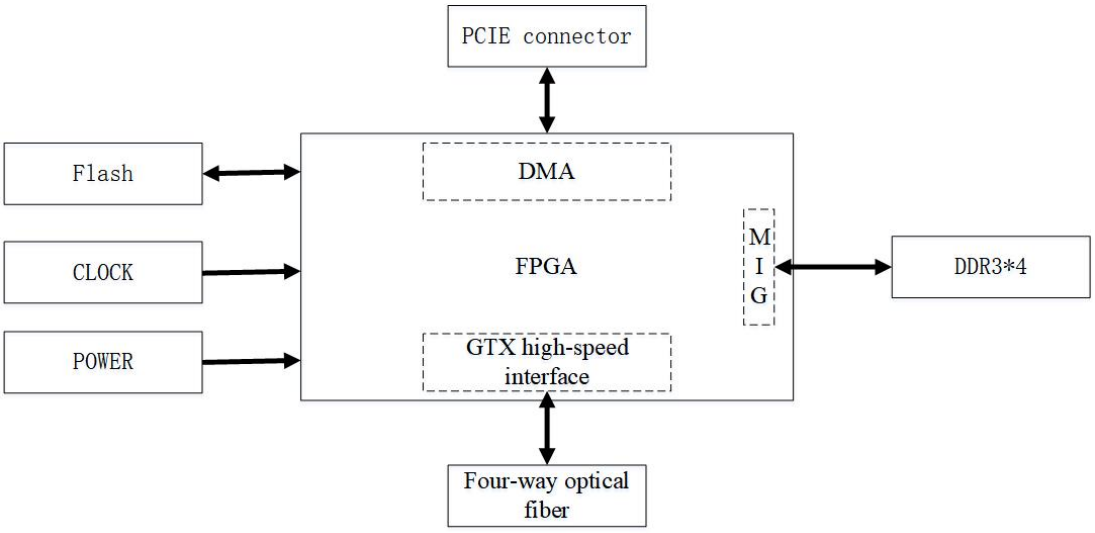

Figure 1. System architecture block diagram

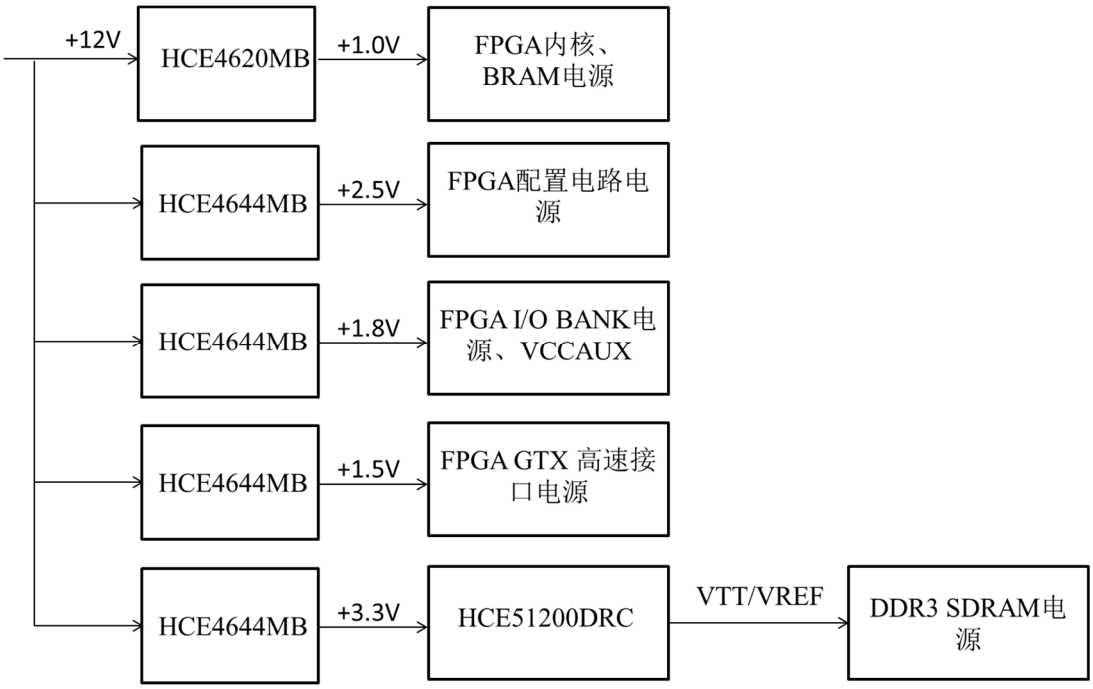

Figure 2. Power supply design

2.1.2. Power Module Design

Since the master chip has its own 100M and 125M crystal oscillators, the clock generated by the crystal oscillator can be used to provide the FPGA with 100M and 125M working clocks. The 125M differential clock becomes the global differential clock after passing the clock buffer, providing the clock for the optical fiber module.

2.1.3. DDR3 storage Module Design

The DDR3 memory granule chip adopted by the system is the MT41J256M16HA-125 product of Micron Company. The bit width of this memory granule data is 16 bits, and the single chip storage capacity is 4G bit. In order to meet the demand of high transmission bandwidth, the bit expansion method is adopted to expand the data bits of four 16-bit DDR3 granules to 64 bits, and the total memory capacity after expansion is 16G bit, meeting the system data transmission requirements.Through the data bus dq [63:0] of four DDR3 memory particles in parallel, data gating signal lines dqs [7:0], dqs_n [7:0], data shielded signal line dm [7:0], realizing bus expansion. The address bus and other control signals are the common signal lines of four DDR3 particles. Therefore, the bus mode is used to realize synchronous control of four DDR3 particles. The DDR3 circuit is shown in Figure 3.

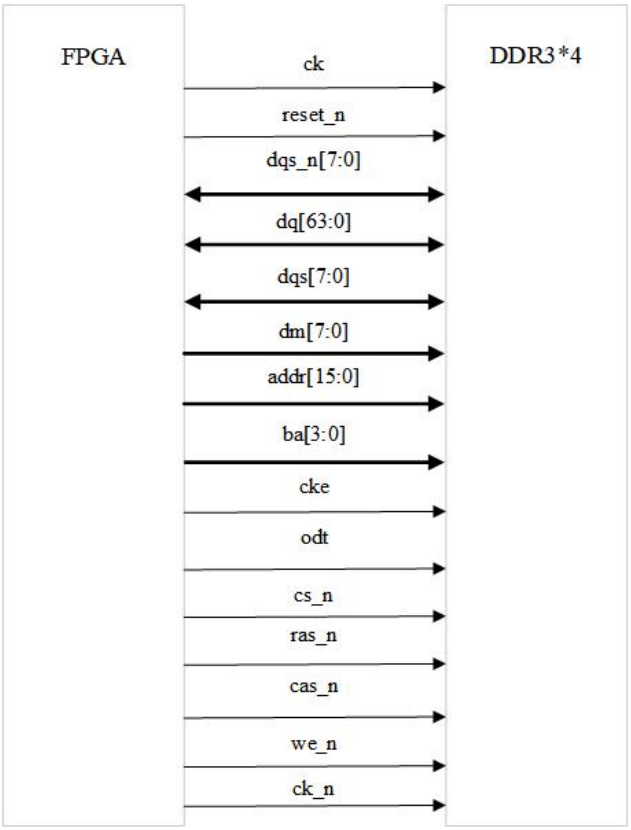

Figure 3. DDR3 circuit

2.1.4. Flash Configuration Circuit Design

Because FPGA adopts SRAM technology, data will be lost after power failure, all programs and data cannot be saved after power failure, and the next restart cannot operate normally [15]. Aiming at the above problems, this paper designs a flash configuration circuit to solidify the program. When the FPGA is powered on again, it will directly read the solidified code from the configuration chip and run it, and the power-on self-start time can be configured, which solves the problem that the whole system cannot work offline. The flash chip model used in this design is N25Q, and the storage capacity is up to 256Mb, which fully meets the design requirements. The Flash configuration circuit is shown in Figure 4.

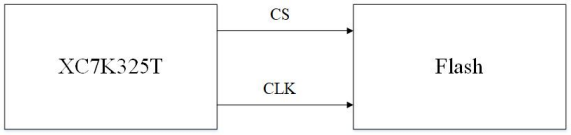

Figure 4. Flash configuration circuit

2.1.5. Design of GTX High-Speed Interface Module

The Xilinx7 series XC7K325T chip used in this design is internally integrated with GTX serial transceiver, and the maximum line speed supports 12.5Gbps. The single-bit data line and differential circuit design can effectively suppress the negative factors in the high-speed signal transmission process.The design adopts Aurora 64B/66B protocol. Compared with the traditional 8B/10B coding mode, its transmission rate is higher, up to 10.3125Gbps.The user data interface uses the AXI4 — Stream interface. The AXI4 — Stream interface does not need to consider address mapping when transmitting high-speed data streams, and allows unlimited data burst transmission. The entire GTX high-speed interface initializes the channel through global logic, drives the GTX serial transceiver through the instantiation of the channel logic, processes the decoding and encoding of the data stream, and performs error checking.

3. Software Design

The software design is to complete the generation of data and the communication logic configuration of PCIE and transmit the data and control signals to the hardware end. The software design mainly includes two functions: one is to configure the communication rate, the other is to send and receive data. The functions of these two parts will be introduced respectively.Two or more .

3.1. Communication Rate Configuration

For the configuration of communication rate, this design uses embedded (SDK) for development.The initial rate is determined by the bit stream at system startup. When modification is required, dynamic configuration is mainly performed by modifying the address in the system. In order to read the bitstream file in the system, you need to delete the header of the bitstream file and save it as a binary file.This process can be realized through the TCL command of Vivado.

Then the bitstreams representing different communication rates are stored in the file system. The software reads the bitstream information as required and downloads the configuration information to the hardware terminal. The communication rate reconstruction software block diagram is shown in Figure 5.

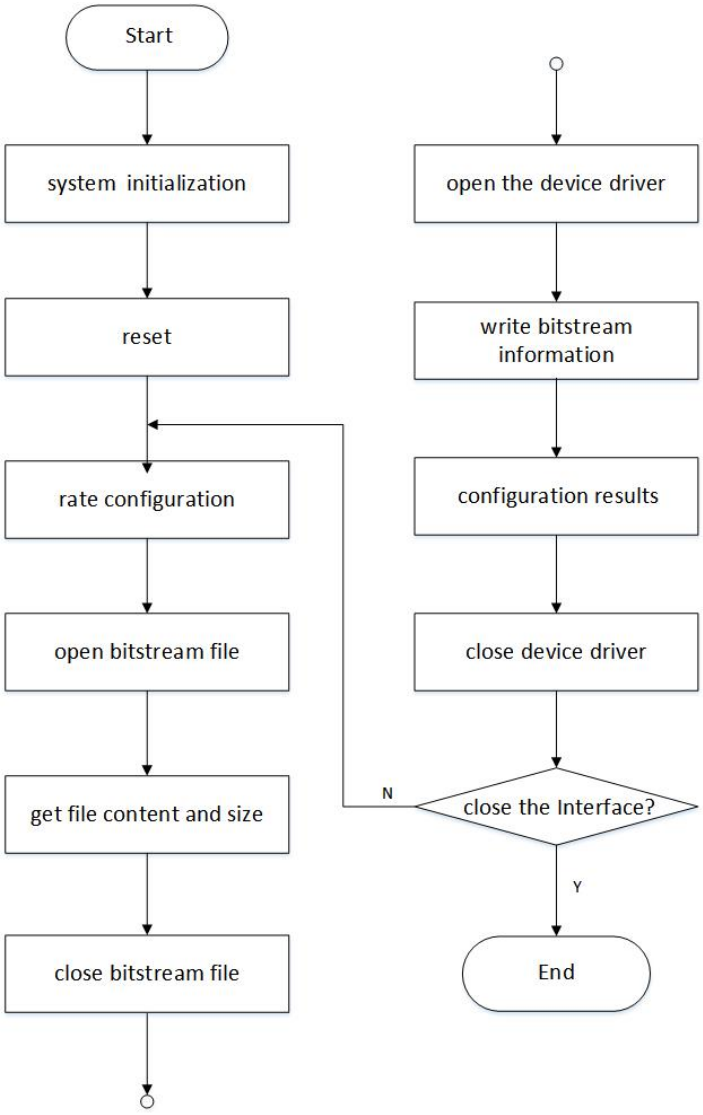

Figure 5. Flow chart of communication rate configuration

When the software is running, the system first performs initialization operation. The user selects to enter the optical fiber communication rate configuration interface. In the software interface, users can write different addresses to configure different rates, such as 10Gbps, 8Gbps, 6.25Gbps, and then click the OK button. The configuration of each rate address of cpll is shown in Table 1. The configuration of each rate address of qpll is shown in Table 2.

Table 1. cpll rate configuration

地址 / 速率	8’hAC(700)	8’h5E(704)	8’h88(708)	8’hA9(70C)
1	16’h0003	16’h0003	16’h0022	16’h1010
2	16’h0003	16’h0003	16’h0011	16’h1020
2.4	16’h0003	16’h1001	16’h0011	16’h1020
3	16’h0003	16’h1081	16’h0011	16’h1020
4	16’h0003	16’h1003	16’h0011	16’h1020
4.8	16’h0003	16’h1001	16’h0000	16’h1040
5	16’h0003	16’h0083	16’h0000	16’h1040

Table 2. Qpll rate configuration

地址 / 速率	8'hAC(700)	8'hA9(70c)	8'h88(708)	8'h32(724)	8'h33(728)	8'h36(72C)	8'h37(730)
8	16'h000b	16'h1040	16'h0000	16'h01c1	16'h8068	16'h0080	16'h0040
10	16'h000b	16'h1040	16'h0000	16'h0181	16'h0068	16'h0170	16'h0040

3.2. Data Transmission and Reception

Data is generated through SDK development at the software end. The flow chart of data reading and writing is shown in Figure 6. After the system initialization is completed, after the software end receives the interrupt signal from the hardware end, the software end starts to send data to the hardware end, and converts the data into AXI-Stream data through the AXI-Connect interface, and sends it to the hardware end. Until the software end detects the write completion signal from the hardware end, the software end closes the write interrupt. When the software end receives the read enable signal from the hardware end, the software end begins to read the data. When the software end detects the read completion signal from the hardware end, it ends the receiving and sending of data until the next drive signal arrives.

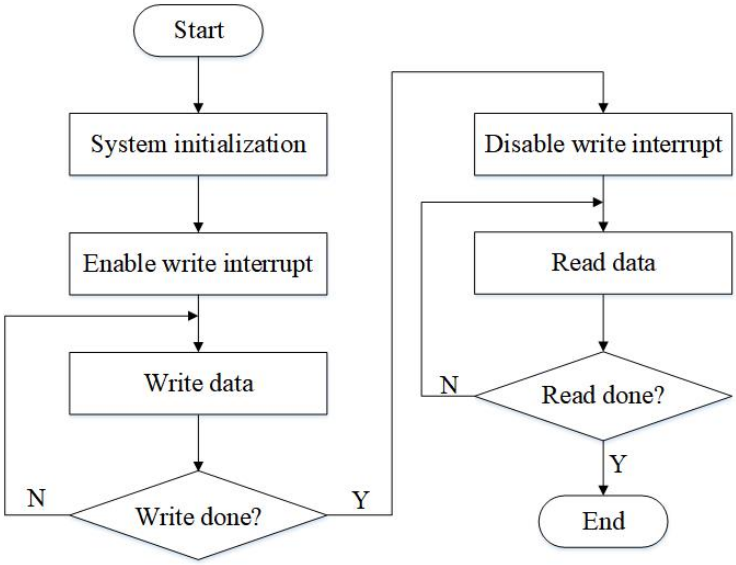

Figure 6. Data reading and writing flow chart

4. Test Results and Analysis

The physical objects used in this test are shown in Figure 7. Because the data bit width of this design is up to 512 bits, in order to facilitate the change and observation of data, 16 32-bit data are spliced when writing data, so as to achieve the data width of 512 bits. Only the lower 32 bits need to be captured when capturing waveform. After completing the system design, a data loopback test platform from the upper computer to the optical fiber is built for data communication test. The waveform of the transmitted data is captured by the ila online logic analyzer of Vivado to check whether the received and transmitted data are correct. Sending data is shown in Figure 8. The received data is shown in Figure 9.

Figure 7. Physical test platform

Figure 8. Write data

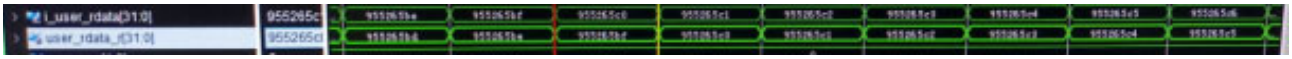

Figure 9. Read data

From the results captured by ila online logic analyzer, it can be seen that the data sent is consistent with the data received. It can also be seen that in the process of multiple data transmission, the data transmission is stable and reliable, without data loss or error, and the data transmission speed is fast.

5. Conclusion

This research is designed and implemented based on the FPGA chip xc7k32tffg900-2 of Xilinx company and the DDR3 storage particle MT41J256M16HA-125 of Micron company. The FPGA side is designed and implemented using Verilog language, and the software side PCIe driver and library functions are designed and implemented using C language. The test verifies that the transmission rate can be switched at will, with a minimum rate of 1Gbps and a maximum rate of 10Gbps. When carrying out high-speed data transmission, the transmission rate has more selectivity, which increases the flexibility of the system.

References

[1] L.K.Ma: Design of high-speed data transmission terminal platform for satellite ground station, Telecommunication Engineering, vol. 60 (2020), 1420-1424.

[2] H.Zhao, K.Song, K.Li, C.Wu and Z.Chen, "A High-Speed Well Logging Telemetry System Based on Low-Power FPGA," in IEEE Access, vol. 9 (2021), p. 8178-8191.

[3] Z.M.Zhao, Y.L. Pei, G.H. Liang, et al. Design and Implementation of Small Marine Magnetic Data Acquisition System Based on Multi-rotor UAV, Ocean Technology, vol. 40 (2021), 43-50.

[4] Afsal S. et al., A novel approach for the enhancement of Fiber optic communication using EDFA, International Conference on Wireless Communications, Signal Processing and Networking (Yangzhou, Jiangsu, China, October 13-15, 2016) , p. 23-27.

[5] G.Y.Zhen, H.S. Su, J.J. Chen, et al. Design and Implementation of Data Transmission of PCIe Interface Based on FPGA, Foreign Electronic Measurement Technology, vol. 40 (2021).

[6] X.M.Wang, Y.Z. Lu, L.F. Meng, et al. Design of Ultra High Speed Data Transmission System Based on FPGA and USB 3.0, Modern Electronic Technology, vol. 45 (2022), p. 71-74.

[7] G.P.Lu, H.Q. Wang,B. Li, et al. Design of a high-speed data transmission system based on STM32 Ethernet, vol. 40 (2021), p. 58-62.

[8] C.L.Yang, L.Zuo. Design of general optical fiber communication system based on FPGA, Application of Electronic Technique, vol. 46 (2020), p. 110-113.

[9] J.M.Li, Z.W.Zheng. Design of high-speed data transmission interface based on LVDS and USB3.0, vol. 44 (2021), p. 1-6.

[10] Y.T.Wang, Z.C.Xue, F.Wen. Design of Ethernet high-speed data transmission system based on W5300. International Electronic Elements | Int Electr Elem, vol. 29 (2021), p. 49-52+59.

[11] B.Z.Li, J.Li, C.J.Hu, et al. Design of high-speed data acquisition and transmission circuit for on-board measurement and control system, Journal of North University of China(Natural Science Edition), vol. 41 (2020), p.571-576.

[12] W.J.Cai, Y.Wu, P.Zou, et al. Design and Implementation of Optical Fiber Communication Board Based on FPGA and PXIE Bus, Electronic Measurement Technology, vol. 44 (2021), p. 1-6.

[13] X.M.Yuan, L.T.Xu. Design of high-speed optical fiber communication baseband board based on FPGA, Electronic Engineering & Product World, vol. 25 (2018), p. 58-61.

[14] Y.L.Zhou, X.Z.Luo, Z.Li , et al. Design of high-speed ADC acquisition system based on PCIe interface, Journal of Hubei University(Natural Science), vol. (2022), p. 1-6.

[15] C.X.Zhou, G.Q.Zeng. Design of high-speed data transmission interface based on USB 3.0, Computer Measurement and Control, vol. 28 (2020), p. 146-150.