

Design of Multi-circuit Motor Control System based on Fabric Defect Detection Device

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Abstract: In order to realize the motion control of multiple motors of the fabric defect detection device, a ZYNQ-based multiple motor control system is designed in conjunction with the fabric defect detection device. In this system, pulse width modulation technique is used to control the multi-channel motors. The flexible logic operability of FPGA is utilized to achieve real-time high-speed control of multi-channel pins, where FPGA is responsible for data caching and acquisition control, and ARM is responsible for data communication and transmission. The logic array was programmed and simulated in Vivado software. Simulation results show that the system is able to control multiple motors synchronously and stably, verifying the effectiveness and feasibility of the system.

Keywords: Fabric Defect Detection Device; Multiplex Motor Control; PWM; VIVADO; Control System.

1. Introduction

Defect detection device is a more complex mechatronics equipment in textile machinery products, where the motor drive mechanism as an important part of the detection device, its performance greatly affects the detection efficiency of the device and fabric yield. The traditional control system mostly uses PC plus microcontroller or multiple microcontroller control method, with the continuous improvement of the structure of the detection device and detection speed requirements, the amount of data and tasks handled by the system are greatly increased, when the traditional control system is difficult to achieve real-time transmission and parallel processing. The industry has improved the performance and real-time processing speed of the control system to handle complex data by combining various different high-performance processors with the lower computer, such as the ARM and microcontroller based electrochemical analyzer designed by Paulraj Santharaman et al[1]-[5], where ARM is used as the central control to realize the control system design through parallel bus and rich peripheral interfaces, E.B. Kapisch et al. designed ARM and FPGA based power system recorder[6]-[10], using field programmable gate array (FPGA) and ARM platform and other devices to process EPS signals in an intelligent way, the above different systems have the advantages of parallel control, scalability and computing performance over the control system, but this architecture requires complex underlying hardware, and the data between ARM and microcontroller, CPLD, FPGA CPLD, FPGA data transfer between the slow, unstable, not suitable for motor control such as real-time demanding scenarios.

ZYNQ is the first product that closely combines high-performance ARM Cortex-A9 series processor and FPGA (Field Programmable Logic Gate Array) within the chip, which reduces the difficulty of hardware development, by shortening the communication distance and realizing high-bandwidth and low-latency bus communication between ARM and FPGA on-chip [11]-[14]. Therefore, this paper designs a ZYNQ-based motor control system to achieve high-speed, real-time, parallel motor control, using the high-

performance PS (i.e., processing system) part to flexibly allocate the on-chip resources of the high-speed parallel PL (i.e., FPGA) part of ZYNQ to control the linear control of the motor through the PL, simulating and verifying the system function through simulation software, and finally, based on Xilinx's Xilinx XC7Z010-based development board for functional verification of the system solution.

2. System Hardware Circuit Design

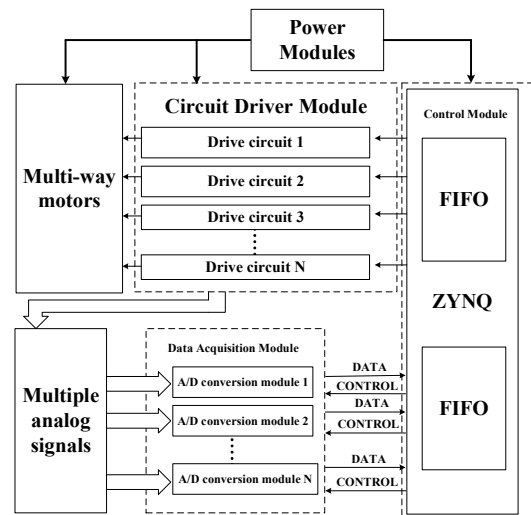


Figure 1. System block diagram

The control system consists of multiplex motors, motor drive modules, data acquisition modules, control modules, etc. The processing system (PS) side of ZYNQ and the programmable logic (PL) side together form the control mode, with the Cortex-A9 as the processor on the PS side and the field programmable gate array (FPGA) logic unit and digital signal processing (DSP) resources on the PL side. The FPGA uses a 50MHz system clock source for internal processing and external communication, first sending control commands via the host computer, which are transferred to the FPGA's RAM via USART serial communication and stored at the set address while parsing the corresponding data, and then sent to the

FIFO loop queue to generate multiple PWM signals for driving when the conditions are met. At the same time, the sampling data obtained in the data acquisition module is compared with the reference current, and the deviation value is calculated through the PID control algorithm to output multiple PWM signals with different duty cycles [15].

According to the overall design requirements of the motor control system, the control chip is Xilinx's ZYNQ series XC7Z010-1CLG400C chip as the FPGA master chip, using its rich IO ports and the host computer and external circuitry to form a complete hardware structure, the ADC chip is TI's TLC1543 type chip, which is a 12-bit sampling The ADC chip is TI's TLC1543 chip, which is a 12-bit sampling accuracy and has 11 analog input channels of analog-to-digital converter, and the data output of TLC1543 follows the serial peripheral interface SPI protocol, through which the conversion process from analog power to digital signal is realized on the FPGA[16]. The overall block diagram of the system is shown in Figure 1.

2.1. System Power Design

The FPGA is powered by +5V, which is converted into +3.3V, +1.5V, +1.8V, +1.0V by the quad DC/DC power chip TLV62130RGT, with each output current up to 3A. 1.5V VTT and VREF voltages required for DDR3 are generated via TI's TPS51200.

2.2. Current Sampling Design

In order to improve the control accuracy of motor control system, the capacitive A/D analog-to-digital converter TLC1543 is used for multi-channel current sampling [17]. The chip has an internal 14-channel multiplexer, which can select one of the 11 analog input channels or 3 internal self-test voltages for testing according to the demand, and its working process is divided into 2 cycles. I/O CLOCK receives a 10-clock-length clock sequence from the FPGA, and when CS is high, I/O CLOCK and ADDRESS are in the forbidden state.

3. FPGA Implementation

FPGA is the key of the whole motor control system, responsible for the reception of communication data, data caching, data cyclic output, motor drive control circuit, etc. Its internal system structure is mainly divided into three parts: serial communication module, FIFO module [18], state machine control, Figure 2 is the internal structure framework diagram of FPGA. The common transmission mode usually uses the FIFO directly as a cache module, and sends the data given by the upper computer directly into the corresponding registers for first-in-first-out data transfer to complete the subsequent control, which can reduce the data transmission time, but there will be some inconvenience for the subsequent optimization of the whole system and data recovery calculation, so in the design of this system, after receiving the data from the upper computer, it will be stored in RAM first This design can avoid the processor is performing other tasks and not read the data in time, to be received after the next frame of data will overwrite the previous frame of data, resulting in communication abnormalities, for this problem designed a pre-storage buffer plus FIFO cyclic queue of data cache module, both convenient for the data cache module with pre-stored buffer and FIFO is designed to facilitate the monitoring of data in the transmission process and to optimize the system.

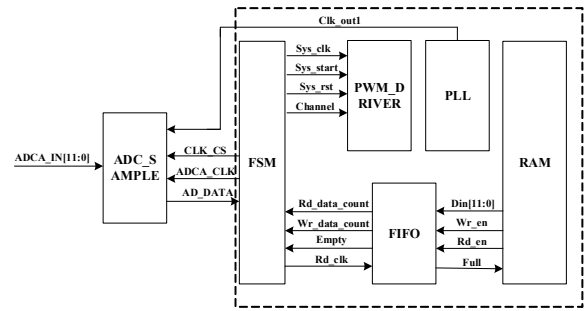


Figure 2. FPGA internal structure block diagram

3.1. FPGA Receiver Module Design

In this system, the FPGA mainly communicates with the host computer through the serial port, and the serial receiver module is used as the receiver of the main control command of the whole system to receive the parameter data sent from the host computer. To ensure the same communication protocol, the same baud rate, i.e., 115200bps, is set for the transmitter and receiver of USART communication [19], and 1-bit start, 8-bit data and stop bits are used as the format of transmitted data. To ensure the accuracy and continuity of timing control, a data reception state machine is designed as shown in Figure 3, which changes from STATE_IDLE to STATE_STOP sequentially, and the whole process corresponds to a complete data reception.

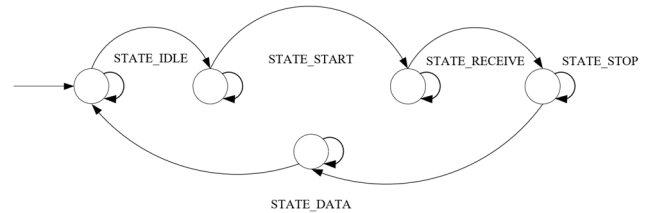


Figure 3. Serial Receiver Status Machine

After the system is powered on, it first enters the "STATE_IDLE" state, which is the idle state, and when the falling edge of the signal, i.e., the first bit of the start bit is low, it is counted into the "STATE_START" state, and waits for one bit of the start bit time. After the end of the data reception state "STATE_RECEIVE", the data is sampled at the midpoint of the baud rate counter time. After waiting for 8 bits of data to be received, the reception is completed and the state "STATE_STOP" is entered, where a half-bit waiting time is set to avoid missing the next data start bit judgment. state, which sends the received data to the data cache module.

4. System Workflow

After the system is powered on, the ARM is first initialized and the PL part of the FPGA is configured with the drive port initialized. The host computer transmits the control data to the data cache module of FPGA through USART communication, and then configures the PWM signal for multiple motor drive. During the motor operation, the current sampling is performed using the sampling circuit, and the error between the actual circuit current and the reference current is compared separately to reconfigure the PWM signal by calculating the compensation value through the PID controller, finally realizing the stable control of multiple motors.

5. System Simulation Results

In order to verify whether the multiplexed motor control

system achieves the expected results, high-speed simulation of each functional module is performed in Vivado's built-in Simulation. First, we verify whether the FIFO can correctly determine the empty/full status of the internal data storage by setting the read/write clock period of 10ns and setting the data depth to 8, and verify by reading/writing data to the FIFO Whether the empty/full flag bit is valid. The simulation results are shown in Figure 4.

The motor control system mainly relies on the drive circuit to drive the motor, through multiple pairs of complementary PWM signals to control voltage changes, so the drive simulation of the multi-way full-bridge circuit, set the clock period of 10ns, generate multiple complementary PWM signals, through the control parameters used in the control system to change the duty cycle of PWM. The simulation results are shown in Figure 5.

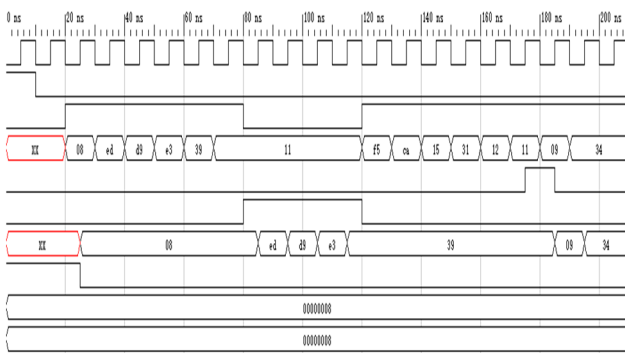


Figure 4. Circular Queue FIFO Simulation Results

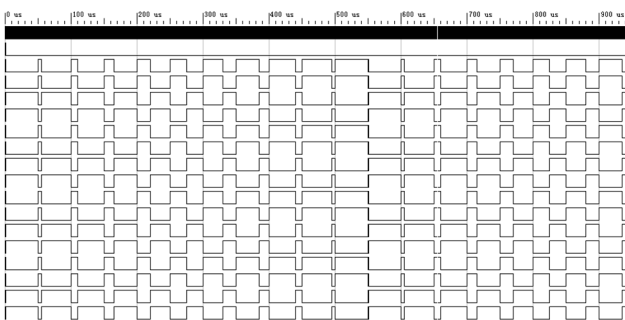


Figure 5. Multiplexed signal drive simulation results

6. Conclusion

This paper designs a motor control system based on ZYNQ development board as the core, for multiplex motor control, the system hardware structure, FPGA internal structure, software development and simulation, and the FIFO cache module according to the system needs. The simulation results show that the motor control system has the characteristics of low power consumption, fast response and easy control, and has some practical production value.

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