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Research on the Suppression of Secondary Power Ripple in Single-Phase Pulse Rectifier Based on Improved Deadbeat-Repetitive Control

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Abstract: In order to solve the problems of increasing the conduction loss of power devices and decreasing the conversion efficiency caused by the secondary power ripple of the single-phase pulse rectifier of high-speed trains, a buck chopper active power decoupling loop is proposed to replace the LC filter loop, which absorbs the secondary pulsation power by increasing the pulsation of the energy storage capacitor and reduces the capacity of the energy storage capacitor to improve the power density of the system. It integrates and improved deadbeat-repetitive control without difference, improves the inherent cycle delay problem of repeated control, realizes the tracking of the second harmonic current without difference, and improves the dynamic performance of the system. Through the MATLAB/Simulink simulation platform, a simulation model of Buck chopper active power decoupling of single-phase pulse rectifier is established, and the harmonic content and load mutation response time are compared and analyzed, and the simulation results prove the correctness and feasibility of the theoretical analysis.

Keywords: Single-phase Pulse Rectifier; Secondary Power Ripple; Active Power Decoupling; Improved Deadbeat-Repetitive Control.

1. Introduction

As a grid-side converter in the traction power supply link of trains, the single-phase pulse rectifier has the advantages of increasing the transmission power and improving the power factor, but there is a natural secondary pulsation on the grid side of the rectifier, which causes the power mismatch between the grid side and the DC side, which leads to the secondary power ripple of the DC bus voltage [1-3]. The power ripple on the DC side will increase the current stress of the rectifier power device, increase the conduction loss, which will affect the power quality of the traction power supply system, and even cause resonance accidents and equipment damage [4-10].

In order to reduce the secondary power ripple on the DC side, the traditional method is to connect a large-capacity electrolytic capacitor in parallel in the DC link to obtain the effect of buffering the ripple power, but this method has the disadvantages of large device size, short service life, and reducing the power density of the system. To this end, some scholars have proposed the use of active power decoupling technology [11-17], that is, actively controlling power semiconductor devices to replace electrolytic capacitors with film capacitors with longer life to compensate for secondary power ripples. However, the method has low control accuracy and requires large-capacity energy storage capacitors, and the Buck/Boost decoupling circuit is complex, so it is not suitable for high-power and low-switching frequency scenarios of high-speed trains. Ref. [19] uses proportional integral control to improve system accuracy, but its limited two-fold gain makes it difficult for the decoupled inductor current to track the second harmonic current reference. In Ref. [20], a dual-objective cost function is constructed by using dual-objective predictive control, which can simultaneously realize the tracking of the decoupling inductor current and the precise control of the decoupling capacitance. This method relies on sampling the input current on the DC side, which requires the current Hall or current transformer to be embedded and decoupled circuit, it is not conducive to the modularization of the system. In Ref. [21], the Buck chopper active power decoupling and repetitive control is adopted, and the Buck topology is used as a device with fewer applications, which effectively prevents the resonance problem with the original circuit, so it is more suitable for use in the high-speed train traction system. However, the high gain of repeated control of a specific frequency is obtained by the cycle delay, so the poor dynamic response is an inevitable defect of repeated control.

In order to improve the dynamic performance of the decoupling circuit and suppress the power ripple on the DC side, this paper proposes a control method for the active power decoupling circuit of Buck chopper based on the improved deadbeat-repetition control, which combines the improved undifferentiated beat algorithm with repetitive control, and uses the undifferentiated beat algorithm to improve the dynamic performance of the system, so that the system can track the secondary pulsation power with high precision and quickly respond to the change of harmonic signal, and verify the feasibility of the control strategy by combining simulation.

2. Buck Chopper Active Power Decoupling Topology and Working Principle

The topology of the single-phase pulse rectifier and Buck chopper active power decoupling topology circuit is shown in Figure 1, which is composed of the rectifier part, the decoupling part and the DC link, the rectifier part is a single-phase full-bridge inverter, which realizes the AC-DC conversion and is transmitted to the post-stage decoupling circuit, and the Buck chopper active power decoupling circuit realizes the purpose of power decoupling through the

secondary pulsation component in the energy storage capacitor absorption current, and continues to transmit to the subsequent DC link, which is composed of capacitive resistance and plays the role of buffering the steady voltage.

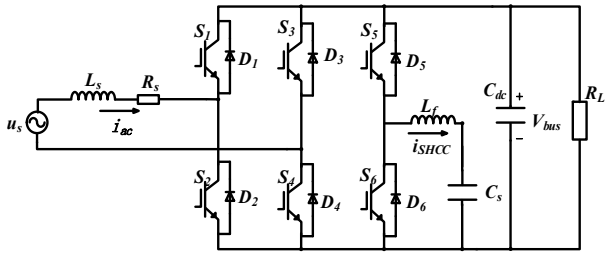


Fig 1. buck chopper active power decoupling topology

In a single-phase pulse rectifier, the grid-side port voltage and current can be expressed as:

$$u_{\mathrm{ac}} = \sqrt{2}V_{\mathrm{ac}} \sin \omega t \tag{1}$$

$$i_{\mathrm{ac}} = \sqrt{2}I_{\mathrm{ac}} \sin(\omega t - \theta) \tag{2}$$

where V_{ac} and I_{ac} are the effective values of port voltage and current; ω is the angular frequency and θ is the phase difference between u_{ac} and i_{ac}. The instantaneous power of this AC port is:

$$P_{\mathrm{ac}} = V_{\mathrm{ac}}I_{\mathrm{ac}} \cos\theta - V_{\mathrm{ac}}I_{\mathrm{ac}} \cos(2\omega t - \theta) \tag{3}$$

If the converter efficiency is 100%, the DC bus output current can be expressed as

$$I_{dc} = i'_{\mathrm{dc}} + i_{SHC} \tag{4}$$

$$i'_{\mathrm{dc}} = \frac{V_{ac}I_{ac}}{V_{bus}} cos\theta \tag{5}$$

$$i_{SHC} = -\frac{V_{ac}I_{ac}}{V_{bus}} \cos(2\omega\, t - \theta) \tag{6}$$

In the formula, $I_{dc}$is the DC current output of the converter, $i'_{dc}$is the output DC component, and i_{SHC} is the second harmonic. In order to compensate for the i_{SHC} at the output end of the converter, the V_{bus} is the bus capacitor voltage, and the input current of the decoupling circuit i_{SHCC} is equal to i_{SHC}. The following figure shows the main waveform diagram when the active power decoupling circuit is working, in which the voltage ripple of the decoupling circuit port is small, which can be regarded as a constant, Therefore, the average value of the voltage of the intermediate DC bus V_{bus}.

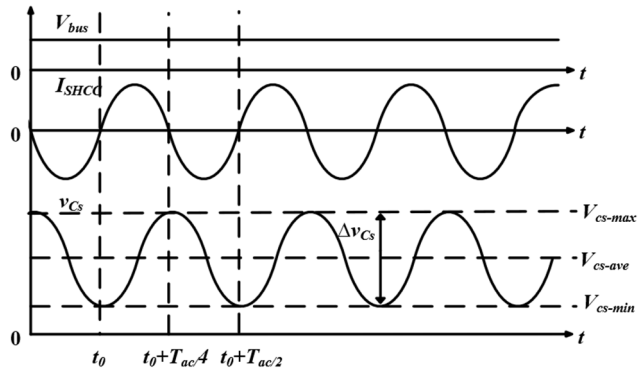


Fig 2. Buck chopper decoupling circuit operating waveform

As can be seen from Figure 2, during the $[t_0,t_0+T_{ac}/4]$ period, the input current i_{SHCC} is greater than zero, the storage capacitor voltage V_{CS} increases, and the active decoupling circuit works in charging mode, During the $[t_0+T_{ac}/4,t0+T_{ac}/2]$ period, the input current i_{SHCC} is less than zero, the voltage of the energy storage capacitor is V_{Cs} reduced, and the active decoupling circuit works in discharge mode.

Since the operating waveform is approximately sinusoidal, only one quarter period needs to be analyzed, and the energy ΔE_{Cs} absorbed by the storage capacitor is in the case of $i_{SHCC}>0$.

$$\Delta E_{Cs} = \int_{t_0}^{t_0+\frac{T_{ac}}{4}} V_{bus} i_{SHCC} dt = \frac{S}{\omega_{ac}} \tag{7}$$

From equation (7), the T_ac is the alternating voltage period; S is the apparent power of the rectifier, which can also be expressed as follows according to the relationship between the capacitor energy storage and its voltage Δ E_Cs which can also be expressed as:

$$\Delta E_{Cs} = \frac{1}{2}C_s V_{Cs-max}^2 - \frac{1}{2}C_s V_{Cs-min}^2 = C_s V_{Cs-\mathrm{ave}} \Delta V_{Cs} \tag{8}$$

In equation (8), $V_{Cs\text{-}max}$and $V_{Cs\text{-}min}$are the maximum and minimum values of the energy storage capacitor voltage, respectively, where $V_{Cs\text{-}ave}$ is the average value of the energy storage capacitor voltage, and ΔV_{Cs} is the energy storage capacitor voltage ripple. equation (7) and equation (8) can be obtained:

$$C_s = \frac{S}{\omega_{ac}} \cdot \frac{1}{V_{Cs_a v} \Delta V_{Cs}} \tag{9}$$

From equation (9), it can be seen that the capacity of the energy storage capacitor C_s can be reduced by increasing the pulsation Δ of the energy storage capacitor voltage V_Cs compared with passive LC filtering, the active power decoupling circuit can reduce the bus capacitance capacity, and the energy storage capacitor in the decoupling circuit can choose a film capacitor with a long life, so as to achieve the design purpose of improving the power density and prolonging the service life of the converter.

3. Basic Repetitive Control Principle

As can be seen from the previous section, power decoupling can be achieved by tracking the second harmonic current on the DC side and controlling the energy storage capacitor pulsation. The repetitive control method is a typical application of the internal mode principle, by introducing a periodic delay in the forward channel and constructing positive feedback, and introducing a resonant peak at the input signal fundamental and its frequency doubling, it can achieve efficient suppression of any integer harmonic, so the use of repetitive control can make the decoupling circuit effectively track the second harmonic, the structure of traditional repetitive control, This is shown in Figure 3.

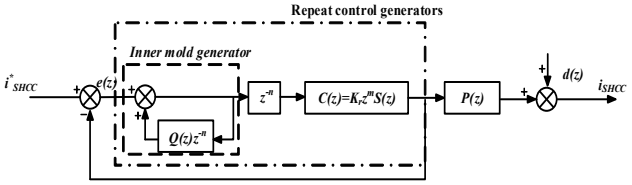


Fig 3. Traditional repetitive control block diagrams

In Figure (3), i^*_{SHCC} is the pulsating current reference input, the error signal is e(z), and d(z) is the disturbance signal, and the recursive function from i^*_{SHCC} to i_{SHCC} is:

$$G_1(z) = \frac{G_{RC}(z)P(z)}{1+G_{RC}(z)P(z)} \tag{10}$$

where G_{RC} (z) is the transfer function of the repeating controller, which can be obtained from the structure diagram:

$$G_{RC}(z) = \frac{z^{-N}}{1-Qz^{-N}} KrZ^m S(z) \tag{11}$$

P(z) is the controlled object, Q(z) is usually a constant or low-pass filter slightly less than 1 in the delay link, N is the number of sampling points in a single cycle of complex control, T is the fundamental period of the reference signal, T_s is the sampling period of the discrete system, Kr is the compensation gain, the selection of Kr affects the stability of the system, the second-order low-pass filter S(z) is added to compensate the control object and the system fluctuation, and z^m is the linear phase advance compensation link.

However, when the frequency changes, due to the existence of the delay link z^{-N}, the system generates a cyclic delay, and cannot respond quickly and accurately track the signal.

4. Improved Deadbeat-Repetitive Control Strategy

In the operation of high-speed trains, the system working environment is complex, the input frequency of the rectifier is changeable, the delay link of repeated control will cause frequency deviation due to input fluctuations, and the compensation gain of the controller will be reduced at the resonant frequency, resulting in the repetitive controller can not respond quickly, but may interfere with the normal operation of the system. deadbeat-predictive control can realize the tracking of a given value, and its algorithm is simple and the dynamic response speed is fast, so the beat-free prediction is proposed to compensate for the delay caused by repeated control.

When the decoupling circuit is working, the voltage of the capacitor C_s as the decoupling capacitor is U_{cs}. When U_{cs} is constant, it is assumed that C_s absorbs all of the two-fold power, i.e.:

$$\frac{1}{2}C_s\frac{d(u_{cs}(t))^2}{dt} = -\Delta E_{cs}cos(2\omega t) \tag{12}$$

Then the capacitor voltage can be solved:

$$u_{cs}(t) = \sqrt{\frac{\Delta E_{CS}}{C_{cs}\omega}[m - sin\,(2\omega t)]} \tag{13}$$

From the above equation, the capacitance value is inversely proportional to the capacitance voltage, where m is the integration constant, because the buck chopper active power decoupling will work in the chopper circuit mode, so the bridge arm voltage does not exceed the DC bus voltage, in order to make the system have a higher power density, the capacitance value should be as small as possible. Therefore, the DC side voltage is equal to the sum of the capacitance and inductor voltage.

$$U_{dc} = U_{cs} + L\frac{\mathrm{d}i_{SHCC}}{\mathrm{d}t} \tag{14}$$

The forward difference method is used to discretize the above equation, the discretization period is T_s, and the discretized expression is

$$L\frac{i_{SHCC}(k+1)-i_{SHCC}(k)}{T_s} = U_{dc} - U_{cs}(k) \tag{15}$$

where $i_{SHCC}(k+1)$ represents the current sampling value at $(k+1)T_s$. Ideal beat-free control assumes that the generation of the control signal from AD sampling to the control signal is instantaneous at the kT_s moment and does not consume time. For the actual digital control system, there is inevitably a digital delay in this process, so the traditional deadbeat-predictive control is generally realized in the way of lag one beat, that is, in the control signal calculated in the k-k control cycle u_{cs}^* (k+1) will play a role in the k+1 control cycle. The control delay diagram is shown below

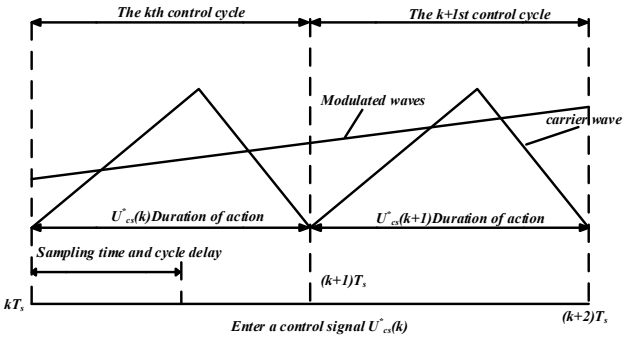


Fig 4. Traditional time-lap control time-lapse plot

Based on the above analysis, it can be seen that only the current is controlled by the above formula, ignoring the one-beat delay of the system itself, that is, the actual lag of the system current is two control cycles of the command current. In order to improve the performance of the deadbeat-predictive control, compensation must be made. Assuming that the selected voltage vector is applied at the k+1 sampling time, the current at the k+2 sampling time must be predicted. Extrapolating the above equation one step back, then the current at the time of k+2 sampling is

$$i_{\mathrm{SHCC}}(k+2) = i_{\mathrm{SHCC}}(k+1) + \frac{T_S}{L}[u_{dc} - u_{cs}(k+1)] \tag{16}$$

Substituting Eq. (6) and $i_{SHCC}(k+2)=i_{SHCC}*(k)$ into Eq. (7) to sort out and deform the command value of the control signal can be obtained:

$$u_{cs}^*(k+1) = 2u_{dc} - u_{cs}^*(k) + \frac{L}{T_s}[i_{\mathrm{SHCC}}(k) - i_{\mathrm{SHCC}}^*(k)] \tag{17}$$

where u_{cs}^* (k+1) works in the k+1 control cycle and is calculated in the k-k control cycle, u_cs^* (k) works in the k-th control cycle, It is calculated in the K-1 control cycle, and the combination of repeat control and deadbeat- predictive control is improved, and the block diagram of the no beat repeat control is as follows:

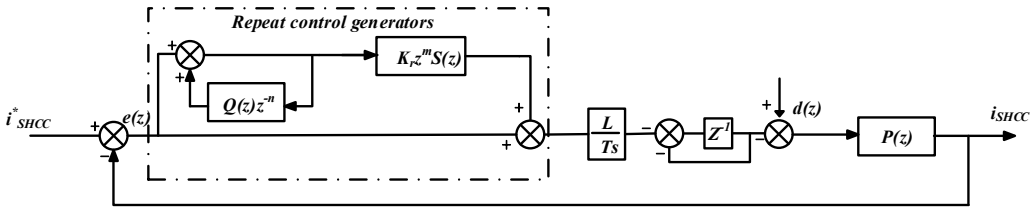


Fig 5. improved deadbeat-repetitive control diagram

As can be seen from the graph, the closed-loop transfer function of the system is

$$G_1(z) = \frac{G_{RC}(z)G_{open}(z)P(z)}{1+G_{RC}(z)G_{open}(z)P(z)} \tag{18}$$

where G_{open} is the open-loop transfer function of the uninterrupted beat.

$$G^{open}(z) = \frac{1}{z^2-1} \tag{19}$$

According to the actual conditions, N is taken as 2000, and Q(z) is taken as 0.95 in practical application, and in order to make the controlled object show zero gain and zero phase shift characteristics in the high, medium and low frequency bands, the design is carried out according to $krz^mS(z)P(z)=1$, Take Kr=1.02, $z^m = z^5$, $z^{-N} = z^{-40}$, The second-order low-pass filter is shown in Eq. (20).

$$S(z) = \frac{0.05061z+0.04306}{z^2-1.523z+0.6166} \tag{20}$$

According to the above controller parameters, a diagram of the amplitude and frequency characteristics of the non-differential beat control under frequency fluctuation is plotted, as shown in Figure 6.

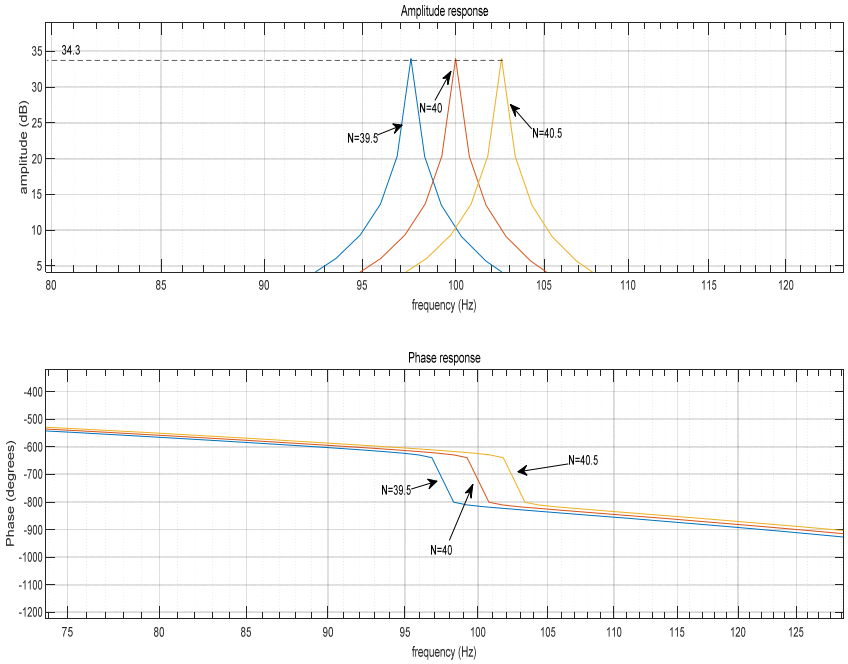


Fig 6. improved deadbeat-repetitive control Amplitude-frequency characteristic diagram

As can be seen from the above figure, when the frequency fluctuates at the double doubling frequency ± 0.5HZ, the gain is maintained at a maximum of 34.3dB, so the steady-state error of current flow can be minimized.

5. Simulation Results and Analysis

In order to verify the correctness and effectiveness of the control strategy, a train single-phase pulse rectifier model was built through the Matlab/Simulink software simulation platform, and its main parameters were set as follows:

Table 1. Simulation parameters

The name of the project	parameter	The name of the project	parameter
DC voltage U_{dc}/V	3600	Decoupling inductors L_f/mH	0.3
Switching frequency/Hz	1kHz	Decoupling capacitorsC_s/mF	2.0
Decoupling capacitor voltageU_{Cs}/V	3200V	Bus capacitors C_{dc}/mF	5.0

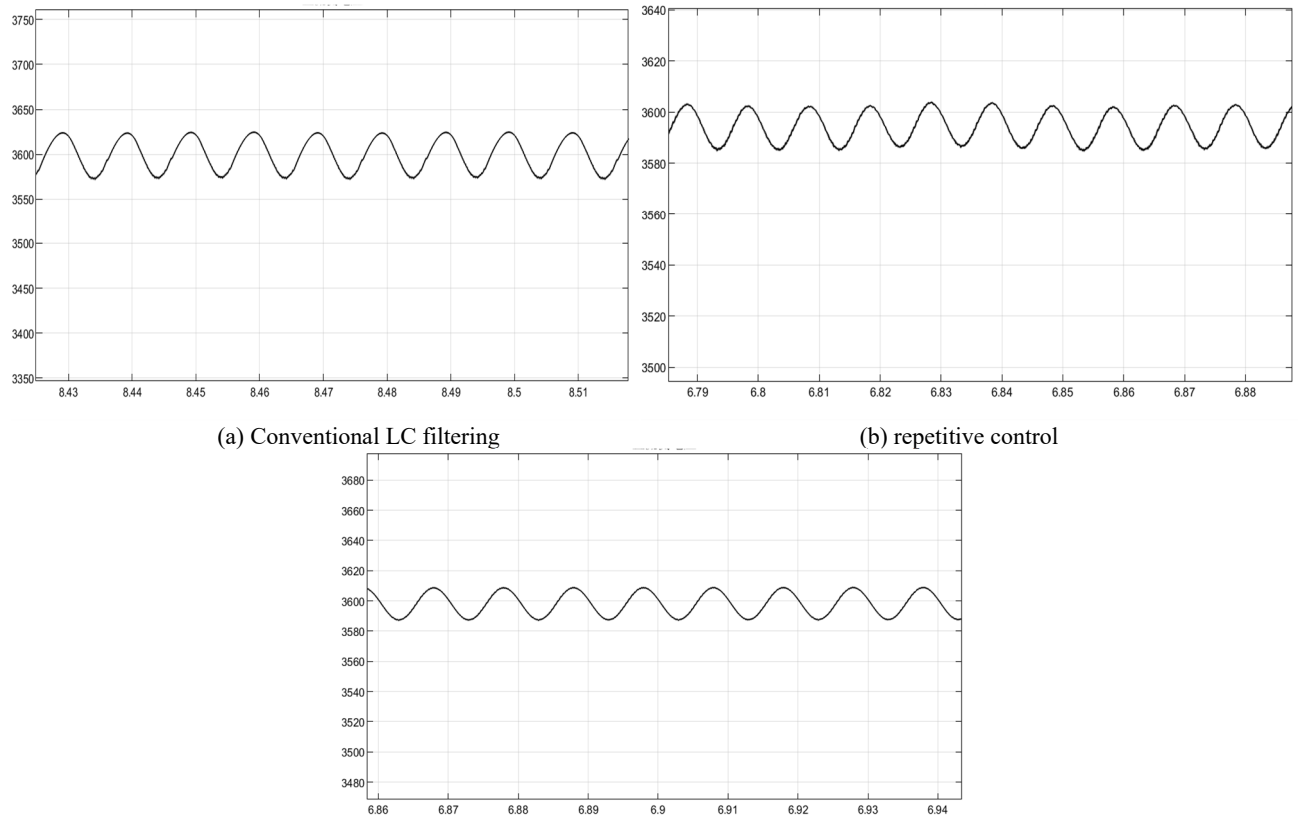
Under the same simulation conditions, the passive LC filtering, the repetitive control strategy and the repetitive control strategy without differential beat are compared and verified, and the simulation results are shown in the figures, including the voltage ripple on the DC side of the rectifier, the second harmonic Fourier analysis, and the response time analysis when the load is abrupt.

As shown in Figure 7, the ripple on the DC side of the traditional LC filter is about 20V, and the repeated control is about 15V, which cannot accurately track the harmonic signal due to its cyclical delay. The improved DC side ripple is about 10V and has a small fluctuation without differential beat, which has better stability.

As can be seen from Figure 8, the ripple harmonic distortion rate of the energy storage capacitor is 2.1%, which is 2.65% less than that of the traditional LC filter of 4.75% and 1.77% less than that of the repeated control of 3.87%. The beat-free repetition control makes the DC side current more stable.

As shown in Figure 9, when the load is abrupt in 2 seconds, the response time of the traditional LC filter is 2.7s, the repeated control is 3.6s, and the repeated control without differential beat is 3s, which improves the dynamic response time compared with the repeated control, but because the addition of devices to the original circuit actually increases the system operation time, the time is 0.3s slower than that of the traditional LC filter, indicating that the anti-interference ability of the improved non-differential beat repetitive control

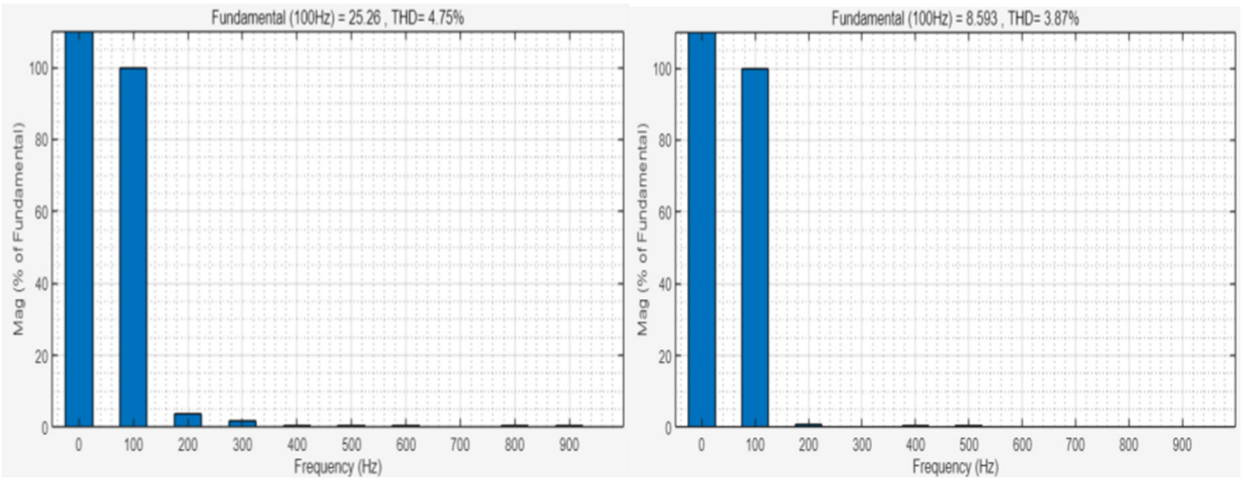
is stronger when the load is abrupt. In this paper, the Buck chopper active power decoupling circuit is used to replace the traditional LC filter circuit, and the electrolytic capacitor is replaced by a thin film capacitor, so as to extend the system life, and the capacitance capacity can be reduced by increasing the energy storage capacitor pulsation, so as to improve the power density of the system.



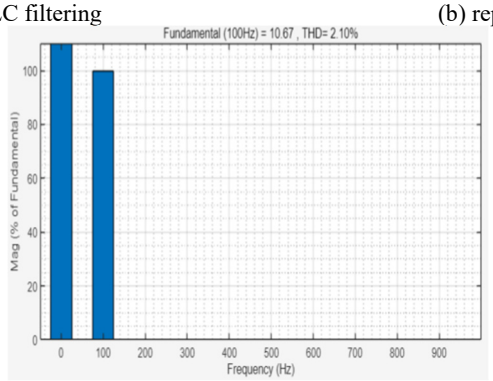
(a) Conventional LC filtering (b) repetitive control

(c) improved deadbeat-repetitive control

Fig 7. DC side voltage

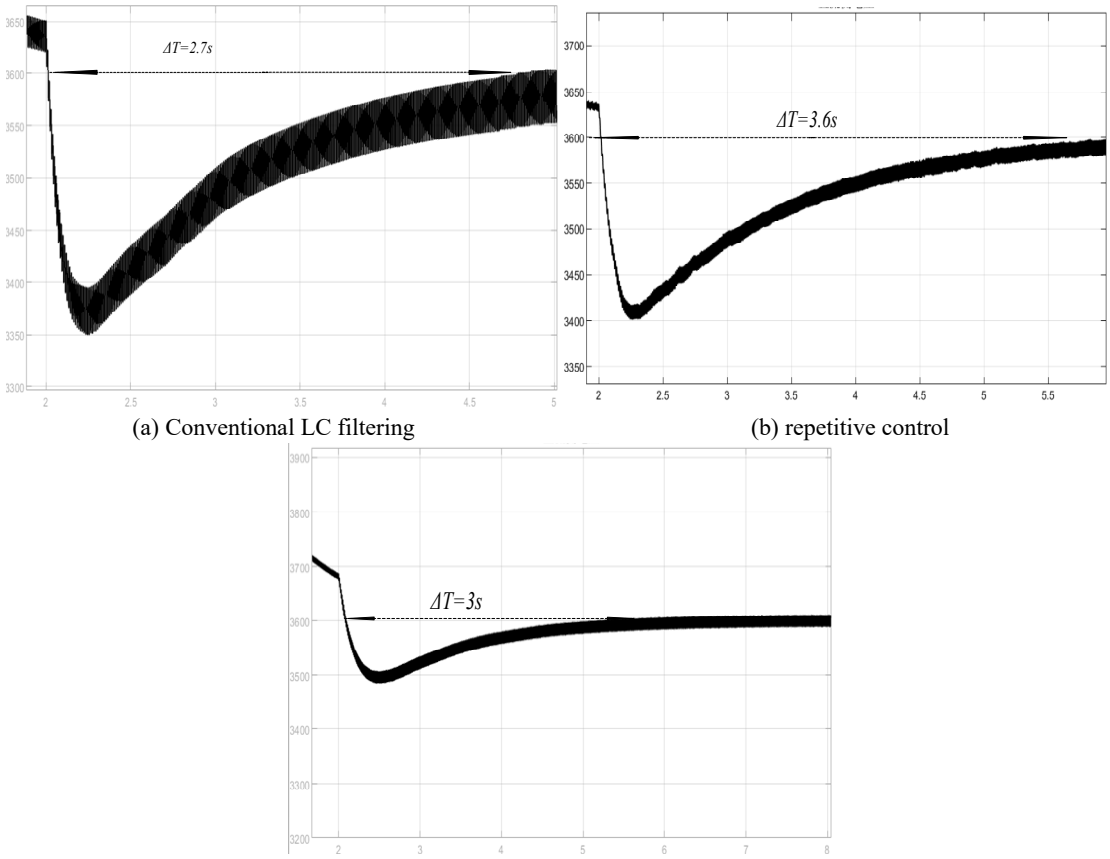


(a) Conventional LC filtering (b) repetitive control



(c) improved deadbeat-repetitive control

Fig 8. DC side voltage spectrum



(a) Conventional LC filtering (b) repetitive control

(c) improved deadbeat-repetitive control

Fig 9. Load change response graph

6. Summary

(1) In this paper, the Buck chopper active power decoupling circuit is used to replace the traditional LC filter circuit, and the electrolytic capacitor is replaced by a thin film capacitor, so as to extend the system life, and the capacitance capacity can be reduced by increasing the energy storage capacitor pulsation, so as to improve the power density of the system.

(2) In this paper, the problem of repeative control cycle delay is obtained through analysis, and an improved control strategy without dead-beat is proposed to improve the dynamic response of the control method, which can effectively reduce the harmonic content and improve the response time of the system through simulation verification.

References

[1] Ruan Xinbo. Second harmonic current suppression technology for single-phase power electronic converter[M]. Beijing: China Machine Press, 2021

[2] Y. Sun, Y. Liu, M. Su, W. Xiong and J. Yang, Review of Active Power Decoupling Topologies in Single-Phase Systems[J]. IEEE Transactions on Power Electronics, 2016,31(7): 4778-4794.

[3] H. V. Nguyen and D. -C. Lee, Reducing the dc-Link Capacitance: A Bridgeless PFC Boost Rectifier That Reduces the Second-Order Power Ripple at the dc Output[J]. IEEE Industry Applications Magazine, 2018,24(2): 23-34.

[4] H. Sun, H. Wang and W. Qi, Automatic Power Decoupling Controller of Dependent Power Decoupling Circuit for Enhanced Transient Performance[J]. IEEE Transactions on Industrial Electronics,2019, 66(3):1820-1831.

[5] XU Junzhong. Research on modulation strategy of modern inverter power supply[D]. Shanghai Jiao Tong University,2021.

[6] S. Li, W. Qi, S. -C. Tan and S. Y. Hui, "Enhanced Automatic-Power-Decoupling Control Method for Single-Phase AC-to-DC Converters[J]. IEEE Transactions on Power Electronics, 2018,33(2): 1816-1828.

[7] ROY J, XIA Yinglai, AYYANAR R. Half-bridge voltage swing inverter with active power decoupling for singlephase PV systems supporting wide power factor range[J]. IEEE Transactions on Power Electronics, 2019, 34(8): 7450-7461.

[8] FENG Zhao, LING Jie, SHEN Yayi. Discrete-Time Integral Terminal Sliding Mode based Repetitive Control for Periodic Motion Tracking[C]//2022 IEEE 11th Data Driven Control and Learning Systems Conference (DDCLS). Chengdu, China. IEEE, 2022: 1031-1036.

[9] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, A dualvoltage control strategy for single-phase PWM converters with power decoupling function[C].2014 IEEE Energy Conversion Congress and Exposition , 2014, 4102–4109.

[10] Shen Lailai, Chen Jie, Liu Dong et al. Research on active secondary filtering based on bidirectional DC-DC circuit [J]. Journal of Beijing Jiaotong University,2019,43(2): 86-92,99.

[11] Cheng Shu, Li Zhuoxin, Zhou Ruirui, et al. Active power decoupling control algorithm for secondary ripple suppression of single-phase rectifier[J].Journal of Electrical Engineering and Control,2024,28(08):94-103.

[12] LI Hongbo,ZHANG Kai,ZHAO Hui. Research on DC active filter for high power density single-phase converter[J], Proceedings of the CSEE,2012,32(15):40.

[13] Lee J-H, Lee J-S, Moon H-C, et al. An Improved Finite-Set Model Predictive Control Based on Discrete Space Vector Modulation Methods for Grid-Connected Three-Level Voltage Source Inverter[J]. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2018, 6(4): 1744–1760.

[14] Ge B, Li X, Zhang H, et al. Direct Instantaneous Ripple Power Predictive Control for Active Ripple Decoupling of Single-

Phase Inverter[J]. IEEE Transactions on Industrial Electronics, 2018, 65(4): 3165–3175.

[15] WANG Yunliang,ZHANG Shuangyang,WU Yanjuan. Harmonic-free detection APF based on active power decoupling [J].Electric Power System and Automation, 2022, 34 (12):145-151.

[16] Wang Liqiao, Wang Haixu, Cui Shumin, et al. Proceedings of the CSEE,2019, 39(17):5195-5204,5300.

[17] Zheng Danping, Nian Heng, Li Laifu, et al. Proceedings of the CSEE,2020,40(11):3643-3654.

[18] Gao Hongxiang, Lin Kai, Mao Xingkui. Research on capacitive clamp active power decoupling circuit[J].Electrical Appliances and Energy Efficiency Management Technology,2019,(13):18-24.

[19] NGUYEN H V, LEE D C. Reducing the dc-link capacitance: a bridgeless PFC boost rectifier that reduces the second-order power ripple at the dc output[J]. IEEE Industry Applications Magazine, 2018, 24(2): 23-34.

[20] Wang Yifeng, Shi Huaidong, Ma Xiaoyong, et al. Active power decoupling method based on dual-objective predictive control[J]. Journal of Electric Power System and Automation, 2024:1-9.

[21] Ding Hao, Zeng Yiming, Li Zhuoxin, et al. Research on decoupling control strategy of active power in DC link of traction converter[J].Journal of Railway Science and Engineering, 2024:1-11.