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Research on Parallel Testing Technology of MCU Chips Based on ATE

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Abstract: Micro - control units (MCUs) are extensively applied across various domains such as automotive electronics, smart homes, and communication equipment. Their testing technology stands as a pivotal element in guaranteeing product quality. Conventional MCU chip testing predominantly utilizes a serial testing mode, which is plagued by issues like lengthy testing duration and low efficiency, rendering it incapable of satisfying the rapid testing demands of large - scale production lines. This paper delves into the parallel testing technology of MCU chips based on Automatic Test Equipment (ATE). By refining the testing scheme, it enhances test parallelism to ensure testing efficiency and diminish testing costs. This study also scrutinizes the fundamental testing requirements of MCU chips and elaborates on the implementation methodology of parallel testing technology based on ATE. It posits that parallel testing technology can substantially curtail testing time, amplify testing throughput, ensure the accuracy and reliability of testing outcomes, and offers a novel solution for large - scale MCU chip testing.

Keywords: MCU; ATE; Parallel Testing Technology; Test Efficiency.

1. Introduction

The industry is exploring parallel testing technology based on automatic test equipment (ATE). As a highly automated testing device, it can accurately test chips and simultaneously test multiple chip functional modules, further improving testing efficiency. This paper introduces the implementation methods of parallel testing technology based on ATE, such as the hardware architecture design of the test system, the optimization strategy of the test process, and the processing and analysis methods of test data. Provide reliable parallel testing solutions for MCU chips to meet the rapid testing requirements of large-scale production lines and promote the application of MCU chip testing technology [1].

This paper uses the TR6836S SII test machine of the new model of TRI and the SOP turret sorter of Macrotest to develop the test scheme of MCU chips.

Fig 1. TR6836S SII

2. Analysis of Testing Requirements and Difficulties for MCU Chips

2.1. Test Requirements

MCU chip testing includes multiple aspects such as functional testing, parameter testing, and stability testing. Functional testing is used to verify whether the chip meets the basic design requirements. Parameter testing focuses on chip simulation parameters, such as voltage, current, rise time, fall time, etc. Stability testing assesses the performance of the chip under external stress conditions.

2.2. Test Difficulties

(1) The issue of interface board universality: Different package of MCU chips have different interfaces, resulting in the interface board of the test system being single, highly specialized, and having a long development cycle[2].

Fig 2. Different package

(2)Signal integrity issue: In parallel testing, interference delays between multi-channel signals lead to inaccurate test results.

(3)Low testing efficiency: The traditional serial testing method takes a long time to test and is difficult to meet the demands of large-scale production [3].

3. The Implementation of Parallel Testing Technology for MCU Chips Based on ATE Testing System Hardware Design

3.1. Test the Hardware Design of the System

(1)Main control device selection and design: FPGA is selected as the main control device. FPGA has a high degree of programmability and can be quickly configured and the test logic adjusted according to the test requirements. The relay

matrix control circuit is designed through FPGA to achieve the parallel control switching of multi-channel signals and improve the test efficiency.

(2) Test board design: In the design of test boards, factors such as signal integrity, impedance matching, and equal delay need to be fully considered. To ensure the accuracy of multi-channel signals during transmission, high-quality transmission lines and meticulous wiring design are required. It has sufficient test resources to meet the test requirements of different models of MCU chips.

T33	1	2	T34	T1	1	2	T2	UR1	1	26	UR3
T35	3	4	T36	T3	3	4	T4	UR2	2	27	UR4
T37	5	6	T38	T5	5	6	T6	UR5	3	28	UR7
GND	7	8	T39	GND	7	8	T7	UR6	4	29	UR8
T40	9	10	T41	T8	9	10	T9	UR9	5	30	UR11
T42	11	12	T43	T10	11	12	T11	UR10	6	31	UR12
GND	13	14	T44	GND	13	14	T12	UR13	7	32	UR15
T45	15	16	T46	T13	15	16	T14	UR14	8	33	UR16
T47	17	18	T48	T15	17	18	T16	UR17	9	34	UR19
GND	19	20	GND	GND	19	20	GND	UR18	10	35	UR20
SP2	21	22	T49	SP1	21	22	T17	UR21	11	36	UR23
T50	23	24	T51	T18	23	24	T19	UR22	12	37	UR24
T52	25	26	T53	T20	25	26	T21	UR25	13	38	UR27
GND	27	28	T54	GND	27	28	T22	UR26	14	39	UR28
T55	29	30	T56	T23	29	30	T24	UR29	15	40	UR31
T57	31	32	T58	T25	31	32	T26	UR30	16	41	UR32
GND	33	34	T59	GND	33	34	T27	GND	17	42	5VR
T60	35	36	T61	T28	35	36	T29	GND	18	43	5VR
T62	37	38	T63	T30	37	38	T31	GND	19	44	5VR
T64	39	40	GND	T32	39	40	GND	GND	20	45	5V
								GND	21	46	5V
								GND	22	47	GND
								GND	23	48	GND
								DVM_N	24	49	NC
								DVM_P	25	50	NC

Fig 3. DD64 Interface definition

(3)Impedance matching and equal delay design: In the hardware design of the test system, impedance matching and equal delay design are completed. Impedance matching ensures the reflection of signals during transmission and improves the quality of signal transmission. The equal delay design ensures that the delay of multi-channel signals is consistent during transmission, avoiding test errors caused by delay differences[4].

(4)Test head and interface design: In the design of the test head, the layout and arrangement of the probes are taken into account to ensure that the probes can accurately contact the pins of the MCU chip. The test head needs to be equipped with a built-in test board card and test channel interface to facilitate connection and communication with devices such as ATE, probe stations and sorters.

3.2. Test Process Optimization

In the parallel testing of MCU chips based on ATE, test programs are written in C language to achieve the automatic sending and receiving of test instructions[5]. To improve the maintainability of the test program, the modular design concept is adopted, and the test program is divided into multiple independent modules, such as the initialization module, functional test module, parameter test module, etc.

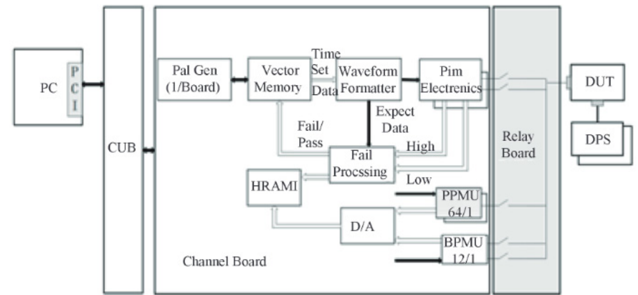

Fig 4. Test the basic structure of the system

When it is necessary to adjust a certain test item, only the corresponding module needs to be modified instead of making large-scale modifications to the entire test program. Test items that independently use test resources, such as functional matching tests, frequency tests, and parameter tests, are processed in parallel. For example, during the functional testing stage, the basic functions of multiple MCU chips are verified simultaneously. During the parameter testing stage, the analog parameters of multiple chips, such as voltage and current, are tested in parallel. In order to achieve real-time collection and processing of test data, corresponding data collection points are set in the test program. When ATE sends test instructions and receives test responses, the test program automatically collects the corresponding test data, observes the test data in real time, and promptly handles abnormal situations to ensure the smooth progress of the test.

Sequence Items | Grade Items

Skip	F/P	UnLog	Seq#	Parm#	Sequence Name	Action	Act_Arg	Parm. Name	Type	Min.	Max.	Unit	Note
			1		OS_PIN	Fail To Bin	2						
				1				OSN_PIN	N	-0.9	-0.2	V	
				2				OSP_PIN	N	0.2	0.9	V	
				3				OS_VDD	N	-0.9	-0.2	V	
			2		OPT_TEST	Fail To Bin	3						
			3		ICC_TEST	Fail To Bin	4						
				1				ICCH	N	-1	1	uA	
				2				ICCL	N	-1	1	uA	
			4		IOH_IOL_TEST	Fail To Bin	4						
				1				P00	N	-40	-10	MA	
				2				P01	N	-40	-10	MA	
				3				P02	N	-40	-10	MA	
				4				P03	N	-40	-10	MA	
				5				P04	N	-40	-10	MA	
				6				P05	N	-40	-10	MA	
				7				P06	N	-40	-10	MA	
				8				P10	N	-40	-10	MA	
				9				P11	N	-40	-10	MA	
				10				P12	N	-40	-10	MA	
				11				P13	N	-40	-10	MA	

Fig 5. DD64 Interface definition

The parallel testing technology of MCU chips based on ATE, combined with intelligent algorithms such as machine learning and artificial intelligence, conducts in-depth analysis of test data. Through intelligent algorithms, abnormal trends

in test data are automatically identified, providing support for the optimization design and improvement of chips. The parallel testing technology of MCU chips based on ATE allows for the automatic generation of detailed test reports and visually presents the test results in the form of charts, curves, etc.

3.3. Test Production Efficiency

Large-scale production enterprises have very short requirements for the testing cycle. Each batch is a product of the KK scale. Generally, all testing steps, including testing, appearance inspection, packaging, etc., are required to be completed within 1 to 2 days. Therefore, the time left for the testing station is usually less than 1 day. Therefore, the efficiency of testing is of great significance to the output of test production, directly affecting the production costs, profits, etc. of enterprises, and is an important indicator for test production enterprises to measure factory operations.

The manifestation of testing production efficiency can be intuitively reflected in the output of the produced products. If the quantity of products produced per day in the test production increases, it can be understood as an improvement in the efficiency of the test production. The following is an analysis of the quantity of products produced within a unit of time. The quantity of products that can be produced per hour is defined as UPH (units per hour). Under ideal conditions, after eliminating uncertain factors such as equipment malfunctions and human operational errors, theoretically, the UPH of test production is defined by the following formula:

$$\mathrm{UPH} = \frac{3600}{\mathrm{T_t} + \mathrm{T_i}} * \mathrm{S} \quad (1)$$

In the formula: 3600 -- the number of seconds per hour;

T_t--Test Time, the number of seconds required to complete one Touchdown (Touchdown refers to a test cycle: if it is a single product test, it is the test time of one product; if it is a multi-station test, it is the test time required to complete the test of products at all stations);

T_i -- Index Time,the number of seconds between the end of one Touchdown test and the next Touchdown;

S -- Site, the number of products to be tested simultaneously with each Touchdown;

It can be concluded through Formula 1 that the production output per hour is the number of seconds per hour divided by the complete time of one test (the time required for product testing + the interval from completing one test to starting the next test), and then multiplied by the number of tests conducted simultaneously in each test. It can be seen that the more the number of simultaneous tests in each test, the more beneficial it is to the number of production outputs per hour. Therefore, it is necessary to study the methods of prompt test outputs in the direction of increasing the number of simultaneous tests.

With the definition of output per hour, let's analyze the output per day, which is defined as UPD (Units per Day), that is, the quantity of products that can be produced each day. Theoretical definition of UPD:

$$\mathrm{UPD} = \mathrm{UPH} * 24 \quad (2)$$

In the formula: UPH -- Throughput in Units per;

24 -- The number of hours in a day;

This is the definition of the daily production quantity under ideal conditions. Multiplying the production output per hour by the number of hours in a day gives the daily production output. However, in general, each factory has its own equipment Utilization rate (Utilization), that is, what proportion of the time each piece of equipment spends on actual production and what proportion of the time is spent on maintenance, repair, etc. The higher the utilization rate, the more time the equipment is used for product production. Under normal circumstances, the general empirical value is 85%, that is, the utilization rate of the equipment =85%. It can be concluded from this that the daily production output of the actual factory is:

$$\mathrm{UPD} = \frac{3600}{\mathrm{T_t} + \mathrm{T_i}} * \mathrm{S} * 24 * 85\% \quad (3)$$

From the above definition analysis, it can be concluded that the daily output in the actual production environment is based on the theoretical UPD and takes into account the actual equipment utilization rate. How to increase the quantity of products produced every day is related to the following factors:

(1) Test Time, the test time of the product is inversely proportional to UPH. The longer the test time, the less UPH, which directly affects UPH.

(2) Index Time, the waiting time between each test of one product and the next product is inversely proportional to UPH. The longer the Index time, the less UPH.

(3) Site, the number of products tested simultaneously each time Touchdown, is directly proportional to UPH. The more products tested simultaneously, the more UPH.

(4) Utilization, which determines the actual time that production equipment is used for output, is proportional to UPD. The higher the utilization rate, the higher the UPD.

Based on the above analysis, if more products are to be produced within a unit of time, it is necessary to optimize the above factors and adjust each factor to the output that is most conducive to production. Thereby improving the efficiency of test production.

Fig 6. DD64 Interface definition

If the test time for each single chip is 1.6 seconds, the UPH of the single SITE test is 1900 and the UPD is 38760. Since some test items can only be tested serially and when using multi-site testing, the index time of the sorter will increase. So during the 2SITE test, the test time was 1.8 seconds, UPH=3500, and UPD=71400. During the 4SITE test, the test duration was 2.1 seconds, with UPH=5200 and UPD=106080.

It can be known from this that by developing the test

scheme of four sites with the same resource allocation, the daily production capacity can be increased by 48.57%. In the case of full order load, the time occupied by this product on the machine can be saved. Meanwhile, the adapter board developed by this solution can be used for the development and optimization of other products.

3.4. Test Data Processing and Analysis

(1) Real-time data acquisition and monitoring: ATE devices can simultaneously send test instructions to multiple MCU chips and receive the returned test responses. The response data contains key information such as the working status and performance parameters of the chip. For example, data collection points are set in the test program to ensure that the corresponding data is obtained in a timely manner after each test operation. Ensure the stability of the monitoring and testing process, and conduct real-time monitoring of key indicators such as the test pass rate, test time, and error rate. Once abnormal fluctuations are detected, the alarm mechanism will be triggered immediately to promptly investigate the problem.

(2) Data preprocessing and cleaning: The collected raw test data contains noise, outliers or missing values, which need to be preprocessed for subsequent analysis. Data preprocessing includes steps such as removing duplicate data, filling in missing values, and smoothing noise. After cleaning, the data is more accurate and reliable, providing a solid foundation for subsequent analysis. In the parallel testing environment, the complexity of data preprocessing and cleaning increases significantly. Processing data from multiple chips simultaneously requires the design of efficient data processing algorithms to ensure the completion of data preprocessing within a limited time.

(3) Data visualization and preliminary analysis: After preprocessing and cleaning, the test data needs to be preliminarily analyzed through visualization. Data visualization visually presents the distribution, trends and outliers of data, providing clues for subsequent in-depth analysis. In parallel testing, various forms such as charts, curves, and scatter plots are used to present test data. For instance, bar charts are used to compare the test pass rates of different chips, line graphs are used to show the changing trend of test time with test batches, and scatter plots are used to analyze the correlation between performance parameters.

(4) In-depth data analysis and mining: Conduct in-depth analysis of test data to extract more valuable information. In statistical analysis, calculate the mean, variance, maximum value, minimum value and other statistical indicators of the test data to understand the overall distribution of the data. In the correlation analysis, the correlations among different performance parameters are explored to provide a basis for the optimal design of the chip. In cluster analysis, similar test data are grouped into one category to discover potential types of test patterns.

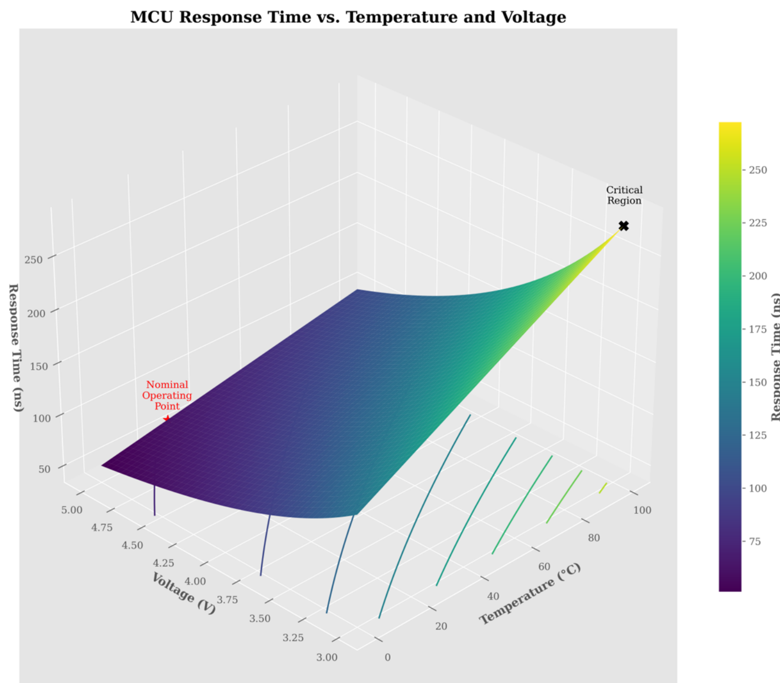

Fig 7. The failure rate presents a typical "bathtub curve" feature

(5) Intelligent data processing and analysis technology: With the continuous development of artificial intelligence technology, intelligent data processing and analysis technology has been widely applied in the testing of MCU chips. Introduce algorithms such as machine learning and deep learning to conduct high-level analysis and mining of test data. For example, machine learning algorithms are used to classify and predict test data to identify potential defects. Use deep learning technology to complete feature extraction of test data and discover hidden test patterns.

(6) Test report generation and data visualization display: The processing and analysis results of test data need to be output and displayed in the form of a report. The test report should include detailed test data, analysis results, conclusions, and suggestions, etc., to facilitate the understanding of the test situation by testers, designers, and managers. Visually display the test data results and generate various charts and graphs using data visualization technology.

4. Summary

To sum up, this paper studies the parallel testing technology of MCU chips based on ATE. The key points are measures such as optimizing the test plan, improving the hardware

design of the test system, optimizing the test process, and strengthening the processing and analysis of test data, to achieve efficient parallel testing of MCU chips. This technology improves the testing efficiency, reduces the testing cost, and provides support for the quality control and performance optimization of MCU chips.

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