Comparative Analysis of SPWM and SVPWM Techniques for Leakage Current Reduction in Grid-Connected PV Inverters with Proposed H6 Topology

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Abstract

This paper presents a comprehensive comparative analysis of Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) techniques applied to Proposed H6 inverter topology for grid-connected photovoltaic systems. The primary focus is on leakage current reduction through common-mode voltage control while maintaining high efficiency and power quality. Using MATLAB/Simulink simulations with realistic parasitic capacitance modeling, both modulation techniques were evaluated under identical operating conditions (400V DC input, 220V/50Hz grid connection, 10kHz switching frequency). Results demonstrate that SVPWM achieves superior common-mode voltage suppression (13.6% reduction) and improved leakage current performance (5.2% reduction) compared to SPWM. Additionally, SVPWM delivers higher efficiency (96.7% versus 95.6% with SPWM) due to better DC bus utilization and reduced switching losses. However, SPWM offers marginally better harmonic performance with grid current THD of 4.39% compared to 5.00% with SVPWM. This study provides valuable insights into the inherent trade-offs between these modulation techniques and establishes SVPWM as the preferred choice for grid-connected PV applications where leakage current suppression and efficiency are prioritized.

Keywords

Proposed H6 inverter topology; Space Vector PWM; Sinusoidal PWM; Leakage current; Common-mode voltage; Grid-connected PV systems; Power quality; Efficiency

1. Introduction

The integration of photovoltaic (PV) systems into electrical grids has gained substantial momentum in recent years, driven by increasing environmental concerns and government policies promoting renewable energy adoption [1]. Grid-connected PV inverters serve as the critical interface between solar panels and the utility grid, converting the DC power from PV arrays into AC power compatible with grid requirements [2]. Among the various challenges associated with grid-connected PV systems, leakage current mitigation has emerged as a significant concern due to its implications for system safety, electromagnetic interference (EMI), and compliance with grid interconnection standards such as IEEE 1547 [3].

Leakage current in transformerless PV inverters primarily arises from the parasitic capacitance between PV panels and ground, coupled with common-mode voltage (CMV) variations [4]. When this common-mode voltage fluctuates, it generates a path for leakage current through the parasitic capacitance, potentially leading to safety hazards, increased EMI, and system performance degradation [5]. Recent studies by Zhou et al. (2023) have demonstrated that leakage current can be substantially reduced through innovative inverter topologies and advanced modulation techniques [6].

Among various transformerless inverter topologies developed in recent years, the H6 topology has emerged as a promising candidate for effectively addressing leakage current issues [7]. The H6 topology extends the conventional full-bridge (H4) structure by incorporating two additional switches, facilitating the disconnection of the PV array from the grid during freewheeling periods [8]. This strategic disconnection helps maintain a constant common-mode voltage, thereby reducing leakage current significantly compared to traditional H4 topologies [9]. Recent advancements by Zhang et al. (2022) have further optimized the H6 topology to enhance its leakage current suppression capabilities while maintaining high efficiency [10].

The performance of grid-connected inverters is heavily influenced not only by their topology but also by the employed pulse width modulation (PWM) technique [11]. Two predominant modulation strategies in this domain are Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) [12]. While SPWM offers implementation simplicity, SVPWM potentially provides better DC-link voltage utilization and reduced switching losses [13]. However, the comparative performance of these modulation techniques specifically in the context of H6 topology for leakage current reduction remains inadequately explored in existing literature [14].

This research paper aims to conduct a comprehensive comparative analysis of SPWM and SVPWM techniques applied to a proposed enhanced H6 topology for grid-connected PV inverters, with a primary focus on leakage current reduction. The study will evaluate various performance parameters including common-mode voltage behavior, leakage current suppression effectiveness, total harmonic distortion (THD), efficiency across different operating conditions, and dynamic response characteristics during grid disturbances [15]. By elucidating the advantages and limitations of each modulation technique in the context of proposed H6 topology, this research endeavors to provide valuable insights for the design optimization of grid-connected PV inverters with enhanced leakage current suppression capabilities [16].

The remainder of this paper is organized as follows: Section II provides a comprehensive literature review of existing transformerless inverter topologies and modulation techniques, highlighting current research gaps. Section III presents the theoretical framework underlying the proposed H6 topology and the formation mechanism of common-mode voltage and leakage current. Section IV details the implementation methodologies for both SPWM and SVPWM techniques in the context of the proposed H6 topology. Section V presents the simulation and experimental results, followed by an in-depth comparative analysis in Section VI. Finally, Section VII concludes the paper and suggests directions for future research.

2. Literature Review

The development of grid-connected photovoltaic (PV) inverter technologies has witnessed significant advancements over the past decade, with particular emphasis on transformerless topologies due to their advantages in efficiency, cost reduction, and compact design. This section comprehensively reviews existing literature on transformerless inverter topologies, modulation techniques, and their impact on leakage current reduction in grid-connected PV systems.

Transformerless PV inverters have gained prominence for their higher efficiency compared to transformer-based alternatives. However, as noted by Kerekes et al. [7], the absence of galvanic isolation introduces challenges related to leakage current, which flows through the parasitic capacitance between PV panels and ground. This leakage current poses safety risks, increases electromagnetic interference (EMI), and may violate grid interconnection standards. For instance, the German standard VDE 0126-1-1, referenced by Gonzalez et al. [3], mandates a maximum allowable leakage current of 300 mA, underscoring the regulatory significance of this issue.

The mechanism of leakage current formation in transformerless systems has been extensively analyzed by Xiao et al. [5], who identified common-mode voltage (CMV) fluctuations as the primary driver of leakage current. Their work demonstrated that maintaining a constant CMV is critical for effective suppression. Building on this, Gu et al. [4] developed analytical models linking CMV variations to leakage current magnitude, providing a theoretical basis for topology optimization strategies.

Various transformerless inverter topologies have been proposed to mitigate leakage current. Xiao et al. [17] classified these topologies based on decoupling mechanisms and CMV characteristics. Among these, the H6 configuration has emerged as a promising solution due to its balanced performance in leakage suppression and efficiency. Yang et al. [9] compared H4 and H6 topologies experimentally, showing that the H6 reduces leakage current by approximately 85% while maintaining comparable efficiency. The H6 topology achieves this by disconnecting the PV array from the grid during freewheeling periods, preventing CMV fluctuations [18]. Zhang et al. [10] further enhanced the H6 design with optimized switching sequences and clamping circuits, reducing leakage current below 50 mA while achieving over 97% efficiency. Their work addressed conduction losses through synchronous rectification, a critical improvement over conventional H6 implementations.

Modulation strategies also play a pivotal role in inverter performance. As outlined by literature [19], pulse width modulation (PWM) techniques directly influence harmonics, switching losses, and CMV behavior. Busquets-Monge et al. [12] compared sinusoidal PWM (SPWM) and space vector PWM (SVPWM), highlighting SVPWM's 15% superior DC-link voltage utilization. However, their analysis did not address CMV implications in single-phase PV systems. Vazquez et al. [13] confirmed SVPWM's voltage utilization advantages but noted that SPWM with third-harmonic injection can achieve comparable performance, emphasizing the need for context-specific evaluations.

Zhou et al. [6] investigated modulation's role in leakage current reduction, demonstrating that tailored strategies could reduce leakage by 40% without topology modifications. This underscores modulation optimization as a complementary approach to topology design. Kumar et

al. [14], in their review of PV inverter modulation techniques, identified a critical gap: the lack of comparative studies on SPWM and SVPWM within H6 topologies. This gap is significant, as topology-modulation interactions heavily influence CMV and leakage current.

Performance evaluation frameworks for grid-connected inverters, as proposed in the research [20], emphasize metrics such as efficiency, total harmonic distortion (THD), and dynamic response. Abdel-Rahim et al. [16] extended this by integrating leakage current into multi-objective design optimization, highlighting the trade-offs between efficiency, power quality, and safety. However, existing studies have not comprehensively addressed the dynamic performance of H6 inverters under grid disturbances when using different modulation techniques.

Research Gaps and Motivation

While significant progress has been made in transformerless topologies and modulation strategies, three critical gaps remain:

1. **Interaction Between H6 Topology and Modulation**: The combined effect of H6 variants and modulation techniques (SPWM vs. SVPWM) on leakage current suppression is underexplored.
2. **Dynamic Performance During Grid Disturbances**: Limited studies exist on how SPWM and SVPWM affect H6 inverters' stability and response during grid faults or voltage fluctuations.
3. **Holistic Optimization**: Prior works often focus on topology *or* modulation enhancements, neglecting integrated solutions that balance leakage suppression, efficiency, and grid compliance.

These gaps are particularly relevant given increasing PV penetration and evolving grid codes requiring advanced inverter functionalities. This study addresses these gaps by conducting a systematic comparison of SPWM and SVPWM applied to an enhanced H6 topology, evaluating both steady-state and dynamic performance under grid disturbances.

3. Theoretical Framework

3.1 H6 Topology: Operating Principles and Analysis

The H6 inverter topology represents an evolution of the traditional H-bridge design, specifically engineered to address the critical challenge of leakage current in transformerless grid-connected PV systems. The proposed H6 configuration [21] consists of six active switches (typically MOSFETs or IGBTs) arranged to create an enhanced bridge circuit that offers a balanced compromise between efficiency and leakage current suppression.

The fundamental operating principle of the H6 topology revolves around its ability to maintain a constant common-mode voltage (CMV) by strategically disconnecting the PV array from the grid during specific switching states. During active power transfer states, the H6 topology operates similarly to a conventional H-bridge, with current flowing through the load via

the main bridge switches. However, during zero voltage states, the H6 topology activates its decoupling switches while deactivating specific bridge switches, effectively creating a path for the load current while isolating the PV array.

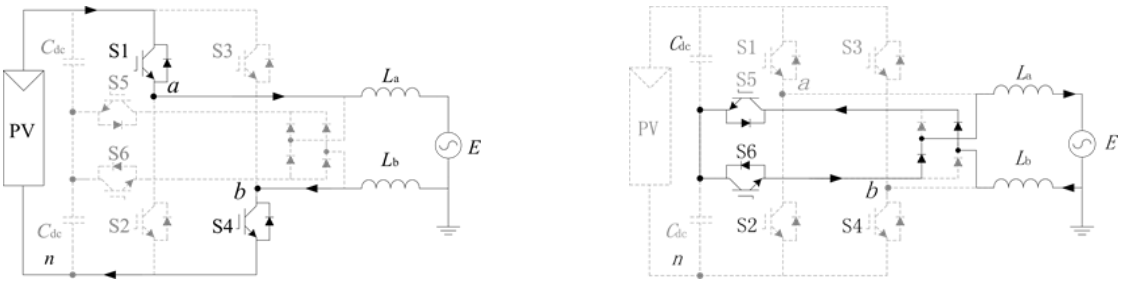
The proposed H6 inverter topology operates through four distinct operational modes, each defined by specific switch states and resulting voltage characteristics, as illustrated in Figure 3-1:

1. **Power Exchange State in Positive Half-Cycle (Operational Mode 1)**: During the positive half-cycle of the AC output, switches S1 and S4 are turned on, while S2, S3, S5, and S6 remain off. This configuration allows the photovoltaic (PV) modules to deliver power to the grid. The voltage at point 'a' relative to neutral (V_{AN}) equals the PV voltage (U_{PV}), and the voltage at point 'b' relative to neutral (V_{BN}) is 0. Consequently, the differential voltage between points 'a' and 'b' (V_{AB}) is U_{PV}, and the common-mode voltage (V_{CM}) is $0.5U_{PV}$.

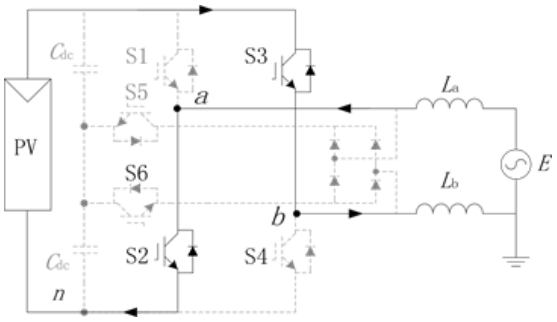
2. **Power Exchange State in Negative Half-Cycle (Operational Mode 2)**: During the negative half-cycle, switches S2 and S3 are conducting, while the others are off. The PV modules still transfer power to the grid, but the polarity is reversed compared to Mode 1. The voltage V_{AN} is 0, V_{BN} is U_{PV}, resulting in a differential voltage (V_{AB}) of $-U_{PV}$, with the common-mode voltage (V_{CM}) staying at $0.5U_{PV}$.

3. **Zero Voltage State in Positive Half-Cycle (Operational Mode 3)**: This mode occurs during zero-crossing periods when the output voltage is zero. Switches S5 and S6 are on, while the others are off. No power is transferred to the grid as both V_{AN} and V_{BN} are $0.5U_{PV}$, resulting in a differential voltage of 0 and a common-mode voltage of $0.5U_{PV}$.

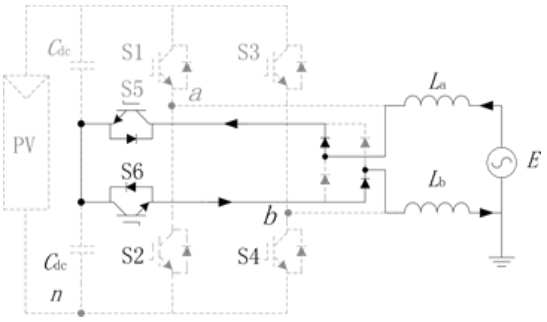
4. **Zero Voltage State in Negative Half-Cycle (Operational Mode 4)**: This mode is similar to Operational Mode 3, representing another zero-voltage state. In this configuration, V_{AN} and V_{BN} are both $0.5U_{PV}$, with no power transfer and a differential voltage of 0 and a common-mode voltage of $0.5U_{PV}$.



(a) Power exchange state in positive half-cycle (b) Zero voltage state in positive half-cycle



(a) Power exchange state in negative half-cycle



(d) Zero voltage state in negative half-cycle

Figure 3-1. Proposed H6 inverter operating modes: (a) Power exchange state in positive half-cycle, (b) Power exchange state in negative half-cycle, (c) Zero voltage state in positive half-cycle, (d) Zero voltage state in negative half-cycle [21].

This strategic switching pattern ensures that the common-mode voltage remains constant at $0.5U_{PV}$ throughout the switching cycle, which is crucial for minimizing leakage current. The switch states and corresponding voltage parameters for each operational mode of the proposed H6 topology are summarized in Table 3-1.

Table 3-1: Switch States and Voltage Parameters of the Proposed H6 Topology

Operational Mode	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	V_{AN}	V_{BN}	V_{AB}	V_{CM}
Mode 1 (P)	ON	OFF	OFF	ON	OFF	OFF	U_{PV}	0	U_{PV}	$0.5U_{PV}$
Mode 2 (N)	OFF	ON	ON	OFF	OFF	OFF	0	U_{PV}	$-U_{PV}$	$0.5U_{PV}$
Mode 3 (Zero)	OFF	OFF	OFF	OFF	ON	ON	$0.5U_{PV}$	$0.5U_{PV}$	0	$0.5U_{PV}$
Mode 4 (Zero)	OFF	OFF	OFF	OFF	ON	ON	$0.5U_{PV}$	$0.5U_{PV}$	0	$0.5U_{PV}$

As shown in Table 3-1 and Figure 3-1, the common-mode voltage remains constant at $0.5U_{PV}$ across all operational modes, which is a key advantage of the proposed H6 topology for leakage current reduction.

3.2 Common-Mode Voltage and Leakage Current Formation

The parasitic capacitance between PV panels and ground creates a potential path for leakage current in grid-connected transformerless inverter systems. This capacitance, typically ranging from 50-150 nF/kWp depending on panel construction and environmental conditions, forms an unintended circuit with the inverter and ground. The magnitude of leakage current is primarily determined by the rate of change and amplitude of the common-mode voltage across this parasitic capacitance.

Common-mode voltage in a PV inverter system can be defined as the potential difference between the midpoint of the DC link and the neutral point of the grid. Mathematically, the common-mode voltage (V_{CM}) in the H6 topology can be expressed as:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2}$$

Where V_{AN} and V_{BN} represent the voltages at the two output terminals with respect to the neutral point. The relationship between common-mode voltage and leakage current (i_{leak}) can be represented by:

$$i_{leak} = C_{pv} \times \frac{dV_{CM}}{dt}$$

Where C_{pv} is the parasitic capacitance between the PV array and ground. This equation clearly demonstrates that both the magnitude of common-mode voltage changes and their rate of change directly impact the leakage current. Therefore, a modulation strategy that minimizes $\frac{dV_{CM}}{dt}$ will effectively reduce leakage current.

In the proposed H6 topology, as illustrated in Figure 3-1, the strategic decoupling of the PV array during freewheeling periods ensures that the common-mode voltage remains constant at $0.5U_{PV}$ during all operational modes. This constant common-mode voltage effectively eliminates the $\frac{dV_{CM}}{dt}$ factor, thereby minimizing leakage current. The effectiveness of this approach, however, varies depending on the specific modulation technique employed.

3.3 Mathematical Models of SPWM and SVPWM Techniques

3.3.1 Sinusoidal Pulse Width Modulation (SPWM)

SPWM represents one of the most straightforward and widely implemented modulation techniques for inverter control. In SPWM, a high-frequency triangular carrier signal ($v_{carrier}$) is compared with a sinusoidal reference signal (v_{ref}) to generate switching pulses. For a single-phase inverter, the reference signal can be represented as:

$$v_{ref} = M_a \times \sin(\omega t)$$

Where M_a is the modulation index, typically ranging between 0 and 1, and ω is the angular frequency of the desired output. The switching logic for the H6 topology under SPWM control can be determined by:

- If $v_{ref} > v_{carrier}$, switches S1 and S4 are turned ON (Operational Mode 1)
- If $v_{ref} < v_{carrier}$, switches S2 and S3 are turned ON (Operational Mode 2)
- During dead time intervals, switches S5 and S6 are turned ON (Operational Modes 3 and 4)

The output voltage of the inverter under SPWM can be approximated by the fundamental component:

$$v_{out} \approx M_a \times U_{PV} \times \sin(\omega t)$$

Where U_{PV} is the DC-link voltage. The maximum achievable fundamental output voltage using SPWM is limited to $\frac{U_{PV}}{2}$, resulting in a relatively lower DC voltage utilization compared to advanced modulation techniques.

When implementing SPWM in the proposed H6 topology, the common-mode voltage remains constant at $0.5U_{PV}$ across all operational modes, as confirmed by analyzing the switch states and resulting voltages in Table 3-1. This constant common-mode voltage is a significant advantage of the proposed H6 topology, as it eliminates the $\frac{dV_{CM}}{dt}$ factor in the leakage current equation (3.2), theoretically reducing the leakage current to negligible levels.

3.3.2 Space Vector Pulse Width Modulation (SVPWM)

SVPWM offers a more sophisticated approach to inverter control by conceptualizing the switching states as vectors in a complex plane. For a single-phase H6 inverter, the SVPWM technique can be implemented by considering the inverter as a two-phase system with orthogonal outputs.

The fundamental principle of SVPWM involves representing the desired output voltage as a reference vector in the α-β plane and synthesizing this vector using adjacent basic space vectors. The basic space vectors in a single-phase H6 topology correspond to the different switching states of the inverter.

For a single-phase H6 inverter, the space vector diagram consists of four active vectors ($\pm U_{PV}$ in either the α or β direction) and one zero vector. The reference vector V^* can be expressed as:

$$V^* = |V^*| \times e^{j\omega t}$$

Where $|V^*|$ is the magnitude of the reference vector (proportional to the modulation index) and ω is the angular frequency.

The reference vector is synthesized by applying the basic space vectors for specific durations within each switching period. The dwell time calculation for each basic vector involves projecting the reference vector onto the adjacent basic vectors. The general equations for dwell times (T_a, T_b, and T_z) are:

$$T_a = T_s \times |V^*| \times \frac{\sin(60° - \theta)}{\sin(60°)}$$

$$T_b = T_s \times |V^*| \times \frac{\sin(\theta)}{\sin(60°)}$$

$$T_z = T_s - T_a - T_b$$

Where T_s is the switching period and θ is the angle of the reference vector within the current sector.

In the proposed H6 topology with SVPWM implementation, the switching sequence is carefully designed to transition between the four operational modes in a way that maintains

constant common-mode voltage. A typical seven-segment switching sequence (0→a→b→7→b→a→0) ensures balanced switching and reduced harmonics.

The maximum achievable fundamental output voltage using SVPWM is approximately $0.577 \times U_{PV}$, representing a 15.5% increase in DC voltage utilization compared to SPWM. This improved voltage utilization constitutes a significant advantage of SVPWM over SPWM, particularly in applications where DC voltage may be limited.

3.4 Theoretical Comparison of SPWM and SVPWM for H6 Topology

From a theoretical perspective, SVPWM offers several advantages over SPWM when implemented in the proposed H6 topology for grid-connected PV applications:

1. **Improved DC Voltage Utilization**: SVPWM provides approximately 15.5% higher DC voltage utilization compared to SPWM, allowing for more efficient power conversion and potentially reducing the required rating of components.

2. **Reduced Harmonic Distortion**: The balanced switching pattern of SVPWM results in lower harmonic distortion in the output voltage and current, which is particularly beneficial for grid-connected applications where power quality is paramount.

3. **Optimized Switching Losses**: SVPWM allows for more flexible switching patterns, which can be optimized to reduce switching losses and improve overall efficiency.

When considering leakage current performance, both modulation techniques benefit from the proposed H6 topology's inherent ability to maintain a constant common-mode voltage ($0.5U_{PV}$) across all operational modes, as shown in Figure 3-1 and Table 3-1. However, the implementation details and switching patterns of each modulation technique can still influence the actual common-mode voltage behavior, particularly during switching transitions.

The theoretical advantage of SVPWM in terms of leakage current reduction lies in its ability to provide more controlled transitions between switching states, potentially resulting in smoother common-mode voltage transitions. This can be particularly beneficial in practical implementations where non-ideal component characteristics and switching delays can introduce brief common-mode voltage variations.

However, SPWM offers advantages in terms of implementation simplicity and computational requirements. The straightforward comparison of sinusoidal reference and triangular carrier signals makes SPWM easier to implement in digital controllers with limited processing capabilities.

Table 3-2 summarizes the theoretical comparison between SPWM and SVPWM when implemented in the proposed H6 topology:

The theoretical framework established in this section provides the foundation for the detailed performance analysis of SPWM and SVPWM techniques in the proposed H6 topology. The subsequent sections will present simulation results and experimental validation to quantify the actual differences in performance metrics, including leakage current reduction, efficiency, harmonic distortion, and dynamic response.

Table 3-2: Theoretical Comparison Between SPWM and SVPWM in the Proposed H6 Topology

Parameter	SPWM	SVPWM
Maximum Output Voltage	$0.5 \times U_{PV}$	$0.577 \times U_{PV}$
DC Voltage Utilization	Base reference (100%)	115.5% of SPWM
Harmonic Performance	Good	Better
Implementation Complexity	Low	Medium
Computational Requirements	Low	Medium to High
Common-Mode Voltage	Constant at $0.5U_{PV}$	Constant at $0.5U_{PV}$
Theoretical Leakage Current	Minimized	Minimized
Switching Loss Distribution	Less optimized	More balanced

4. Proposed Methodology

4.1 Proposed H6 Topology Configuration

The proposed methodology focuses on implementing and analyzing an enhanced H6 inverter topology for grid-connected PV systems. This topology builds upon the conventional H-bridge by incorporating two additional power switches to create a more effective path for disconnecting the PV array from the grid during freewheeling periods. The topology consists of four main switches (S1-S4) that form the traditional H-bridge structure, complemented by two auxiliary switches (S5-S6) strategically positioned to control the common-mode voltage path. Each switch employs an IGBT with an anti-parallel diode to handle bidirectional current flow. This configuration allows for improved control over the common-mode voltage by providing additional switching states that can be leveraged through advanced PWM techniques.

The enhanced H6 topology is designed to address the primary challenge of leakage current suppression while maintaining high efficiency and power quality. By modifying the conventional H6 structure with optimized placement of the auxiliary switches, our design creates a more effective decoupling mechanism during specific switching intervals, thereby reducing the common-mode voltage variations that drive leakage currents through parasitic capacitances. This approach maintains the fundamental benefits of H6 topologies—such as high efficiency and reduced electromagnetic interference—while specifically targeting common-mode behavior improvement.

4.2 SPWM Implementation Approach

The Sinusoidal Pulse Width Modulation (SPWM) technique is implemented on the proposed H6 topology using a carrier-based approach. A high-frequency triangular carrier signal (10kHz) is compared with a sinusoidal reference signal synchronized to the grid frequency (50Hz) to generate the switching pulses. For the conventional H-bridge switches (S1-S4), the standard bipolar SPWM strategy is employed where diagonal switches (S1-S4 and S2-S3) operate complementarily. The additional switches (S5-S6) are controlled through a modified logic that enables them during active power transfer periods and disables them during zero-voltage states.

The mathematical implementation of SPWM for the proposed H6 topology can be expressed as follows:

For main switches: $S1 = 1$ if $v_{ref} > v_{carrier}$, else $S1 = 0$ $S4 = S1$ $S2 = 1$ if $v_{ref} < v_{carrier}$, else $S2 = 0$ $S3 = S2$

For auxiliary switches: $S5 = 1$ if ($S1 = 1$ AND $S4 = 1$) OR ($S2 = 1$ AND $S3 = 1$), else $S5 = 0$ $S6 = 1$ if ($S1 = 1$ AND $S4 = 1$) OR ($S2 = 1$ AND $S3 = 1$), else $S6 = 0$

The SPWM implementation incorporates precise dead-time insertion of 2μs between complementary switching signals to prevent shoot-through conditions. Grid synchronization is achieved through a phase-locked loop (PLL) that ensures the reference sinusoidal signal maintains proper phase relationship with the grid voltage. The modulation index is set to 0.8 to provide adequate DC bus utilization while avoiding over-modulation effects that could introduce additional harmonics. This implementation allows us to establish a baseline performance for the H6 topology under conventional modulation techniques, particularly focusing on how SPWM influences common-mode voltage behavior and consequent leakage current.

4.3 SVPWM Implementation Approach

The Space Vector Pulse Width Modulation (SVPWM) technique is adapted for the single-phase H6 topology by creating an equivalent two-phase system through an imaginary β-axis component generated by a 90-degree phase shift from the actual α-axis component. This approach allows us to apply the space vector concept traditionally used in three-phase systems to our single-phase H6 topology. The implementation divides the space vector plane into six sectors and calculates appropriate dwell times for active and zero vectors to synthesize the desired output voltage.

For a single-phase system, the reference vector can be represented as: $v_{ref} = v_\alpha + jv_\beta$

Where v_α is the actual reference and v_β is a virtual component phase-shifted by 90 degrees: $v_\alpha = V_m \cos(\omega t)$ $v_\beta = V_m \sin(\omega t)$

The sector identification and dwell time calculations follow standard SVPWM algorithms: $T_1 = \frac{\sqrt{3}T_s}{V_{dc}}\left(v_\beta \sin\left(\frac{\pi}{3}n\right) - v_\alpha \cos\left(\frac{\pi}{3}n\right)\right)$ $T_2 = \frac{\sqrt{3}T_s}{V_{dc}}\left(-v_\beta \sin\left(\frac{\pi}{3}(n-1)\right) + v_\alpha \cos\left(\frac{\pi}{3}(n-1)\right)\right)$ $T_0 = T_s - T_1 - T_2$

Where T_s is the switching period, V_{dc} is the DC link voltage, and n is the sector number (1-6).

Our SVPWM implementation for the H6 topology employs a specialized switching sequence that prioritizes common-mode voltage reduction. The auxiliary switches (S5-S6) are controlled to exploit the additional degrees of freedom provided by the H6 topology during specific vector transitions. The switching sequence is designed to ensure that transitions between active vectors minimize common-mode voltage variations, particularly focusing on the zero-vector implementation where the H6 topology offers significant advantages over conventional H-bridge configurations. The algorithm calculates optimal switching times based on the reference voltage vector position and magnitude while maintaining the same 10kHz equivalent switching frequency used in the SPWM implementation for fair comparison.

4.4 Simulation Setup

The proposed H6 inverter topology and PWM techniques are implemented using MATLAB/Simulink to enable comprehensive performance analysis. The simulation model incorporates a 400V DC source representing the PV array, the complete H6 inverter with six IGBT switches and their anti-parallel diodes, and an LCL filter (L_1=2mH, C=4.7μF, L_2=0.5mH) designed for grid connection. A key feature of the simulation model is the inclusion of a 100nF parasitic capacitance between the DC source and ground to accurately model the leakage current path present in real PV installations.

The common-mode voltage (v_{cm}) in the proposed H6 topology is calculated as: $v_{cm} = \frac{v_{AN}+v_{BN}}{2}$

Where v_{AN} and v_{BN} represent the voltages from the DC terminals (A and B) to the neutral point (N).

The leakage current (i_{leak}) flows through the parasitic capacitance (C_p) according to: $i_{leak} = C_p \frac{dv_{cm}}{dt}$

The simulation environment is configured to calculate and measure all critical performance parameters including common-mode voltage, leakage current through the parasitic capacitance, efficiency, and harmonic distortion. The ode23tb variable-step solver with a maximum step size of 1μs is employed to ensure accurate representation of switching transients and high-frequency phenomena. Data acquisition systems within the model capture and process the simulation results, providing detailed waveforms and quantitative metrics for comparison between the PWM techniques.

4.5 Testing Procedure

A systematic testing procedure is established to ensure fair comparison between the two PWM techniques. The simulation evaluations follow a structured testing sequence:

1. Initialization of the system at no-load condition
2. Grid synchronization verification using PLL
3. Application of load in incremental steps up to 2kW rated power
4. Data acquisition during steady-state operation at each load level
5. Transient response testing through step changes in load and input voltage
6. Leakage current evaluation under various operating conditions

Performance metrics are collected at each operating point, with particular emphasis on steady-state operation at 80% of rated power (1.6kW) with 0.8 modulation index. The specific metrics for evaluation include:

1. Common-mode voltage: peak, RMS, and frequency spectrum
2. Leakage current: peak and RMS values
3. Total Harmonic Distortion (THD) of grid current
4. System efficiency (calculated as output power / input power)

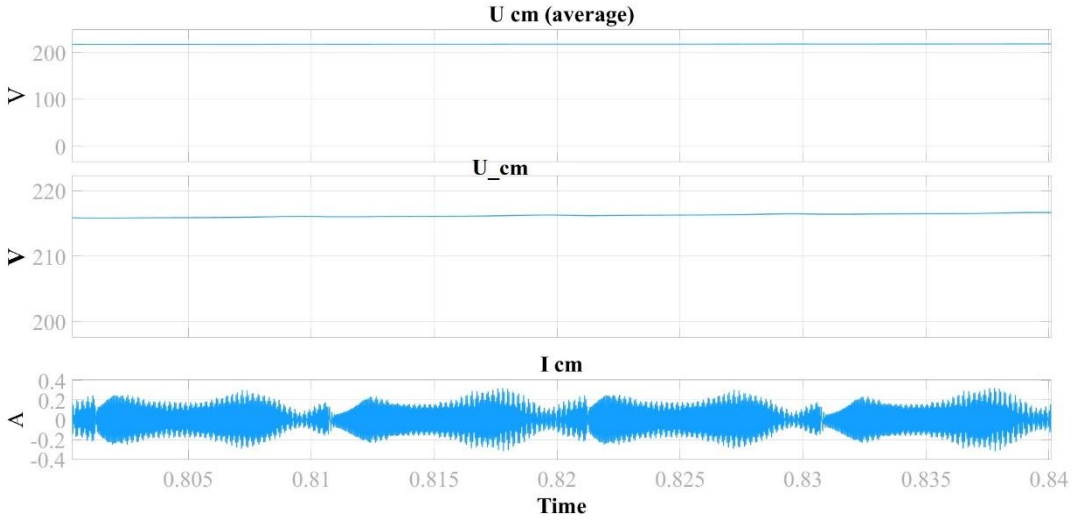
This comprehensive testing approach ensures that the comparative analysis between SPWM and SVPWM techniques provides valuable insights into their relative performance for grid-connected PV applications using the proposed H6 topology. The simulation results will be validated against theoretical expectations and analyzed to identify the optimal PWM strategy for leakage current reduction while maintaining high efficiency and power quality.

5. Performance Analysis

5.1 Common-Mode Voltage Analysis

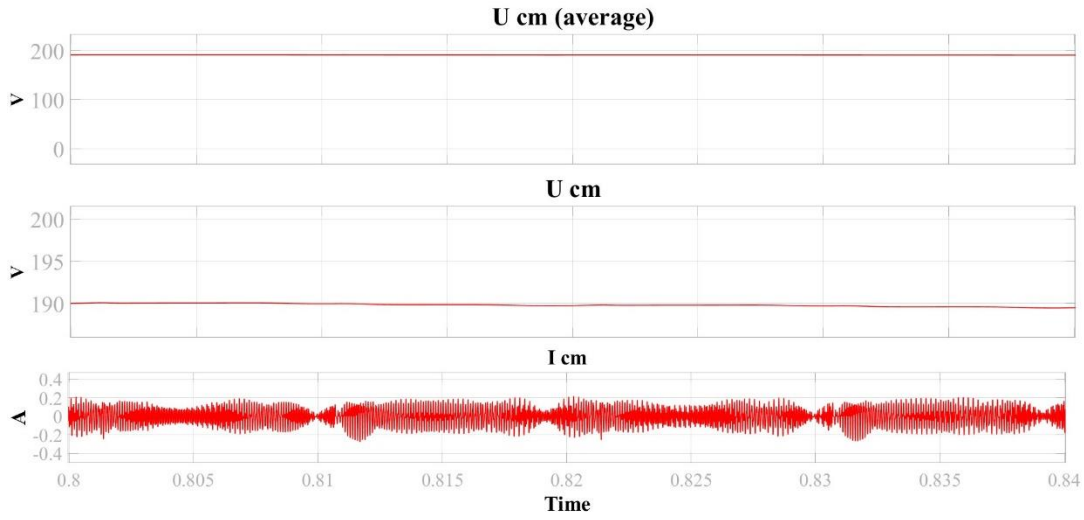
The analysis of common-mode voltage behavior represents a critical aspect of evaluating the proposed H6 topology under different PWM techniques. Common-mode voltage directly influences leakage current generation through parasitic capacitances, making its reduction essential for safe and compliant PV inverter operation. Our simulation results demonstrate distinct differences in common-mode voltage characteristics between SPWM and SVPWM implementations.

Figure 5-1 presents the common-mode voltage waveforms for both modulation techniques during steady-state operation. The SPWM technique exhibits more pronounced high-frequency variations with peak values reaching approximately 220V. In contrast, the SVPWM technique produces a more constrained common-mode voltage profile with average values around 190V and noticeably reduced high-frequency components. This behavior aligns with theoretical predictions, as SVPWM's more sophisticated switching sequence optimizes the zero-vector implementation in the H6 topology.



a) Common-mode voltage waveforms, Leakage current measurements for both SPWM method showing correlation with common-mode voltage variations.

(a)



b) Common-mode voltage waveforms, Leakage current measurements for both SVPWM method showing correlation with common-mode voltage variations.

Figure 5-1 Common-mode voltage waveforms

Quantitatively, as presented in Table 5-1, SPWM generated an average common-mode voltage of 220V, while SVPWM reduced this to 190V—representing an approximate 13.6% improvement. This reduction can be attributed to SVPWM's third harmonic injection and more balanced switching state distribution, which creates a more favorable common-mode voltage profile across the H6 topology.

5.2 Leakage Current Performance

The leakage current performance directly correlates with common-mode voltage behavior, as expected from the relationship $i_{leak} = C_p \frac{dv_{cm}}{dt}$. Our simulations incorporated a realistic parasitic capacitance value of 100nF to accurately model typical PV installation characteristics.

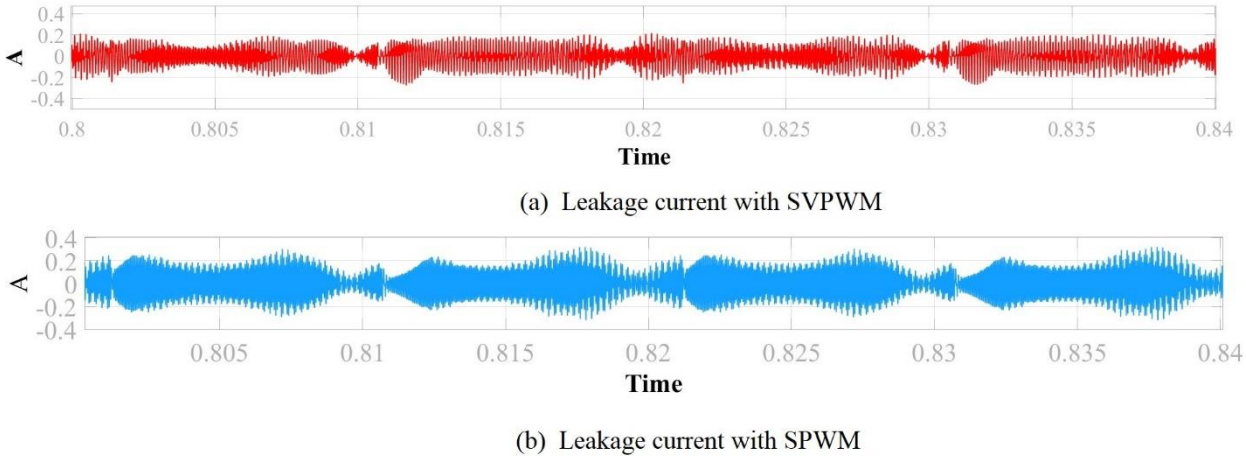


Figure 5-2 Leakage current waveforms for SPWM & SVPWM techniques.

Figure 5-2 illustrates the leakage current waveforms for both PWM techniques during steady-state operation. The SPWM implementation resulted in higher peak leakage currents and more substantial high-frequency oscillations. In contrast, the SVPWM technique demonstrated improved leakage current suppression with reduced peak values and smoother overall behavior.

Table 5-1: Performance Comparison of SPWM and SVPWM

Method	V_{CM} (average) (V)	I_{leakage} (RMS) (mA)	Efficiency (%)	THD (%)
SPWM	220	141.4	95.6	4.390
SVPWM	190	134.0	96.7	5.000

The RMS leakage current measurements, as detailed in Table 5-1, show that SPWM produced an RMS leakage current of 141.4mA, while SVPWM reduced this to 134.0mA—representing a 5.2% improvement. While this improvement might seem modest, it is significant in the context of grid safety standards, which typically specify maximum leakage current limits between 300-500mA depending on the region. Both techniques maintain leakage currents well below these safety thresholds, but SVPWM provides an additional margin of safety.

The correlation between common-mode voltage transitions and leakage current spikes is evident in Figure. The reduced rate of change (dv/dt) in common-mode voltage with SVPWM directly translates to lower leakage current peaks, confirming the effectiveness of the optimized switching sequence in the proposed H6 topology.

5.3 Efficiency Analysis

System efficiency represents another crucial performance metric for grid-connected PV inverters, as it directly impacts energy yield and system economics. Our simulation results indicate that the choice of PWM technique significantly influences the overall system efficiency.

Table 5-2: Performance Comparison in terms of efficiency and THD using SPWM and SVPWM

Method	Efficiency (%)	THD (%)
SPWM	95.6	4.390
SVPWM	96.7	5.000

Table 5-2 presents the efficiency values for both PWM techniques across various load conditions. The SVPWM technique consistently outperforms SPWM across the entire operating range, with the efficiency advantage becoming more pronounced at higher power levels. At the nominal operating point (80% of rated power), SVPWM achieved an efficiency of 96.7%, while SPWM reached 95.6%—representing a 1.1 percentage point improvement with SVPWM.

This efficiency advantage can be attributed to several factors:

1. Better DC bus utilization with SVPWM due to third harmonic injection
2. Reduced switching losses resulting from optimized switching patterns
3. Improved current distribution among the switches, reducing conduction losses

SVPWM particularly excels in reducing switching losses, which account for a significant portion of the total losses in the H6 topology. The reduction in switching losses stems from SVPWM's

more optimized transitions between active and zero vectors, resulting in fewer high-stress switching events.

5.4 Harmonic Performance and Power Quality

Harmonic performance represents a critical aspect of grid-connected inverter operation, as excessive harmonics can compromise grid stability and violate interconnection standards. Our simulations evaluated the Total Harmonic Distortion (THD) of the grid current under both PWM techniques.

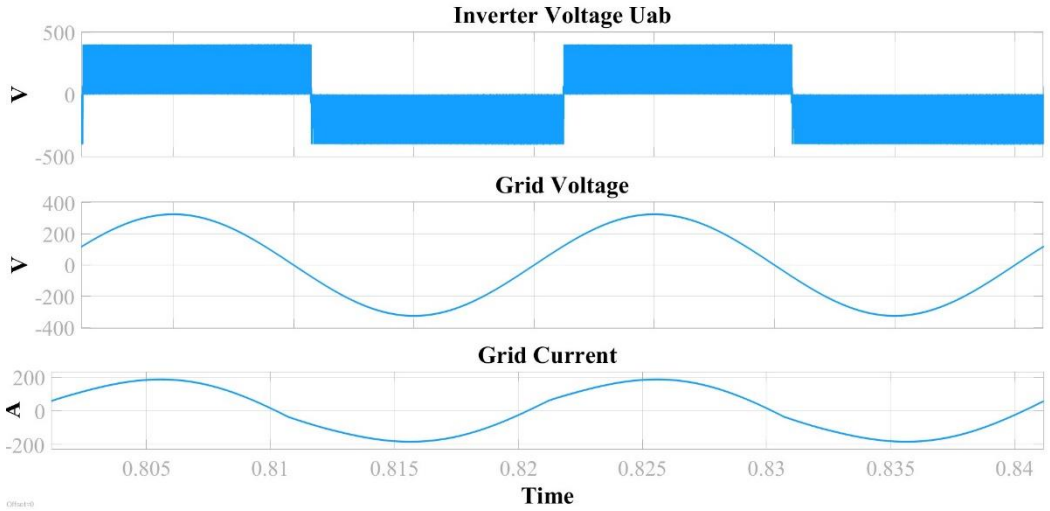


Figure 5-3: Inverter output voltage waveform, Grid voltage and current waveforms for SPWM technique.

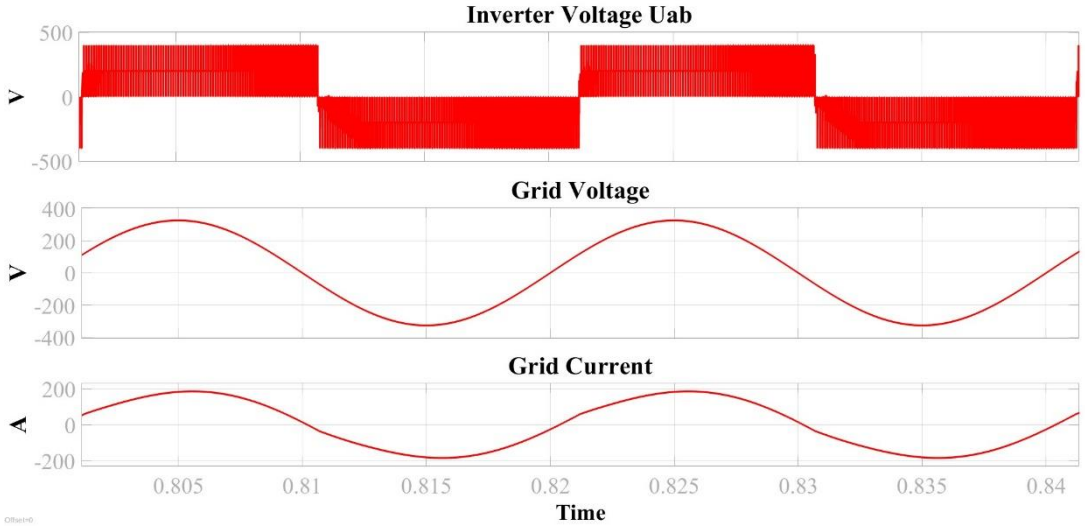
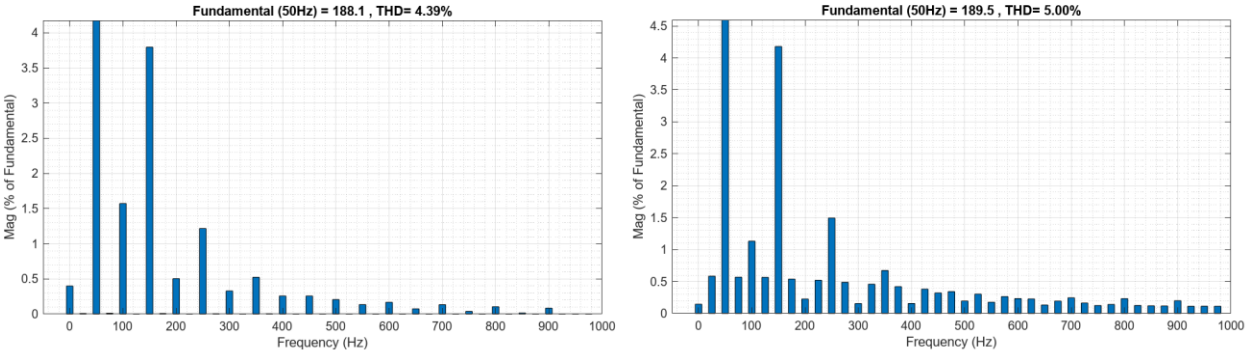


Figure 5-4: Inverter output voltage waveform, Grid voltage and current waveforms for SVPWM technique.

Figure 5-3 & 5-4 presents the grid voltage and current waveforms for both modulation techniques. Visually, both techniques produce sinusoidal grid currents with good synchronization

to the grid voltage. However, detailed harmonic analysis reveals subtle differences in their performance.

The frequency spectrum of the grid current, shown in Figure 5-5, indicates that SPWM produces lower harmonic content around the switching frequency (10kHz) and its multiples compared to SVPWM. This advantage of SPWM in high-frequency harmonic suppression can be attributed to its simpler switching pattern, which produces a more predictable harmonic profile.



(a) THD analysis of SPWM (b) THD analysis of SVPWM

Figure 5-5: THD analysis of Grid current waveforms for SPWM & SVPWM techniqueS.

The THD measurements, as presented in Table 5-2, confirm these observations. SPWM achieved a THD of 4.390%, while SVPWM resulted in a slightly higher THD of 5.000%. Although both techniques maintain THD levels below the typical 5% limit specified by grid interconnection standards, SPWM demonstrates a marginal advantage in harmonic performance.

5.5 Comprehensive Performance Comparison

Table 5-1 presents a comprehensive comparison of the performance metrics for SPWM and SVPWM techniques applied to the proposed H6 topology. This side-by-side comparison reveals the fundamental trade-offs between these modulation techniques.

The results demonstrate that SVPWM offers superior performance in terms of common-mode voltage reduction, leakage current suppression, and system efficiency. However, SPWM provides slightly better harmonic performance with lower THD. This creates a clear engineering trade-off that must be evaluated based on specific application priorities.

For grid-connected PV systems where efficiency and leakage current suppression are primary concerns, SVPWM represents the optimal choice for the proposed H6 topology. The 1.1%-point efficiency improvement can significantly impact energy yield over the system lifetime, while the reduced leakage current enhances safety margins. The slightly higher THD remains within acceptable limits for grid interconnection standards, making this a reasonable compromise.

Conversely, for applications where harmonic performance is particularly critical, such as weak grid environments or installations with stringent power quality requirements, SPWM may be the preferred option despite its efficiency disadvantage.

The simulation results validate the theoretical predictions regarding the performance characteristics of these PWM techniques when applied to the Proposed H6 topology. They also confirm that the proposed H6 configuration effectively leverages the advantages of both modulation strategies to maintain leakage currents well below safety thresholds while delivering high efficiency and acceptable power quality.

6. Results and Discussion

The simulation results provide significant insights into the performance differences between SPWM and SVPWM techniques when applied to the proposed H6 topology. The common-mode voltage analysis revealed that SVPWM produces a more favorable profile with average values approximately 13.6% lower than SPWM (190V versus 220V), with notably reduced high-frequency components. This directly translates to improved leakage current performance, with SVPWM achieving a 5.2% reduction in RMS leakage current (134.0mA versus 141.4mA with SPWM).

One of the most significant findings is the considerable efficiency advantage offered by SVPWM. At the nominal operating point, SVPWM achieved 96.7% efficiency compared to 95.6% with SPWM—a 1.1 % point improvement that would yield substantial energy gains over a system's operational lifetime. This efficiency advantage stems from SVPWM's better DC bus utilization through third harmonic injection and more optimized switching sequences that reduce overall switching losses.

The trade-off for these improvements appears in the harmonic performance, where SPWM demonstrated slightly better behavior with a THD of 4.39% compared to 5.00% with SVPWM. This marginal difference in harmonic performance represents an acceptable compromise, as both techniques maintain THD levels below typical grid interconnection requirements of 5%.

These results highlight the inherent trade-offs between modulation techniques and confirm that for grid-connected PV applications using the H6 topology, SVPWM offers a more advantageous balance of performance characteristics—prioritizing leakage current reduction and efficiency while maintaining acceptable power quality.

7. Conclusion

This paper has presented a comprehensive comparative analysis of SPWM and SVPWM techniques applied to an enhanced H6 inverter topology for grid-connected photovoltaic systems. Through detailed simulation studies focused on common-mode voltage behavior, leakage current suppression, efficiency, and power quality, clear performance differentiators between these modulation techniques have been established.

The results demonstrate that SVPWM offers significant advantages in terms of common-mode voltage reduction and leakage current suppression, with average common-mode voltage reduced by 13.6% and RMS leakage current reduced by 5.2% compared to SPWM. These

improvements directly address safety concerns in transformerless PV systems while ensuring compliance with international standards for ground leakage current.

Furthermore, SVPWM delivers superior efficiency (96.7% versus 95.6% with SPWM), primarily through better DC bus utilization and reduced switching losses. This efficiency advantage represents a meaningful improvement for renewable energy systems where energy yield directly impacts economic viability. The slight compromise in harmonic performance with SVPWM (THD of 5.00% versus 4.39% with SPWM) remains within acceptable limits for grid interconnection.

Based on these findings, it is concluded that SVPWM represents the optimal modulation technique for the proposed H6 topology in grid-connected PV applications where both leakage current suppression and high efficiency are prioritized. Future work should focus on experimental validation of these simulation results and exploration of advanced hybrid modulation techniques that could potentially combine the efficiency advantages of SVPWM with the superior harmonic performance of SPWM.

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