Optimized IC Design for Low-Power, High-Speed Computing Using GDI-Based Carry Look-Ahead Adders

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Abstract

Increased demands for greater power efficiency, compactness, energy efficiency, and speed have resulted from the widespread usage of electronic devices, such as computers, laptops, mobile phones, and tablets. In order to satisfy user expectations, engineers, designers, and developers must take these factors into consideration. Ripple carry adders, carry choose adders, carry skip adders, carry look-ahead adders, carry increment adders, carry save adders, and carry bypass adders are among the different types of adder designs that are available. The Ripple carry adder has a limited computation speed despite its tiny size. Carry look-ahead and Carry select adders, on the other hand, provide better performance. Designers must pay attention to factors including delay time, power consumption, and occupied area in order to produce integrated circuits (ICs) that are fast, low-power, and space-efficient. To lower power consumption and increase performance speed, many logic styles are used, such as pass transistor logic (PTL), dual rail domino logic, pseudo NMOS logic, dynamic CMOS, and static CMOS. The Gate Diffusion Input (GDI) technique is one of these approaches that is particularly effective at lowering transistor counts, propagation delays, and power consumption in digital circuits. PTL logic does, however, provide certain output degradation problems. This work purposefully uses the GDI technique to design the logic gates required to implement a Carry look-ahead adder in order to solve these difficulties. Low power consumption, short latency times, energy efficiency, and fewer transistors are the goals of this strategy.

Keywords: Adders, Carry Look-Ahead Adder, PTL, CMOS, GDI, Tanner EDA, Low-Power IC Design, High-Speed Performance, Energy Efficiency.

1. Introduction

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. While performance and Area remain to be the two major design tolls, power consumption has become a critical concern in today's VLSI system design[]. The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on

demand or application some compromise between constraints has to be made. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. In 2002, a new concept of hybrid adders is presented to speed up addition process by Wang et al. that gives hybrid carry look-ahead/carry select adders design. In 2008, low power multipliers based on new hybrid full adders is presented.

2. Literature survey

Khan, Burhan, and Suraj Pattanaik (2020) [1] proposed that pass transistor logic is a better way to implement circuits for high-speed and low-power applications in less number of transistors. Parameters like delay, power consumption, and energy are reduced so much as compared to available logic styles such as static CMOS logic, DOMINO logic, and sub-threshold regime logic. Hasan, Mehedi (2021) [2] proposed to inspect performance in wide word length adder structure, the 4-bit CLA architectures (proposed and existing) are extended to 16-bits using Carry-Select Adder (CSA) architecture. Both as 4-bit cell and extended 16-bit structure, the proposed 4-bit CLA shows remarkable improvement in speed while maintaining quite acceptable level of power consumption. As a result, the proposed 4-bit CLA can be utilized as a highly suitable substitution of the existing 4-bit CLA architectures in high-speed microprocessor design.Dipto, Md Ashik Zafar, et al.(2020) [3]. This paper developed on reducing power, delay and transistor count in Conventional Static CMOS based 4-bit Carry Look Ahead adder. The conventional static CMOS XOR and gates are replaced by Gate Diffusion Input technique and Pass Transistor logic based XOR and AND gates in the input side to enhance performance parameters and to reduce transistor count. Two new modified CLA adder have been proposed and their performance parameters have been compared with conventional circuit using Tanner simulation tools. The proposed designs showed significant performance improvement while keeping the advantages of static CMOS Logic.El-Bendary, Mohsen AM, and Ayman Haggag(2021) [4] This work proposed several logic circuits for Different metrics are utilized for evaluating the performance of the implemented CLA circuits. The simulation experiments results prove the superiority of the proposed FA implementation which consists of 23 transistors only compared to the previously CLAs circuits design by the various design style. The implementation of the presented CLA design achieves reducing the consumed power, optimizing the processing time, and area of the implemented CLA circuits. Hossain, Muhammad Saddam, and Farhadur Arifin(2020) [5] This paper provided method towards the improved performance parameters of conventional CMOS based 4-bit carry look-ahead adder. Conventional CLA adder has high numbers of transistors and high input impedance due to which various performance aspects are affected. Due to high input impedance, its delay and power consumption are high. Therefore, to increase the performance and to reduce delay, we have proposed an advanced version of CLA adder where hybrid logic based XOR gate and GDI AND gates have been used as input to reduce the transistor count as well as to improve performance. Finally, performance of modified adder has been compared with the conventional CLA adder..Bhatt, Uttara, et al(2019) [6]. This paper proposed an eight-bit carry select adder utilizing four bit carry look ahead adders as the individual stages. Further, the carry look ahead adders have been implemented using three MOS circuit design styles, Static, Dynamic (MODL) and Pass Transistor logic.Putra, Adiwena, and Trio Adiono(2021) [7] This paper provided a full custom design of a 4-bit ANN processing element, implemented using 120 nm technology. The processing element consists of register, adder, and multiplier. The register is implemented using push-pull D flip-flop architecture,Jhamb, Mansi(2021[8] present a Carry select adder using multiplier and adder circuits. In proposed designs, extra circuitry is eliminated and leads to a reduction in 43.995% of power consumption, 93.912% of time delay, and 97.515% of energy. The transistor count of the proposed

carry select adder is 61.788% less than that of the conventional carry select adder. The power, delay, energy of it has been compared with state-of-art carry select adder. This advanced circuit of adder shows highly efficient and reliable performance Ahmed, Rekib Uddin, and Prabir Saha.(2021) [9]. This paper provided an implementation aspect of popular multi-bit adders (e.g. ripple carry adder (RCA) and carry look ahead adder (CLA)) through UTBSOI transistors. Performance parameters comparison in terms of power consumption, delay, power-delay product (PDP), and energy-delay product (EDP) have been analysed for the application of the intelligent systems. Chauhan, Anurag, et al.(2021) [10]. In this paper, they presented a four bit arithmetic logic unit which is energy efficient and temperature invariant implemented using the dual mode pass transistor logic. The basic logic gates such as NOR and NAND are designed using both CMOS logic and dual mode pass. Bhuyan, Muhibul Haque, Md Mahfuz Ahmed, and Shafiul Alam Robin.(2021) [11] proposed design and simulation of a 4-bit CMOS based full adder circuit at various technology nodes usingMicrowind and DSch are presented. After that performances are compared to see how the reduction oftransistor size can help to achieve those benefits. The designed circuit is used for the addition of 4-bit binarynumbers. To design a 4-bit full adder fully automatic CMOS design process is used. In the first fully CMOSdesign, schematic and layout of a 4-bit full adder are developed. The layouts are designed and simulated at 90nm, 65 nm, and 45 nm technology nodes. It has been observed from the simulated results andvarious outputsthat the reduction of node sizes improves the performances of the digital integrated circuit.Deepthi, Kummetha, et al(2021) [12]. This paper demonstrated using Brent Kung adder (BK) which optimizes the design constraints like speed, area, and power compared to all other adders mentioned. RCA, CLA, regular linear Brunt Kung carry select adder (RL BKCSA), and modified square root (MSQRT) Brent Kung CSA are designed in Xilinx.Kumari, M. Meena, Bhaskara Rao Doddi, and G. Sunil Kumar(2018)[13] This paper proposed Carry look ahead adder with low area and low power. They have designed xor and xnor cells in which it generates two outputs. Xor outputs the xor and nor logic whereas xnor outputs the xnor and nand logic.We can design adder by efficiently utilizing the hardware required for sum logic to the carry logic. But the choice of using only xor or only xnor or combination of both for designing sum logic has considerable impact on the hardware requirements of the carry logic. Total transistor count for proposed 4 bit carry look ahead adder is 164 with existing design transistor count of 236.Chu, Shunan(2022) [14 The analysis results show that the conventional 4-bit adder structure can be improved by designing the carry term Field Effect Transistor (FET) network and replacing the existing gate circuit with a hybrid Gate diffusion technology (GDI) gate, which can reduce the number of transistors and the design circuit area. They also contribute to improving the power consumption, delay, power delay product (PDP) and other performance parameters. Johari, Ayoush, Aparna Gupta, and Rita Jain(2017) [15].. This paper provided carry-look ahead adder calculated one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. Carry Propagator and Carry Generator FFT results are compared in terms of their amplitude, phase and group delays

3.Proposed Mythology

The GDI contains three inputs: G (common gate input of both the nMOS and the pMOS), P (input to the source/drain of the pMOS), and N (input to the source/drain of the nMOS). It was shown that multiple Boolean functions can be implemented by a simple GDI cell, as demonstrated in Figure 1. This is achieved by a change of the input configuration of the GDI cell. While implementation of most of these functions is relatively complex (6–12 transistors) in Static CMOS, it is very efficient (only 2 transistors) with the GDI cells. The Multiplexer (MUX) is the most complex function that can be implemented with a basic GDI cell, while being the most efficient function as compared to CMOS implementation. GDI gates may suffer from threshold voltage drops which reduce current drive and

therefore affect the performance of the gate. These drops also increase direct-path static power dissipation in the cascaded inverters, used for swing restoration. It was shown that these effects can be significantly reduced by using swing restoration buffers with a multiple VTH approach, herein named MVT. This approach suggests using low threshold transistors in all paths where a voltage drop is expected. This way, the voltage drop at the output will be minimal. In addition, all regenerative inverters are implemented using high threshold transistors. This combination allows minimization of the direct path static power in the inverters. Most of today's static digital designs are based on CMOS NAND and NOR gates. The reasons for this are known and well explored. Both NAND and NOR gates are implemented using only four transistors and each one of these functions is a universal set. The GDI method, which is very efficient for implementation of various gates, such as MUX, AND, OR (see Table 1), has similar number of transistors in NAND/NOR gates implementation as standard CMOS methodology. However, the GDI technology provides alternative basic functions, F1 and F2. Consisting only of two transistors (one GDI cell), each one of these functions represents a universal set. Moreover, F1 and F2 functions can be used to synthesize other functions more efficiently than the NAND and NOR gates.

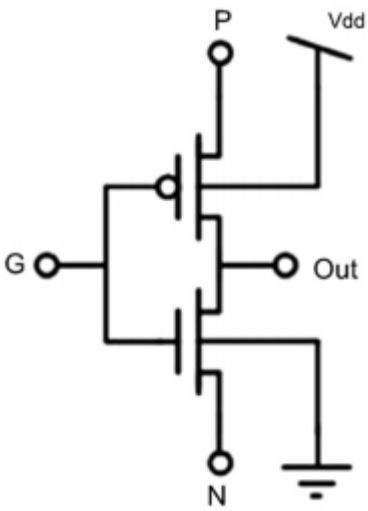

Figure 1. Basic GDI cell.

Table 1: Boolean function synthesis through input configuration of a simple GDI cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

3.1 GDI based CLA

The basic adder which first comes to mind is Ripple carry adder. But it has some limitation; that is the propagation delay to calculate the carry bit. It takes too much time to propagate the carry. To overcome this type of limitation, Carry look-ahead adder comes into consideration which calculates the carry bit in advance based on the input values given to the adder. To understand the working

principle of Carry look-ahead adder, let us see the modified Boolean expressions for propagate P and generate G as shown in Figure 2 and Figure 3.

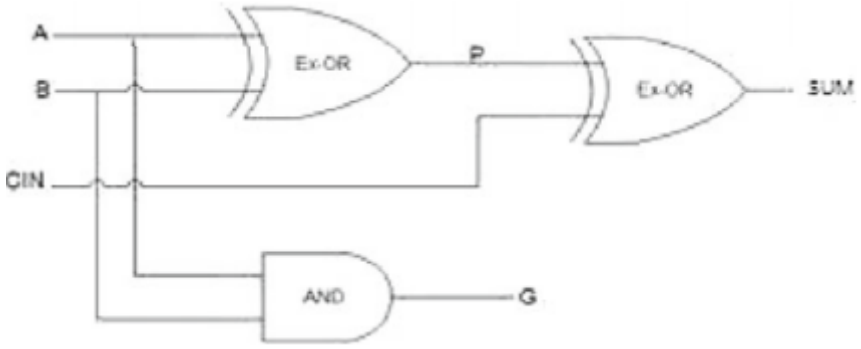

Figure 2. Gate-level representation of B-cell

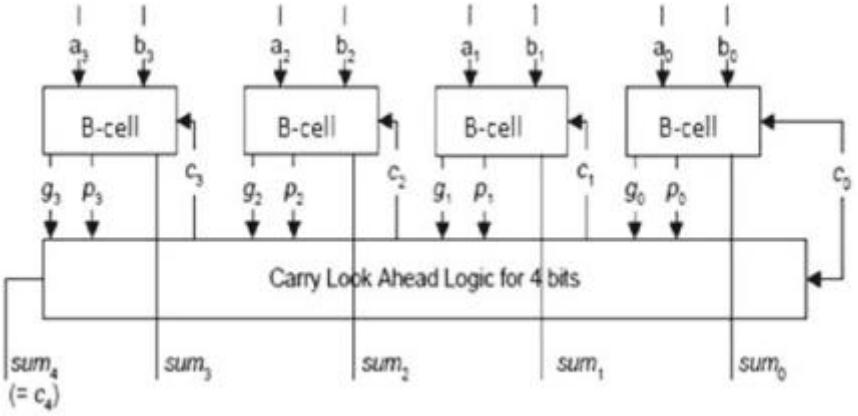

Figure 3. Block diagram of 4-bit CLA

$$Pi = ai \oplus bi \quad (1)$$

$$Gi = ai \cdot bi \quad (2)$$

For 4-bit CLA Summations are given from Eqs. 3–6 as follows:

$$Sum0 = a0 \oplus b0 \oplus c0 \quad (3)$$

$$Sum1 = a1 \oplus b1 \oplus c1 \quad (4)$$

$$Sum2 = a2 \oplus b2 \oplus c2 \quad (5)$$

$$Sum3 = a3 \oplus b3 \oplus c3 \quad (6)$$

Carry-out are given from Eqs. 7–10 as follows

$$c1 = g0 + p0 \bullet c0 \quad (7)$$

$$c2 = g1 + p1 \bullet g0 + p1 \bullet p0 \bullet c0 = g1 + p1\ g0 + p0 \bullet c0 = g1 + p1 \bullet c1 \quad (8)$$

$$c3 = g2 + p2 \bullet g1 + p2 \bullet p1 \bullet g0 + p2 \bullet p1 \bullet p0 \bullet c0$$

$$= g2 + p2\ g1 + p1 \bullet g0 + p1 \bullet p0 \bullet c0 = g2 + p2 \bullet c2 \quad (9)$$

$$c4 = g3 + p3 \bullet g2 + p3 \bullet p2 \bullet g1 + p3 \bullet p2 \bullet p1 \bullet g0 + p3 \bullet p2 \bullet p1 \bullet p0 \bullet c0 = g3 + p3\ g2 + p2 \bullet g1 + p2 \bullet p1 \bullet g0 + p2 \bullet p1 \bullet p0 \bullet c0 = g3 + p3 \bullet c3 \quad (10)$$

4. Results and Discussion

By using the basic gates such as Inverter, AND gate, OR gate, and EX-OR gate which have been designed earlier based on GDI, let us design the B-cell first and then by using B-cells we can easily construct our proposed 4-bit CLA circuit as shown in Figure 4, 5, 6, and Figure 7.

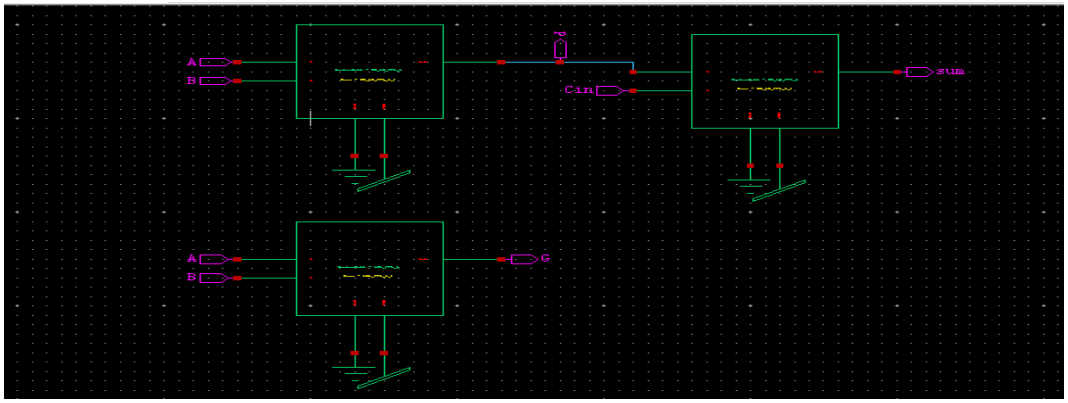

Figure 4. Schematic diagram of B-cell

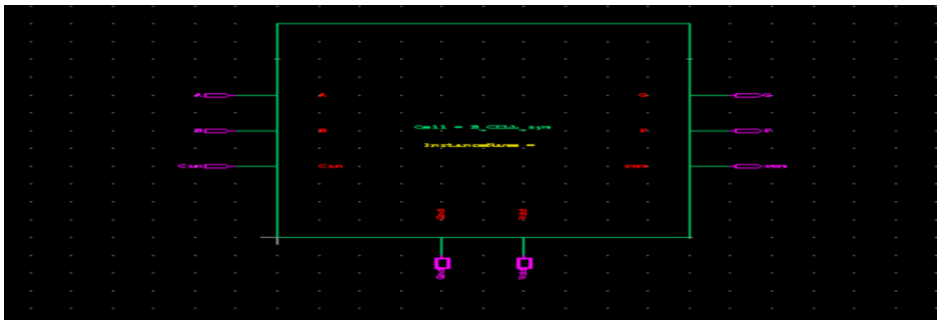

Figure 5. Symbolic representation of B-cell

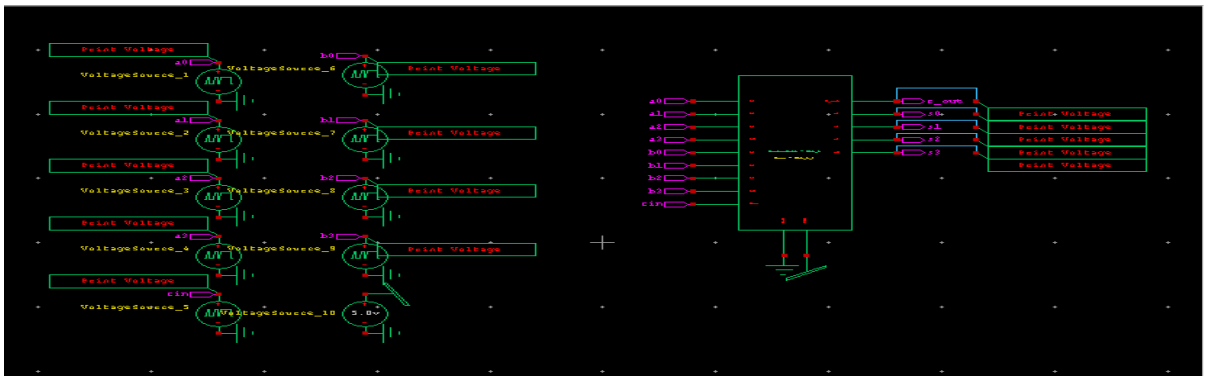

Figure 6. Symbolic representation of 4-bit CLA

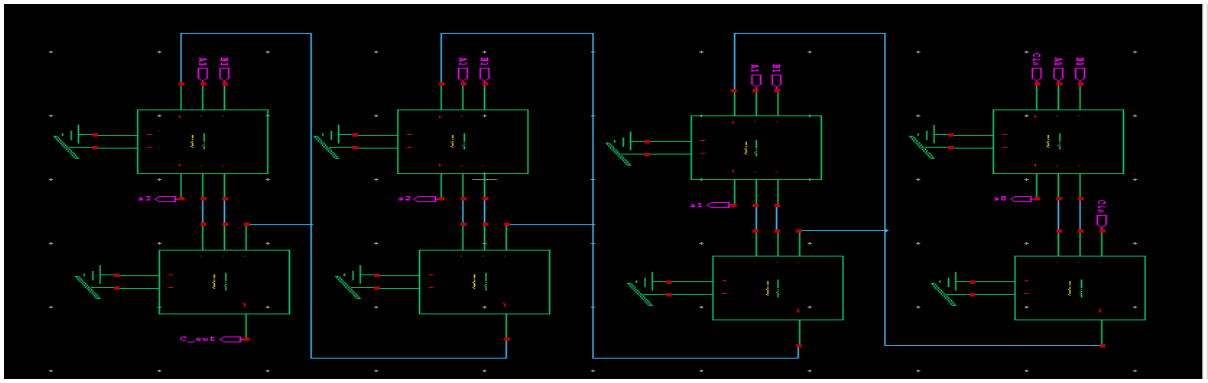

Figure 7. Schematic diagram of 4-bit CLA by using B-cells using GDI

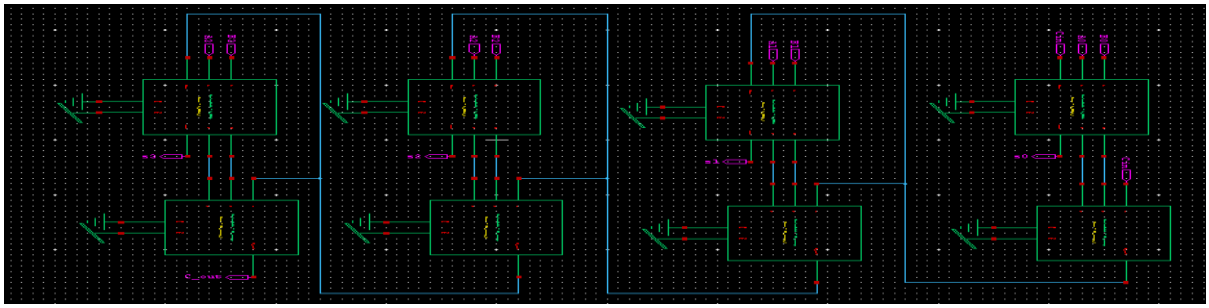

Figure 8. 4-bit CLA Adder

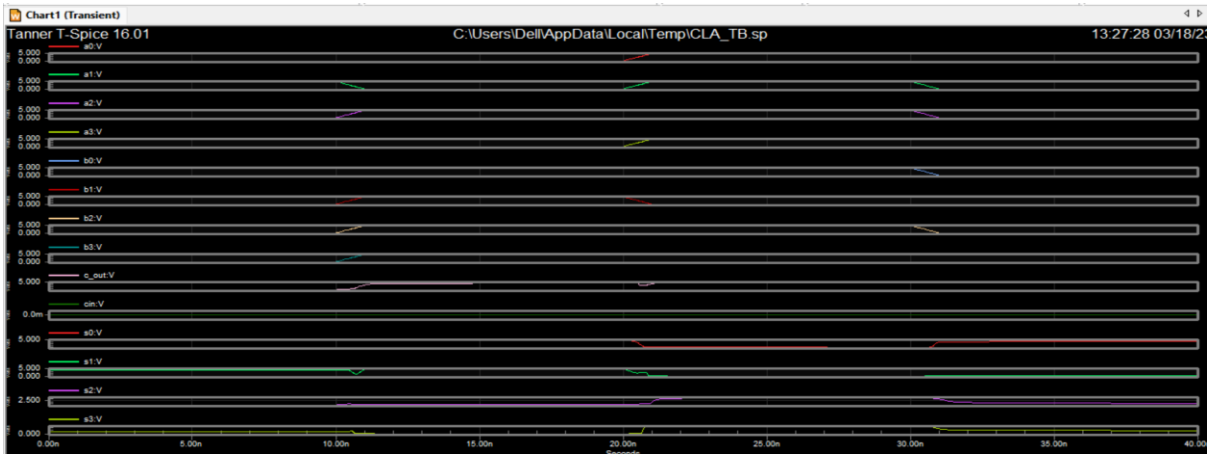

Figure 9. Output wave of 4- CLA Adder

Table 1 Comparison table

Technology	Area	Power(milli watts)
GDI	56	0.0168
PTL	80	157

5. Conclusion

From the above comparison tables, it is concluded that the GDI is the best logic among all other logic style available to design Carry look-ahead adder with a smaller number of transistor, fast performance, and more accurate with low power consumption. The delay, power, energy, PDP, and

EDP also decrease as compared to other available designs.

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