Power-Aware VLSI Design Using Multi-Threshold CMOS Technology

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Abstract- in CMOS rationale circuits, the decrease in the threshold voltage because of voltage scaling prompts increment in the sub limit spillage current and henceforth static power dispersal. In spite of the fact that power utilization is critical for current VLSI outline, operation speed and possessed territory are as yet the principle necessities of the VLSI plan. Multi limit voltage CMOS (MTCMOS) innovation is a decent arrangement which gives a superior and low-control Design with no range overhead. The downsizing of innovation in CMOS circuits brings about the down scaling of edge voltage consequently expanding the sub-limit spillage current. An IC comprises of many circuits of which a few circuits comprises basic way like full snake, while a few circuits like multiplexer and decoder has no predetermined basic way.

Keywords – CMOS, Low Power, Voltage, VLSI, multiplexer & Decoder, Low Control Design.

INTRODUCTION

Since the innovation of the primary Integrated Circuit (IC), silicon innovation downsizing keeps on taking care of the expanding requests for higher usefulness and better execution at a lower cost[1]. Power dissemination, however not by any stretch of the imagination overlooked, has been of little worry as of not long ago. The advances in VLSI incorporation innovation have made it conceivable to put an entire System on a Chip (SoC) which encourages the improvement of compact frameworks[2]. Versatile battery controlled applications, for example, scratch pad PCs, mobile phones, Personal Digital Assistants (PDAs), and military types of gear profile control dissemination as a basic parameter in advanced VLSI outline. Downsizing of edge voltage Vt brings about exponential increment of the sub edge spillage current. It can be seen from Fig.1 that the spillage control is less contrasted with the dynamic power for 180nm innovation[3]. At the point when the innovation scaling achieved 65nm, the spillage control practically rose to the dynamic power. Thus, productive spillage control diminishment strategies are extremely basic for the profound submicron and nanometer circuits. Despite the fact that power utilization is essential

for current VLSI outline, operation speed and involved range are as yet the primary necessities of the VLSI plan[4].

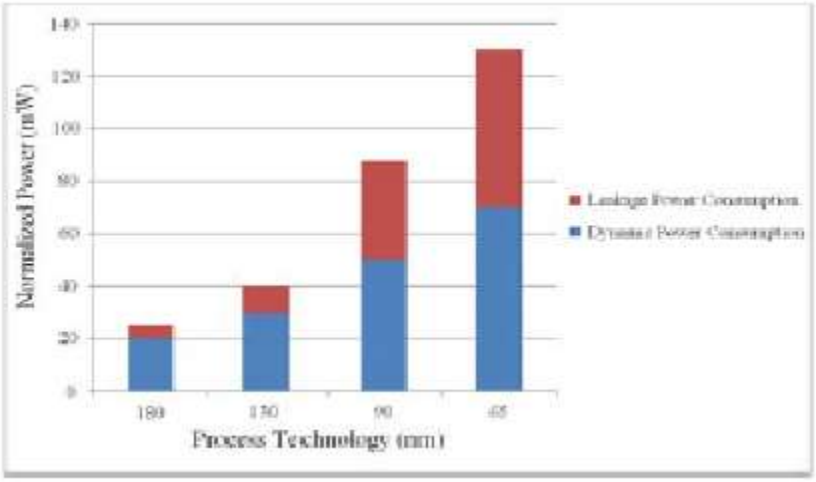

Figure 1- Leakage and dynamic power consumption with technology scaling[5]

RELATED WORK

Numerous systems have been appeared to conquer the spillage control issue in the nano scale innovation, yet those strategies have tradeoff between region, delay and furthermore dynamic power. Some of those procedures are as depicted in this area[5].

This is one of the methods proposed for spillage lessening, which kills the gadget by removing the supply voltage. Massive NMOS as well as PMOS gadget called rest transistor is utilized as a part of a way between supply voltage and ground, making virtual power and ground rails in the circuit . This makes a negative impact on the exchanging pace of the circuit when the circuit is working in dynamic mode[6]. Extra equipment is expected to recognize the sit out of gear areas of the circuit and the era of the rest flag. Notwithstanding when the circuit is in a sit out of gear express, this extra equipment expends control all through the circuit operation to control the rest transistors and ceaselessly screen the circuit state [7].

Constrained stacking presents an extra transistor for each contribution of the door in both N-system and P-arrange. This guarantees two transistors are OFF rather than one for each OFF-contribution of the door and thus makes a critical investment funds on the spillage current. Be that as it may, the stacking prerequisite for each information presented by the constrained stacking lessens the drive current of the entryway essentially. This outcomes in an adverse effect on the speed of the circuit[8].

CIRCUIT DESIGN WITH MTCMOS TECHNOLOGY

MTCMOS innovation gives an answer for the elite and low power outline prerequisites of present day plans. MTCMOS innovation gives the transistors that have low, ordinary and high limit voltage . This innovation is a successful circuit level system that gives an elite and low-control configuration by using both low and high limit voltage transistors [9]. Low-edge voltage transistors have rapid execution however high-control utilization. High-limit voltage transistors have low-control utilization however low speed execution. While the low-limit voltage transistors are utilized to lessen the proliferation defer time in the basic way, the high-edge voltage transistors are utilized to diminish the power utilization in the most brief way [10]. This paper portrays a low-

power and rapid outline for full viper, 4-bit swell convey snake and 4×4 multiplier circuits with MTCMOS innovation [11].

(i) Plan of full snake- When we include three bits A, B and Cin (input convey), at that point the Boolean capacity of the total and convey are given as

Sum = A B

Convey = AB + (A B) Cin

Fig. 2 demonstrates the rationale outline of 1-bit full viper cell. The full snake contains 3 inputs (A, B, Cin) and 2 yields (Sum and Carry). For the full viper circuit, convey way is the longest way and whole way is the most brief way. We utilize low-edge voltage transistors, ordinary edge voltage transistors and high-edge voltage transistors in the circuit outline [12]. Since convey way is the longest way in the circuit, the low-limit voltage transistors are utilized as a part of this way to diminish the spread postpone time in the basic way. The second selective OR door display in the aggregate way is outlined with high-edge voltage transistors to decrease the power utilization in the most limited way. The remaining AND door is composed with ordinary limit voltage transistor [13].

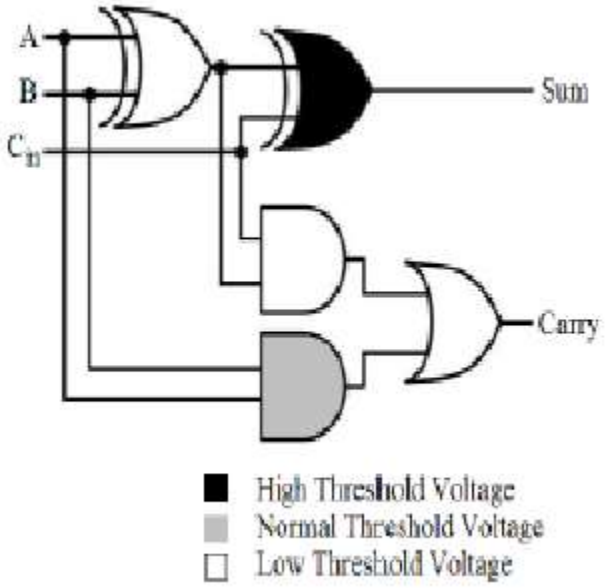

Figure 2- Logic diagram for 1-bit full adder

ECTOR AND MTCMOS TECHNIQUES

An IC comprises of many circuits of which a few circuits have basic way, while a few circuits have no predetermined basic way. LECTOR method is utilized to configuration circuits with no basic way and MTCMOS procedure is utilized to configuration circuits with basic ways [14].

(i) LECTOR technique and its applications- The Leakage Control Transistor (LECTOR) procedure depends on the viable stacking of transistors in the way from supply voltage to ground. The thought behind this system from is that "a state with more than one transistor OFF in a way from supply voltage to ground is far less cracked than a state with just a single transistor OFF in any supply to ground way." In this strategy, for each CMOS entryway, two spillage control transistors (LCTs) were presented, a PMOS added to the draw up organize and a NMOS added to the draw down system [15]. The entryway terminal of each LCT is controlled by the wellspring of the other, with the end goal that one of the LCTs is constantly close to its cutoff locale of operation.

In view of this game plan, extra resistance is given in the way, diminishing the sub-limit spillage current. This paper outlines LECTOR method with the instance of CMOS rationale circuit, viz., Decoder. LECTOR NAND gate is appeared in Figure 1. Two spillage control transistors LCT1 (PMOS) and LCT2 (NMOS) are presented at the hubs N1and N2 separately of the draw up and pull-down rationale of the NAND gate [13]. The source hubs of the transistors are associated with hubs N1 and N2 of draw up and pull-down rationale, separately. The voltage possibilities at hubs N2 and N1 controls the exchanging of transistors LCT1 and LCT2 individually [14]. This wiring setup guarantees that one of the LCTs is constantly close to its cutoff area, independent of the info vector connected to the NAND gate.

METHODS OF POWER MANAGEMENT

Due to the increased circuit density and speed, the power dissipation has emerged as an important consideration in circuit design. A lot of efforts on power reduction have been made at various levels of design abstraction. Considering the fact that the charging/discharging of capacitance is the most significant source of power dissipation in well-designed CMOS circuits Power consumption grows exponentially at 90nm and beyond technologies [11]. At smaller geometries, aggressive management of leakage current can greatly impact design and implementation choices. Indeed, for some designs and libraries, leakage current exceeds switching currents, thus becoming the primary source of power dissipation in CMOS Depending upon the architecture of the design, the designers can choose from a wide range of options for reduction in power consumption of VLSI circuits. Some of the techniques to reduce the power consumption are briefed below [12]. There are several methodology are available for low power management for IC. Some of them are listed below and briefly discussed (1) Logic restructuring (2)Clock tree optimization and clock Gating (3)Logic resizing (transistor resizing). (4)Transition rate buffering. (5)Pin swapping (6) Using multi-threshold voltage (7)Multi-supply voltage (voltage islands) (8)Dynamic voltage scaling (9)Dynamic voltage and frequency scaling (DVFS) (10)Power shutoff or power gating (11)Memory splitting (12)Substrate biasing (body-biasing or
back-biasing) (13) Operand isolation [15]

(i) Logic restructuring- The CMOS design uses both NMOS and PMOS transistors for logic design. Due to mobility variation in NMOS and PMOS transistors, the rise and fall time differ. By moving high switching operations up in the logic cone and low switching operations back in the logic cone, a considerable amount of power can be saved.

(ii) Clock tree optimization and clock Gating- Due to the impressive advancement of the VLSI circuit technology has been the rapid scaling down the feature size, i.e., the minimum dimension of the transistor. It decreased from 2μm in 1985 to 0.35μm in 1996. According to the National Technology Roadmap for Semiconductors (NTRS) it will further decrease at the rate of 0.7μm X per generation (consistent with Moore's Law) to reach 0.07μm by 2010. Such rapid scaling has two profound impacts [14]. First, it enables much higher degree of on-chip integration. The number of transistors per chip will increase by more than 2x per generation to reach 800 millions in the 0.07μm technology. Second, it implies that the circuit performance will be increasingly determined by the interconnect performance. The interconnect design will play the most critical role in achieving the projected clock frequencies. Interconnect has become the dominating factor in determining circuit performance and reliability in deep submicron designs interconnect design as the technology feature size rapidly decreases towards below 0.1 micron [13]. Thus we need a commonly used interconnect models and a set of interconnect design and optimization techniques for improving interconnect performance and reliability. Clock distribution is crucial for timing and

design convergence in high-performance very large scale integration designs. Minimum-delay/power zero skew buffer insertion/sizing and wire-sizing problems have long been considered intractable .Most of the power is consumed due to the high clock frequency used for operating the device. Portions of the clock tree that are not being used at any particular time can be disabled to save the power [12].

(iii) Logic resizing (transistor resizing)- The length-to-width ratio of transistors determines the driving strength and speed. Upsizing improves slew times, reducing dynamic current. Hence The dynamic power consumption is reduced. Downsizing reduces leakage current, thereby reducing the static power consumption. To be effective, sizing operations must include accurate switching information. Gate Sizing (GS) is a well-known technique which targets power optimization by reducing load capacitance several approaches have been published from a general point of view, reducing the physical size of a gate, at logic level, leads to the gate delay increase which implies the decreased slack time [15]. The basic rule is to use the smallest transistor or gates that satisfied the delay constraints. To reduce the dynamic power the gate that toggle with higher frequency should be made smaller. Actually the basic rule sounds simple, the actual sizing problem is very complicated. Consider a part of the circuit part as shown in the below figure 3. Suppose that the gates are not on the critical delay path and should be size down [13]. We can size down the first gate, the second gate, or both, subjected to the available sizes in the cell library as long as the path delay is not violated. If the path contains many gates, the optimization problem quickly becomes very complicated. Fig. 3. Model circuit The concept of slack time is often used to express the timing constrains of the circuit. The slack time of a gate is the difference between the signal required time and the signal arrival time at the output of the gate [14]. A positive slack time means that the signal arrived earlier than its required time and the gate can be sized down. The goal of gate sizing is to adjust the gate sizes such that the slack time of each gate is s low as possible without any gate having a negative slack i.e., time violation a greedy algorithm was proposed by an exact algorithm for low power library specification gate resizing, it attempts to downsize a set of gates that gives the most reduction in the power dissipation without affecting the time slack of all other gates [15].

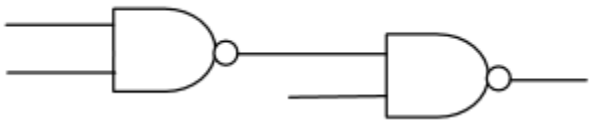

Figure 3- Model circuit[12]

The new slack times of the downsized gates are then compute and a new set of gates is selected. The simplest transistor gate sizing problem is that of an inverter chain the general design problem is to derive a large capacitive load without excessive delay, area and power requirements [11-14]. In a chain of successively large inverter, so that all the inverters in the chain drive appropriate loads and do not causes excessive delay. Using a simple RC delay model in inverter chain the delay of the inverter is directly proportional to the load it drives. For example if an inverter drives K other inverters of the same size, the delay through the inverter is Kd where d is the intrinsic delay of the inverter under a single load. Then the total delay is given by D through the chain [15-21].

CONCLUSION

An IC comprises of many circuits of which a few circuits have basic way, though a few circuits have no predetermined basic way. LECTOR procedure is utilized to configuration circuits with no basic way and MTCMOS system is utilized to configuration circuits with basic ways. At the point when connected to non specific rationale circuits, the LECTOR method accomplishes up to 40-45% spillage decrease over the traditional circuits without influencing the dynamic power. The proposed full viper circuit planned with MTCMOS procedure accomplished 20.99% power diminishment and 4.95% defer decrease with no region overhead for 90nm innovation.

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