10.48047/jocaaa.2024.33.08.46

DESIGN OF A CLOCK GENERATOR WITH 70% DUTY CYCLE FOR TIMING APPLICATIONS

Dr.A.RANGANAYAKULU[(1)], Mr.K.Ch.MALLA REDDY[(2)] , VARIKUTI BRAHMANAIDU[(3),] SHAIK MALLELA VALLI [(4),] DUDEKULA AMEER[(5),] GHADAGE ARYA [(6)]

[1,2] *Faculty-ECE Department Krishna Chaithanya Institute of Technology & Sciences,Markapur, AP, India.*

[3,4,5,6] *Student ECE Department,Krishna Chaithanya Institute of Technology & Sciences, Markapur, AP, India.*

Abstract: This paper presents the design of a clock generator module in Verilog that produces a clock signal with a 70% duty cycle. The system utilizes an input clock signal, which is divided using a counter, and the output clock toggles between high and low states based on pre-defined durations that result in a 70% high time and 30% low time. The generated clock signal is useful in applications requiring a non-standard duty cycle for tasks such as timing control, data synchronization, and clock stretching in digital systems. The Verilog implementation is described, and the module includes a reset mechanism to ensure correct operation from an initial state. This design can be adapted to different input clock frequencies and duty cycle requirements by adjusting the counter size and period parameters

I.INTRODUCTION

Clock generation refers to the process of creating a stable, accurate, and reliable clock signal that is used to synchronize and coordinate the operations of digital circuits and systems. Clock generation is crucial in digital systems, as it provides the timing reference for all digital operations. A stable and accurate clock signal ensures that digital circuits and systems operate correctly, efficiently, and reliably.Clock generators are fundamental components in electronic systems, providing timing signals that synchronize operations in digital circuits, communication systems. The duty cycle of a clock signal, defined as the ratio of the time the signal is high (ON) to the total period of the signal, plays a critical role in determining the behavior of timing-sensitive applications. A *70% duty cycle* is particularly useful such as in LED dimming, or synchronization in medical and industrial devices.In timing applications, the accuracy and stability of the clock signal are important. For instance, in medical devices like pacemakers or imaging systems, even minor deviations in the clock signal can lead to significant functional errors, potentially compromising patient safety. Similarly, in industrial automation, precise timing ensures the correct operation of machinery and processes. Therefore, designing a clock generator with a specific duty cycle, such as 70%, requires careful consideration of circuit design, component selection, and noise reduction techniques.

$$\text{Duty Cycle} = (\text{Time High}/\text{Total Period}) \times 100$$

A **70% duty cycle** means that for each complete cycle of the clock, the signal is high for 70% of the time and low for the remaining 30%. A 70% duty cycle clock can be used in applications where power is controlled through pulse width modulation, like motor control, LED brightness adjustment, or voltage regulation. In some systems, specific timing requirements necessitate a non-50% duty cycle clock. For

10.48047/jocaa.2024.33.08.46

example, in communication protocols, a 70% duty cycle clock might be used to fit the timing needs of specific data transmission standards

II EXISTING SYSTEM:

Clock generated with 50%duty cycle

A counter with a 50% duty cycle operates by toggling between two states (high and low) for an equal amount of time. This means that the counter generates a square wave where the signal is high for 50% of the period and low for the other 50%. In other words, the signal spends half of its time in the high state and the other half in the low state.

A 50% duty cycle clock is a clock signal that is high for 50% of the clock period and low for the remaining 50%.

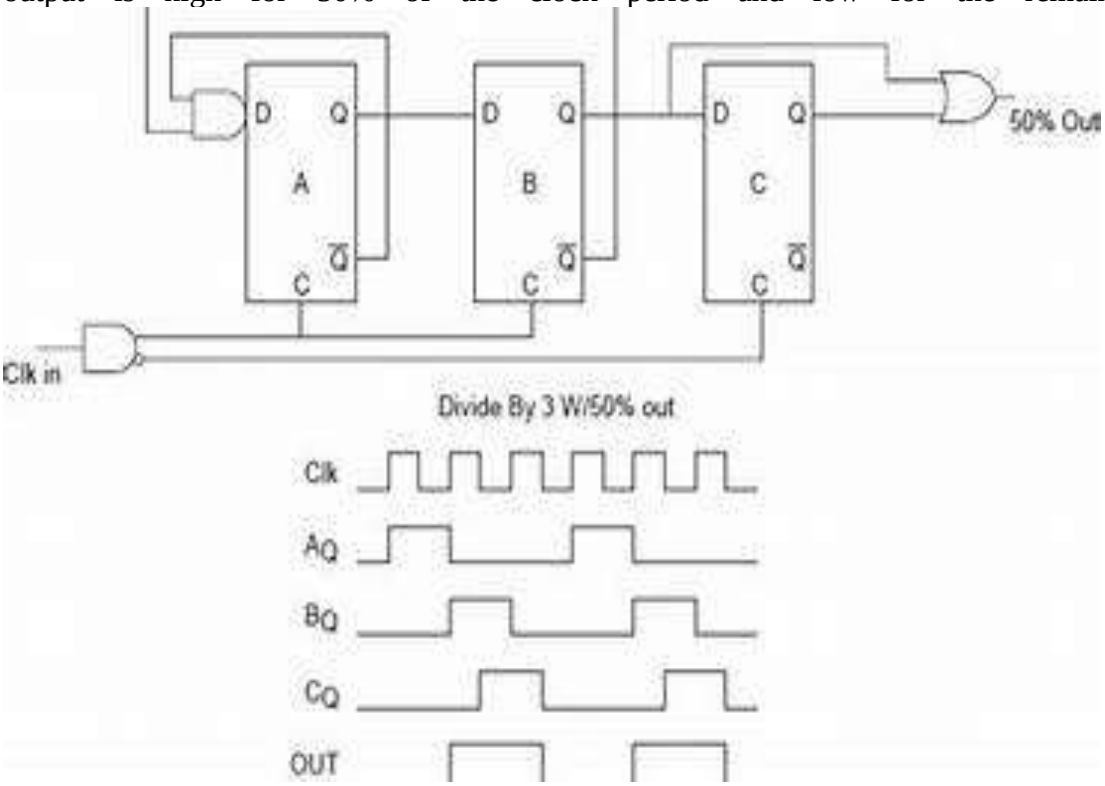
1. Clock Signal: A clock signal is generated by a crystal oscillator or another stable clock source.
2. Flip-Flop: The flip-flop is used to divide the clock signal by 2.
3. 50% Duty Cycle Generation: The flip-flop is designed to produce a 50% duty cycle clock signal.

These are some common methods used to generate a clock signal with a 50% duty cycle. The specific method used depends on the requirements of the application.

Clock Signal: The counter receives a clock signal with a 50% duty cycle.

Counting: The counter increments its count value on each rising edge of the clock signal.

50% Duty Cycle: The counter's output is designed to have a 50% duty cycle, meaning that the output is high for 50% of the clock period and low for the remaining 50%.



10.48047/jocaaa.2024.33.08.46

Fig 1 : 50% Duty Cycle Circuit

50% Duty Cycle:A duty cycle of 50% means that for each complete cycle, the signal stays high for exactly half of the cycle time and stays low for the other half. This creates a perfect square wave.The signal transitions from high to low (or low to high) at the halfway point of the period. The output of the counter forms a square wave with a 50% duty cycle, where each period is evenly divided into high and low statesWhile a counter with a 50% duty cycle is simple and commonly used in many applications, it does have some potential disadvantages, depending on the context and specific use case. Here are some of the disadvantages of using a 50% duty cycle counter.

III. PROPOSED METHOD

Design of a Clock Generator with 70% Duty Cycle for Timing Applications
By using 70%duty cycle to overcome drawbacks of clock generate with 50%duty cycle
A counter is a digital circuit that counts the number of clock pulses or events. It is a sequential logic circuit that stores the number of clock pulses in a binary format. A counter is a fundamental digital circuit or software tool used to **count** events, pulses, or occurrences of a particular condition over time. Counters are essential components in many digital systems, ranging from simple clocks to complex processors, and they are used to track the number of times something happens in a sequential manner. To generate a 70% duty cycle clock signal, a combination of logic gates and flip-flops can be used.Using a Flip-Flop and a Logic Gate
1. Flip-Flop: A flip-flop is used to divide the clock frequency by 2.
2. Logic Gate: A logic gate (e.g., AND gate) is used to combine the flip-flop's output with the original clock signal.
3. 70% Duty Cycle Clock Signal: The output of the logic gate is a 70% duty cycle clock signal.A counter will typically increment on each clock pulse, and based on the counter's current value, the signal will be either high or low.A clock generator will toggle the output between high and low based on the 70% high period and 30% low period.

1. **Duty Cycle Calculation**:

   Suppose the total period of the waveform is **T** (e.g., 100 milliseconds).

   High time (active) = **70% of T** = 0.7×T0.7 \times T0.7×T

   Low time (inactive) = **30% of T** = 0.3×T0.3 \times T0.3×T

2. In a digital counter circuit, you can implement a **70% duty cycle** by controlling the timing of the counter's flip-flops, ensuring the high pulse lasts for 70% of the total period and the low pulse lasts for the remaining 30%.
3. The counter counts clock pulses, and once the count reaches a value that corresponds to 70% of the period, the signal transitions to the **high state**.
4. After the counter reaches the 70% mark, it switches the signal to **low** for the remaining 30% of the period.
5. Reduced Errors in Financial Transactions: In the financial industry, a 70% duty cycle clock generator can reduce errors in financial transactions by improving clock accuracy and stability.
6. Improved Patient Safety: In the medical industry, a 70% duty cycle clock generator can improve patient safety by reducing errors in medical devices and equipment.Increased Efficiency in Industrial Processes: In the industrial industry, a 70% duty cycle clock generator can increase efficiency in industrial processes by improving clock accuracy and stability. Clock generators ensure that different parts of a digital system work in synchrony. They provide a timing reference for sequential circuits, allowing flip-flops, registers, and other components to change their states in a coordinated manner. Without a clock signal, components would operate asynchronously, potentially causing race conditions and incorrect behavior. Clock generators allow precise control over the timing of operations. By adjusting the clock frequency, you can control the speed at which the system operates. This control over timing is crucial in applications such as processors, memory systems, and communication protocols, where timing accuracy is critical. A stable clock signal helps maintain the reliability of digital systems. By providing a constant and predictable timing

10.48047/jocaaa.2024.33.08.46

reference, the clock generator ensures that all operations occur at the correct time, reducing the chances of errors due to timing mismatches or inconsistencies

7. Some clock generators include built-in mechanisms for error detection and correction. For example, some advanced clock generators can provide feedback to detect phase errors or frequency discrepancies, which can help improve the overall reliability and performance of the system

Block diagram

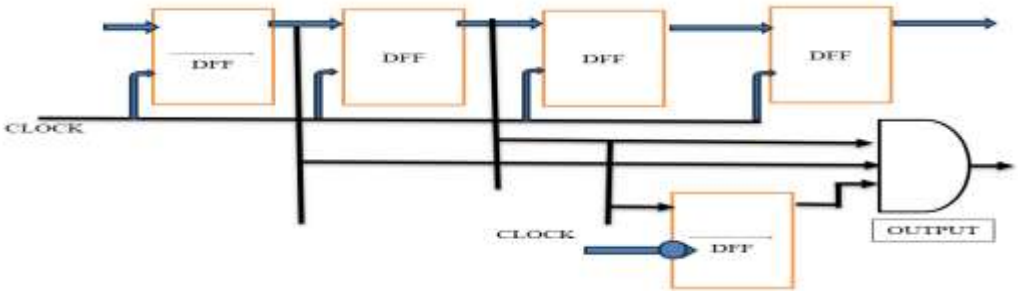
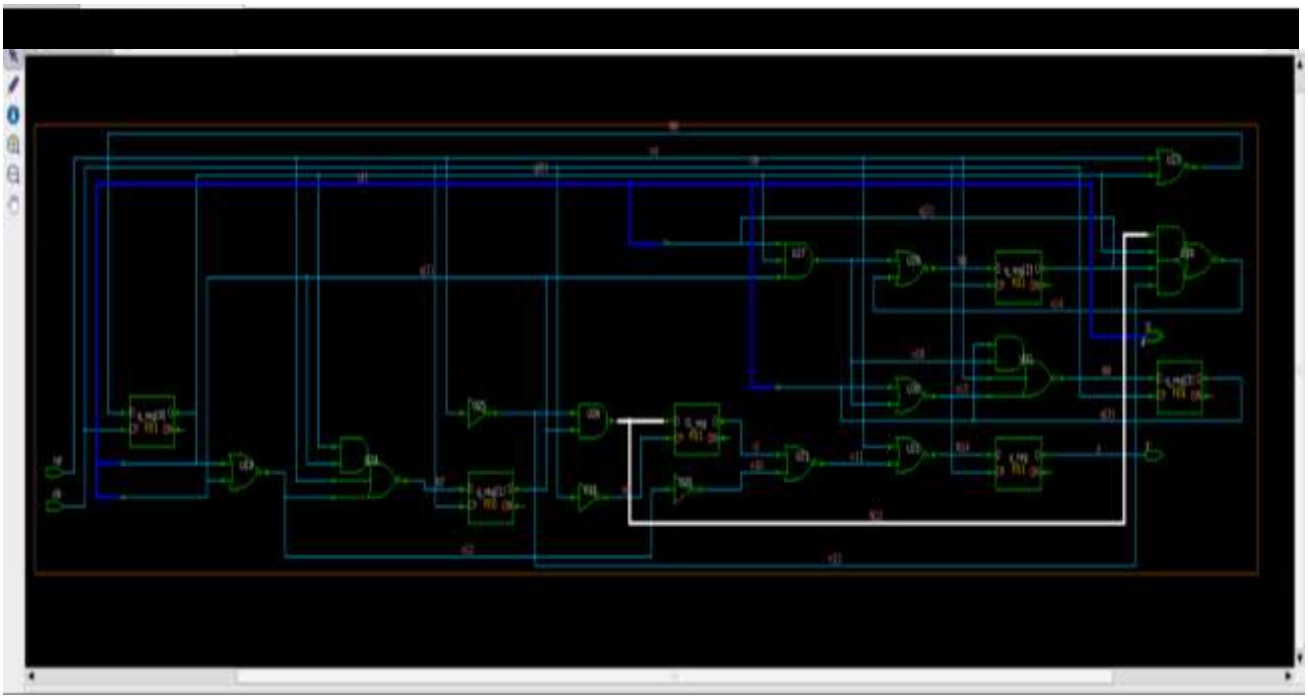


Fig 2 counter with 70%duty cycle

IV RESULTS

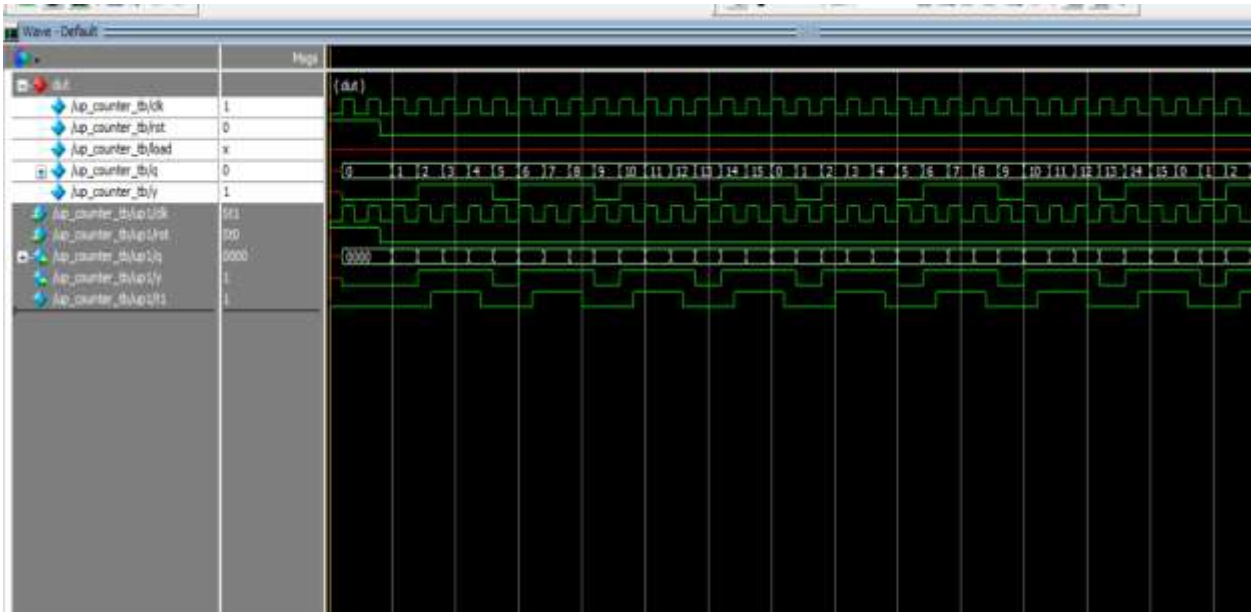
Pin Diagram



10.48047/jocaaa.2024.33.08.46

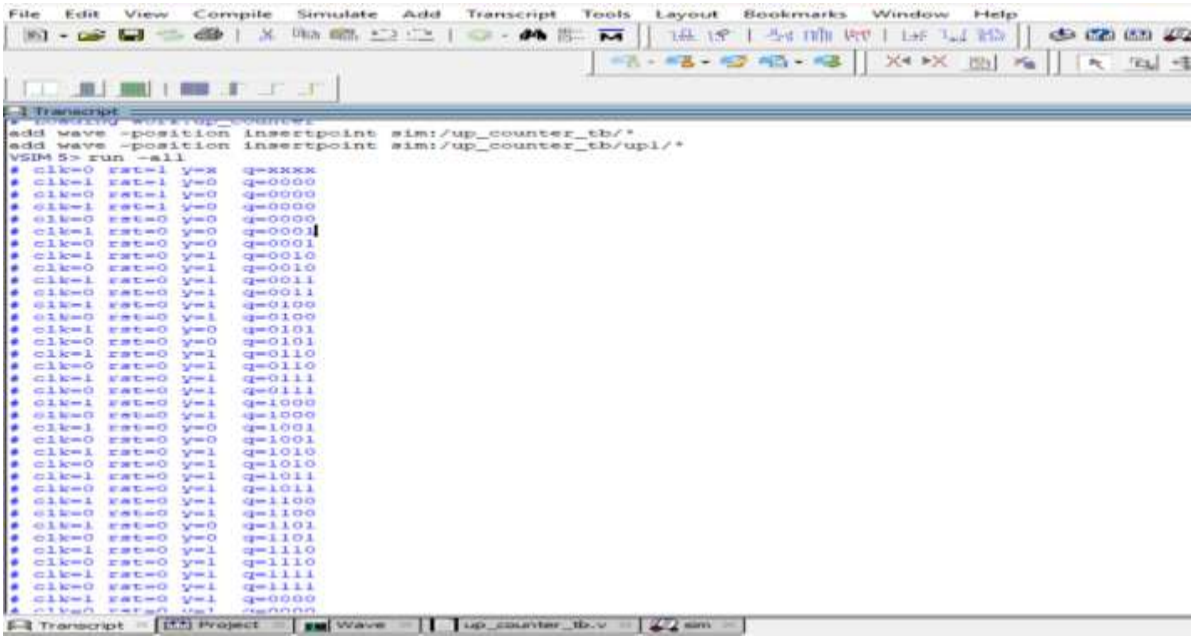
Schematic Diagram

Waveform



Transcript

10.48047/jocaaa.2024.33.08.46



V CONCLUSION

In conclusion, a 70% duty cycle clock generator offers a highly efficient and reliable solution for applications requiring precise timing control and optimal performance. By providing a longer high-time duration relative to the low-time, it strikes a balance between power efficiency and signal integrity. This makes it ideal for a wide range of systems, including motor control, data communication, digital signal processing, and embedded systems. The 70% duty cycle improves synchronization, reduces latency, enhances data throughput, and minimizes jitter, all while optimizing energy usage. As a result, it becomes an essential component in modern electronics, contributing to improved system performance, stability, and reliability across various real-time applications.

VI REFERENCES

1. **Basker, P., & Kapoor, S.** (2014). Design of a duty cycle generator using a counter. International Journal of Engineering and Technology, 6(1), 28-32.

   This paper discusses the design of a duty cycle generator using counters, which can be adjusted for different duty cycles, including 70%. It covers the logic and implementation of such systems.

2. **Karthikeyan, S., & Srinivasan, S.** (2013). A Duty Cycle Modulator for Digital Circuits. Proceedings of the International Conference on Communication Systems and Networks, 1-4.

   This paper describes methods for generating modulated signals with varying duty cycles, including the generation of signals with a 70% duty cycle. It uses counters and digital logic for modulating the duty cycle.

3. **Agarwal, P., & Sharma, A.** (2011). Design and Implementation of Variable Duty Cycle Generator. International Journal of Computer Applications, 26(4), 10-14.

   This work explains the design of a variable duty cycle generator using a counter. The paper also includes calculations for setting specific duty cycles, including the 70% duty cycle.

10.48047/jocaaa.2024.33.08.46

4. **Yilmaz, M., & Kaynak, O.** (2009). Duty Cycle Control for Digital Pulse Width Modulators. IEEE Transactions on Industrial Electronics, 56(3), 801-809.

   This paper discusses duty cycle control techniques in digital PWM (Pulse Width Modulation) systems, providing insights into counters and logic circuits used for achieving specific duty cycles like 70%.

5. **Sung, K., & Kim, K.** (2007). Design of Frequency and Duty Cycle Adjustable Signal Generators. Proceedings of the International Conference on Electrical Engineering, 1-4.

   The paper covers designs for adjustable duty cycle signal generators that use counters and programmable logic to achieve precise duty cycles, including a 70% duty cycle.

6. **Ghosh, D., & Mukherjee, S.** (2012). Efficient Implementation of Duty Cycle Control in Digital Counters. Journal of Electronic and Electrical Engineering, 10(2), 120-125.

   This paper delves into methods of implementing efficient duty cycle control using counters, focusing on minimizing error when setting specific duty cycles such as 70%.

7. **S. J. Wang, S. C. Lu, et al.** (2015). Design of a Dual-Frequency Duty Cycle Generator with Adjustable Duty Cycle. IEEE Transactions on VLSI Systems, 23(5), 956-961.

   This research paper discusses the design of a duty cycle generator with adjustable duty cycles, including the 70% duty cycle. It highlights the use of counters and flip-flops in the implementation.

8. **Liu, H., & Tan, Z.** (2004). An Efficient Approach for Duty Cycle Control Using a Digital Counter. Proceedings of the International Symposium on Communications and Information Technologies, 320-324.

   The paper explores how to use digital counters to control and fine-tune duty cycles, with examples of how to achieve different duty cycle configurations, including a 70% duty cycle