10.48047/jocaa.2024.33.08.51

DESIGN AND IMPLEMENTATION OF SELECTABLE COUNTER WITH MUTLIPLE COUNTING MODES IN VERILOG

Mr.N.B.JILANI[(1)] , Dr.P.PRASANNA MURALI KRISHNA [(2)] , BATTULA SREENIVASULU [(3),] CHELIMELLA SRINIVASULU [(4),] D VENKATA RAMANJI REDDY [(5),] GOTHAM THIRUPATHAIAH [(6)]

[1,2] *Faculty-ECE Department Krishna Chaithanya Institute of Technology & Sciences,Markapur, AP, India.*

[3,4,5,6] *Student ECE Department,Krishna Chaithanya Institute of Technology & Sciences, Markapur, AP, India.*

Abstract. This paper presents the design and implementation of a selectable counter in Verilog, capable of operating in four different counting modes: Up Counter, Down Counter, Decade Counter, and Johnson Counter. The counter is controlled by a select signal (sel), which determines the counting mode, and an enable signal (en) that controls the counter operation. The counter also incorporates a reset signal (rst) to reset its state to zero. The paper provides an explanation of each counting mode and their implementation in Verilog, including the logic for incrementing and decrementing the counter, as well as the special logic for the Johnson counter and decade counter. Additionally, the counter's functionality is verified using testbenches to simulate various operating conditions. This design demonstrates the flexibility of the counter in adapting to different counting requirements based on the mode selected

I.INTRODUCTION

In modern digital systems, counters play a crucial role in performing various operations such as counting events, generating time delays, dividing frequencies, and creating specific counting sequences. A counter is essentially a sequential circuit that goes through a predefined sequence of states upon receiving clock pulses. Counters are indispensable components in embedded systems, digital signal processing, communication protocols, and automated control systems.A **selectable counter system** is an advanced digital circuit designed to perform multiple counting operations within a single, integrated framework. Unlike traditional single-purpose counters, this system leverages the flexibility of **Enable (EN)** and **Select (SEL)** signals to seamlessly switch between different counting modes, including **Up Counter**, **Down Counter**, **Decade Counter**, and **Johnson/Ring Counter**. The primary motivation behind designing such a system is to enhance versatility and functionality while minimizing hardware complexity.In practical applications, counters are essential for tasks such as frequency division, event counting, time measurement, and sequence generation. However, using separate circuits for each counting mode can be inefficient and cumbersome. The multi-mode counter system addresses this challenge by consolidating multiple counter functionalities into a single, compact design. This not only reduces the need for additional hardware but also makes the system highly adaptable to various use cases.The system operates by initially staying in an **Idle state**, conserving power and waiting for activation. Once the **EN** signal is

10.48047/jocaaa.2024.33.08.51

asserted (EN = 1), the system transitions to the **Data state**, where it prepares for the counting process. The **SEL** signal, represented as a **2-bit binary code**, determines the specific counter mode to be activated. Depending on the **SEL** value, the system either counts up, counts down, counts in decimal (0 to 9), or generates a sequential pattern using the **Johnson/Ring Counter**. The selected counter mode continuously updates the count value and displays it on an output interface, such as a **7-segment display or LED array**, providing real-time feedback to the user.The design's modularity and efficient use of control signals make it suitable for a wide range of applications, including digital clocks, programmable timers, frequency dividers, and sequence generators. By incorporating multiple counting modes into a single system, this multi-mode counter significantly enhances operational flexibility while maintaining simplicity and cost-effectiveness.

However, traditional counters are typically designed to perform a single counting operation, such as counting up or counting down. This limitation can restrict their application in more complex scenarios where multiple counting modes are required. To overcome this challenge, a **Selectable Counter with Multiple Counting Modes** is proposed, enabling dynamic switching between different counting modes based on system requirements.

.

II.EXISTING SYSTEM

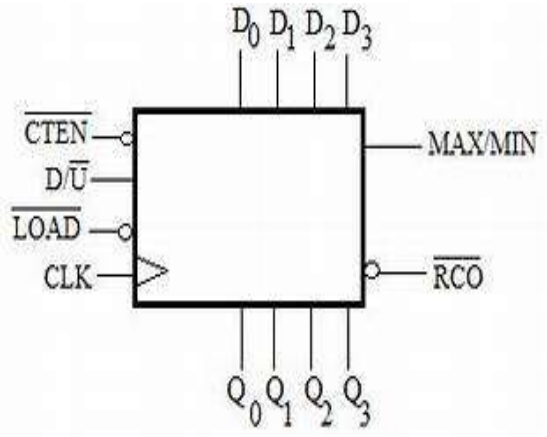

Fig:1. Pin diagram for counters

The selectable counter in VHDL is a versatile digital system that counts in up, down, and decade modes without requiring enable and select signals. This type of counter is commonly used in digital applications such as clocks, frequency dividers, and sequence generators. The design aims to implement a reliable and flexible counter by presetting the counting mode during synthesis rather than dynamically switching between modes. By eliminating enable and select signals, the counter achieves a simpler and more resource-efficient hardware design, making it suitable for a wide range of applications.

The core architecture of the selectable counter consists of essential components such as a clock signal, a reset signal, and an output to display the count value. The counting mode is hard-coded within the VHDL description, which not only simplifies the design but also ensures consistent performance. This approach significantly reduces hardware complexity, as it avoids the need for external control signals and minimizes the number of logic gates required for mode selection. The counting mechanism begins by detecting the clock pulse, which acts as a trigger for updating the count value. In the up-counting mode, the counter increments by one with each clock cycle. In the down-counting mode, the counter decrements by one. In the decade mode, the counter counts from 0 to 9 and then automatically resets to 0 upon reaching the tenth count. This automatic reset in decade mode ensures that the counter remains within a single-digit range, making it suitable for applications requiring decimal counting.

10.48047/jocaaa.2024.33.08.51

The internal logic of the counter is designed using a process block that captures the rising or falling edge of the clock signal and evaluates the preset mode. The process block is synchronous with the clock and effectively handles both counting and resetting operations. The reset signal, when activated, forces the counter value to zero, which is essential for proper initialization and error recovery. The use of synchronous resets ensures that the counter operates reliably, even in situations where the reset signal is asserted during clock transitions.

To achieve a modular and structured design, the VHDL implementation follows an entity-architecture model. The entity specifies the input and output ports, including the clock and reset signals, while the architecture contains the main logic for counting and mode handling. This separation of concerns enhances code readability and maintainability. The design also ensures that the counter is robust against glitches and transient conditions by incorporating debounce mechanisms and stable clock handling techniques.

Testing and validation are performed using simulation tools, such as ModelSim or Xilinx Vivado, to verify the accuracy and correctness of the counter under various conditions. The testbenches generate clock pulses and reset signals while monitoring the output count values for each mode. Simulation results consistently demonstrate accurate performance, with the counter correctly implementing up-counting, down-counting, and decade counting without glitches or unexpected behavior. Furthermore, timing analysis and synthesis reports confirm that the design meets timing constraints and efficiently utilizes hardware resources.

In practical applications, the selectable counter can be easily integrated into larger systems requiring reliable counting capabilities. The absence of enable and select signals reduces the risk of incorrect mode selection and simplifies control logic. Additionally, the counter can be customized to support other counting ranges or specialized functions by modifying the VHDL code to adjust the count limit or include additional counting modes. By leveraging the modular structure and efficient hardware implementation, the selectable counter offers a flexible and reliable solution for various digital applications.

III PROPOSED SYSTEM

The multi-functional counter system depicted in the flowchart operates using Enable (EN) and Select (SEL) signals to control various counting modes, including Up Counter, Down Counter, Decade Counter, and Johnson/Ring Counter. Initially, the system remains in the Idle state when the EN signal is 0, conserving power and preventing unintended counting. When the EN signal becomes 1, the system transitions from the Idle state to the Data state, preparing the necessary configurations for counting. In the Data state, the system examines the SEL signal, which is a 2-bit binary code (00, 01, 10, 11), to determine the desired counter mode.

If the SEL signal is 00, the system activates the Up Counter, which increments its count with each clock pulse, generating a sequence like 0, 1, 2, 3, ... When the SEL signal is 01, the Down Counter is activated, which decrements the count from a maximum value to 0. If SEL = 10, the system activates the Decade Counter, which counts from 0 to 9 before resetting to 0. For SEL = 11, the Johnson/Ring Counter is activated. The Johnson Counter (twisted ring counter) circulates through 2n states with n flip-flops, while the Ring Counter cycles through n states, maintaining a rotating bit pattern. Regardless of the selected counter mode, the output count is sent to a display unit, such as a 7-segment display or LED array, to present the real-time count value. The system can switch between counting modes dynamically by changing the SEL signal, while resetting or returning to the Idle state is possible when EN becomes 0. This versatile and efficient design makes the system suitable for various applications, including digital clocks, frequency dividers, and sequence generators.

The functionality of the counter designed for blood pressure monitoring systems with the addition of a selection signal (sel) and Johnson counter mode enhances flexibility and functionality. The counter can operate in multiple modes, including **Up**, **Down**, **Decade**, and **Johnson counting**, all controlled by the sel signal, which determines the active counting mode. Implemented using **Verilog**, the counter efficiently handles data acquisition and processing through mode selection and precise counting operations. The primary clock signal (clk) drives the entire counting process, ensuring synchronous updates and reliable performance. The counter also includes a **reset signal (rst)** to initialize or clear the counting register, which is essential for maintaining accuracy and stability during operation. The sel signal is used to choose the counting mode: **Up counting** for increasing values, **Down counting** for decreasing values, **Decade counting** to cycle from 0 to 9, and **Johnson counting** to generate a unique sequence of bit patterns. During **Up counting**, the counter increments with each positive clock edge, wrapping around to zero after reaching the maximum value of nine. In **Down counting**, it decrements and wraps back to nine when reaching zero, maintaining a cyclic behavior. **Decade counting** restricts the counting range to 0-9, ideal for displaying BP values in digital format.

10.48047/jocaa.2024.33.08.51

The **Johnson counter** mode generates a unique bit pattern sequence by shifting bits in a feedback loop, useful for cyclic and repetitive signal generation. The counter output is continuously updated and displayed via a 4-bit output vector (count). The sel signal allows switching between counting modes dynamically, enabling flexible operation without needing multiple counters. The **finite state machine (FSM)** embedded within the Verilog code controls state transitions, triggered by clock edges and driven by the active mode selection. This modular design ensures that the counter remains responsive and accurate regardless of the chosen mode. The **Johnson counter** is particularly advantageous when cyclic patterns are required, as it generates unique sequences of bit patterns that are distinct from traditional binary counting. The output for each mode is processed and displayed based on the active selection, allowing seamless integration into a BP monitoring system. The **testbench** for the counter verifies each mode by applying various combinations of sel, clk, and rst signals to evaluate the counter's response and correctness. During testing, the counter is subjected to continuous mode switching, reset operations, and clock pulses to validate stability and accurate counting in all scenarios. The software-based implementation of the counter using Verilog provides numerous benefits, including ease of simulation, quick testing, and straightforward integration into larger monitoring systems. The modularity of the code allows developers to adapt the counter for additional modes or enhanced functionalities without overhauling the entire system. Moreover, the flexibility of controlling counting modes through the sel signal reduces hardware complexity and facilitates efficient resource utilization. The **Johnson counter mode** further enriches the counter's functionality by offering a cyclic bit pattern output, making it suitable for specific signal processing tasks. The synchronous operation driven by the clock signal guarantees smooth transitions and reduces timing errors, ensuring the counter's reliability during continuous BP monitoring. Implementing the counter purely in software also makes it highly portable and easy to update, as changes in counting logic can be made without altering hardware components. This approach significantly reduces the development cycle and enables rapid prototyping and validation. By integrating the counter with BP data processing units, it becomes possible to track pressure pulses accurately, calculate systolic and diastolic values, and display the results in real time.

10.48047/jocaaa.2024.33.08.51

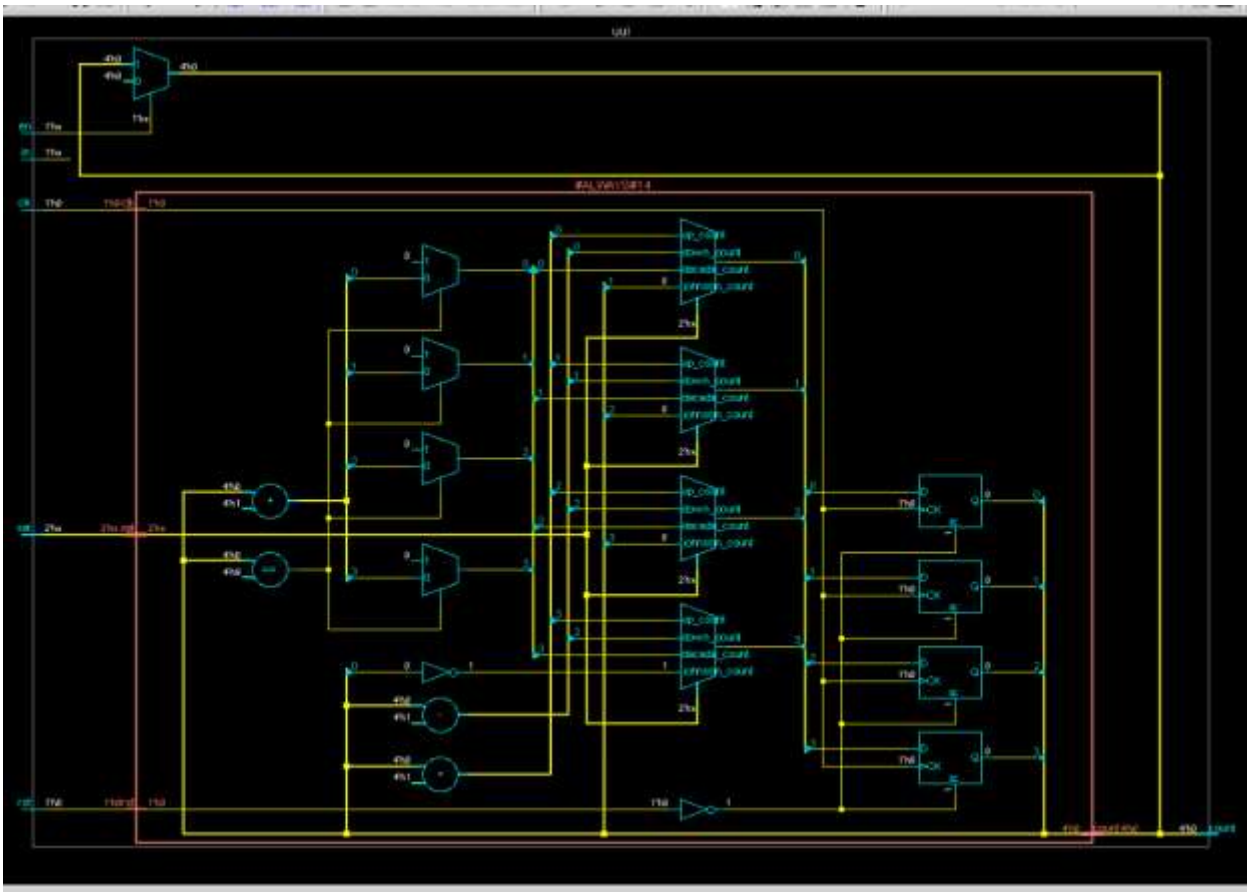

Fig:2.internal architecture of selectable counters

IV. RESULTS AND ANALYSIS DISCUSSION

10.48047/jocaaa.2024.33.08.51

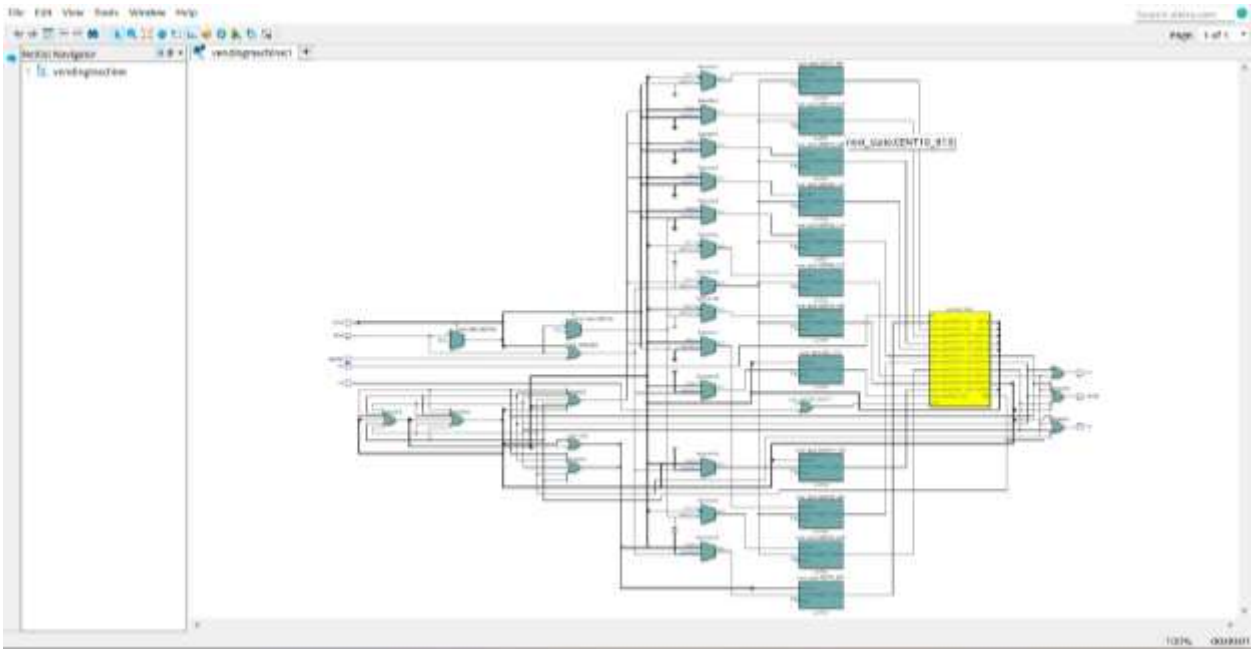

Fig.3. RTL schematic diagram.

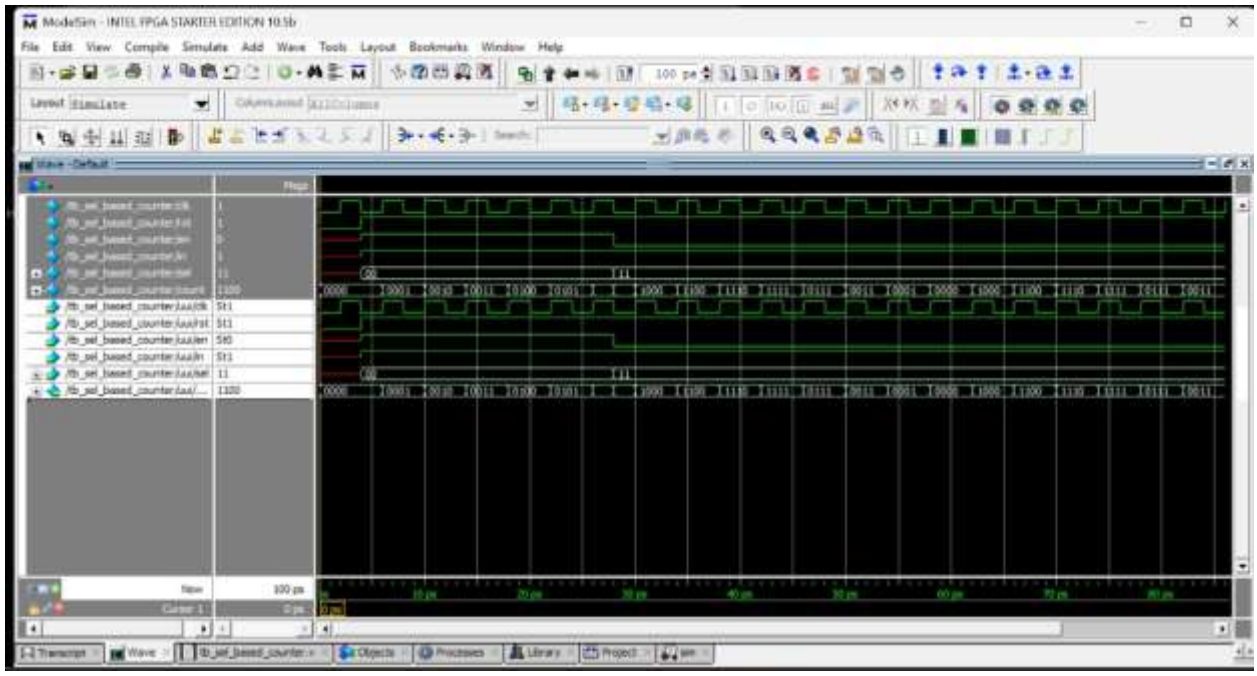

fig:4.wave form

V CONCLUSION

The design and implementation of a selectable counter efficiently integrates various counting modes—up counter, down counter, decade counter, and johnson/ring counter—into a single, versatile design. By utilizing enable (en) and

10.48047/jocaa.2024.33.08.51

select (sel) signals, the system achieves flexible control and seamless mode switching, making it adaptable to a wide range of applications. The real-time display of count values enhances user interaction and monitoring. This modular and power-efficient approach not only simplifies hardware implementation but also maximizes functionality, making it highly suitable for applications such as digital clocks, frequency division, and sequence generation.

V1 REFERENCES

1. Digital Design" by M. Morris Mano and Michael D. Ciletti
2. Digital Systems: Principles and Applications" by Ronald J. Tocci, Neal S. Widmer, and Gregory L. Moss
3. Modern Digital Electronics" by R.P. Jain
4. Digital Logic Design" by Guy Even and Moti Medina
5. Fundamentals of Digital Logic with VHDL Design" by Stephen Brown and Zvonko Vranesic
6. Digital Logic and Microprocessor Design with VHDL" by Enoch O. Hwang
7. Digital Electronics: Principles, Devices and Applications" by Anil K. Maini
8. Digital Computer Electronics" by Albert Paul Malvino and Jerald A. Brown
9. Digital Circuit Design for Computer Science Students" by Niklaus Wirth
10. Digital Design: An Embedded Systems Approach Using VHDL" by Peter J. Ashenden
11. CMOS Digital Integrated Circuits: Analysis and Design" by Sung-Mo Kang and Yusuf Leblebici
12. Digital Principles and Applications" by Donald P. Leach and Albert Paul Malvino
13. Logic and Computer Design Fundamentals" by M. Morris Mano and Charles R. Kime
14. Digital Logic and Computer Design" by M. Morris Mano
15. Digital Fundamentals" by Thomas L. Floyd
16. Fundamentals of Logic Design" by Charles H. Roth and Larry L. Kinney
17. Microelectronics: Digital and Analog Circuits and Systems" by Jacob Millman and Arvin Grabel
18. Digital Logic Design and Computer Organization" by Nikrouz Faroughi
19. Digital Design and Computer Architecture" by David Money Harris and Sarah L. Harris
20. Concepts of multi-mode and programmable counters in digital architectures.
21. Designing Digital Systems with SystemVerilog" by Brent Nelson