10.48047/jocaaa.2024.33.08.62

DESIGN AND IMPLEMENTATION OF DUAL-PORT RAM WITH MULTI-CLOCK SUPPORT IN VERILOG

Mr.M.RAMANA REDDY[(1)], Mr.B.AJANTHA REDDY[(2)] , AVUKU SUBRAMANYAM [(3),] KOTLA SHIVA REDDY[(4),] DUDDELA RAMAKRISHNA REDDY[(5),] YELAM VENKATA SAI VAMSI[(6)]

[1,2] *Faculty-ECE Department Krishna Chaithanya Institute of Technology & Sciences,Markapur, AP, India.*

[3,4,5,6] *Student ECE Department,Krishna Chaithanya Institute of Technology & Sciences, Markapur, AP, India.*

ABSTRACT

This paper discusses the design and implementation of a Dual-Port RAM (DPRAM) with multi-clock support using Verilog. Dual-Port RAM allows simultaneous read and write operations on two independent ports, which can be useful for high-performance applications such as data buffering, communication systems, and video processing. This design incorporates multi-clock support, enabling the two ports to operate under different clock domains. We leverage Verilog's always blocks and asynchronous resets to ensure correct operation of the dual-port memory with minimal timing issues. The Verilog implementation includes a testbench to simulate the functionality of the DPRAM, ensuring the correct read/write operations under various clocking conditions. The solution provides flexibility for systems that require independent clocking for read and write operations.

I.INTRODUCTION

Dual-port RAM (DPRAM) in VLSI (Very-Large-Scale Integration) is a type of memory that allows simultaneous read and write operations from two separate ports, making it highly efficient for applications where data must be accessed and modified concurrently. It typically consists of two independent access ports one for reading and one for writing each capable of performing operations independently without interfering with the other. In VLSI designs, DPRAM is widely used in systems that require high throughput, such as communication systems, video processing, and signal processing. The two ports, often referred to as Port A and Port B, can either be configured for reading or writing, allowing them to operate in parallel. This parallelism improves system performance, as one port can read data while the other writes without waiting for the first operation to completed.DPRAM can be implemented using various architectures, such as static RAM (SRAM) cells. However, ensuring proper synchronization and avoiding read/write conflicts between the two ports are key challenges in its design. Dual-port RAM (DPRAM) in VLSI (Very- Large-Scale Integration) is a type of memory that allows simultaneous read and write operations from two separate ports, making it highly efficient for applications where data must be accessed and modified concurrently. It typically consists of two independent access ports—one for reading and one for writing each capable of performing operations independently without interfering with the other. Dual-Port RAM is a specialized type of random-access memory (RAM) that allows two independent ports to access the memory simultaneously. Each port has its own set of address, data, and control signals, enabling simultaneous read and write operations without conflicts when accessing different memory locations.Dual-port RAM is a type of memory that allows simultaneous access by two different devices or processors. This capability is especially useful in systems requiring high-speed data exchange between two independent units, such as communication buffers, graphics systems, or multiprocessor systems. Dual-port RAM, is a type of random-access memory (RAM) that can be accessed via two different buses. A simple dual-port RAM may allow only read access through one of the ports and write access through the other, in which case the same memory

10.48047/jocaaa.2024.33.08.62

location cannot be accessed simultaneously through the ports since a write operation modifies the data and therefore needs to be synchronized with a read or another write operation.A dual-port RAM may be built from single-port memory cells to reduce cost or circuit complexity, and the performance penalty associated with it, which may still allow simultaneous read and write accesses to different memory locations depending on the partitioning of the memory array and having duplicate decoder paths to the partitions. A true dual-port memory has two independent ports, which means that the memory array is built from dual-port memory-cells, and the address, data, and control lines of the two ports are connected to dedicated IO controllers so that the same memory location can be read through the ports simultaneously. A write operation through one of the ports still needs to be synchronized with a read or write operation to the same memory location through the other port. Independent clocking" refers to the ability of each port (Port A and Port B) to operate with its own separate clock signal. Each port has its own clock frequency: Port A and Port B can operate at different clock frequencies, allowing for greater flexibility in system design. Each port has its own clock phase: Port A and Port B can operate with different clock phases, allowing for more efficient data transfer and reduced skew. Each port can operate asynchronously: Port A and Port B can operate independently, without being synchronized to a common clock signal.

II EXISTING METHOD

Design and Implementation of Dual Port RAM in VHDL:

Dual-Port RAM (DPRAM) refers to a type of memory where two separate ports allow for independent read and write operations at the same time. It is widely used in applications such as gaming and graphics, where high-speed memory access is crucial for performance. Each port can be either for reading or writing, and each port can access different data independently.In gaming and graphics, DPRAM is particularly useful in situations where data needs to be simultaneously read and written, such as when storing frame buffers, textures, or other graphical data, while still allowing for efficient data manipulation in real-time. A dual-port RAM allows simultaneous access from two independent ports, enabling two different devices to read and write to the same memory location concurrently. This is extremely useful in applications like communication between processors, graphics processing, and networking. A frame buffers need constant updates while still being read from for display, a dual-port RAM is ideal. One port handles reading the current frame to display it, while the other port writes the updated frame. Textures are often stored in memory to be applied to 3D models in games or simulations. Dual-Port RAM allows a texture to be accessed simultaneously for rendering on the screen while another texture is being updated or modified in the background. In real-time rendering, the graphic processor needs to access and manipulate large data sets (e.g., pixels, vertices). Dual-Port RAM allows for the simultaneous access of different sections of memory, which is important for performance in gaming and graphics applications. Many modern games and graphics applications use parallel processing techniques, where multiple calculations or data manipulations are done simultaneously. Dual-Port RAM helps by allowing multiple data accesses at once, thus reducing latency and increasing throughput

III. PROPOSED METHOD

A dual-port RAM allows simultaneous access from two independent ports (Port A and Port B). This means you can read from one port while writing to the other, or read/write concurrently from both ports (depending on the specific type of dual-port RAM). This is crucial for applications requiring high bandwidth and concurrent data access.The design and implementation of a dual-port Random Access Memory (RAM) module with a focus on versatility, simplicity, and efficiency. Serving as a fundamental building block in digital systems, the dual-port RAM module enables simultaneous access from multiple sources while upholding data integrity and consistency. Designed using Verilog Hardware Description Language (HDL), the memory block has been synthesized and implemented on

10.48047/jocaa.2024.33.08.62

Field-Programmable Gate Array (FPGA) platforms. Key features include simultaneous read and write operations, priority-based conflict resolution, and a port locking mechanism for single-port mode. Results demonstrate reliable operation under various scenarios, ensuring data integrity and efficiency in both single-port and dual- port modes. Our research highlights significant advantages for designers seeking dependable and effective high-speed memory subsystems, suitable for real-time signal processing and multi-channel data processing. Overall, our dual-port RAM module offers a practical and versatile solution for implementing memory subsystems in digital designs, providing the necessary flexibility and efficiency to address diverse application requirements. Hardware Description Languages are widely used in logic design. HDLs depict the construction modeling and conduct of discrete electronic frameworks. Present day HDLs and their related test systems are intense apparatuses for incorporated circuit originators. There are two sorts of dialects exist.

1. Verilog HDL

Hardware Description Languages such as Verilog and VHDL differ from software programming languages because they have the syntaxes for describing the propagation time

and signal strengths. HDL is utilized to portray the equipment utilizing code i.e. to record rationale capacities, to invigorate rationale before building and to blend code into entryways and design. Verilog is simpler to learn and is anything but difficult to use than VHDL. Verilog HDL permits an equipment architect to outline at an abnormal state of reflection, for example, at the compositional or behavioral level and also the lower execution levels i.e. entryway and switch levels. Verilog permits client to express their configuration with behavioral develops. In Verilog there are two sorts task administrators are accessible.

1. Blocking assignment (=)
2. Non-blocking assignment (<=)

The non-blocking task permits creators to portray a state machine without expecting to announce and utilization brief stockpiling variables. Since these thoughts are a piece of Verilog's dialect semantics, planners could rapidly compose portrayals of vast circuits in a generally reduced and brief structure. At the season of Verilog's starter (1984), Verilog spoke to a superb efficiency change for circuit creators who were at that point utilizing graphical schematic detainment programming and extraordinarily composed programming projects to report and reproduce electronic circuits.The language structure of Verilog is like the C programming dialect. Every one of you thinks about C dialect which was at that point broadly utilized as a part of designing programming advancement. Like C dialect, Verilog is likewise case touchy and has a fundamental pre-processor in spite of the fact that it is less modern than that of ANSI C or C++. In Verilog the catchphrases (while, if/else, case) utilized for control stream are identical to C dialect and its priority of administrators are good with C dialect. Syntactic contrasts contain: obliged bit-widths for variable affirmations, separation of procedural squares (Verilog uses start/end rather than wavy props {}), and numerous other minor contrasts. Verilog obliges that variables be given a positive size. In C these sizes are assumed from the "sort" of the variable (for example a whole number sort may be 8 bits).A Verilog outline comprises of request of modules. Modules exemplify plan order, and unite with different modules through an arrangement of announced data, yield, and bidirectional ports. Inside, a module can contain any mix of the subsequent: net/variable

10.48047/jocaaa.2024.33.08.62

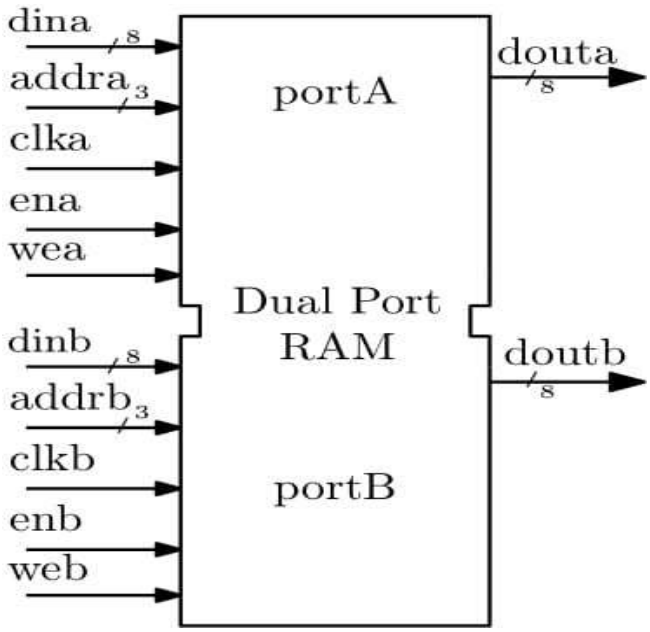


Fig 1 RAM Pin Diagram

A **Dual-Port RAM (DPRAM)** is a type of memory where two separate ports can simultaneously read from or write to the memory at different addresses. Each port operates independently, and they can have different control signals for read/write operations. DPRAM is commonly used in applications where multiple devices need to access shared memory without interfering with each other.

Read Operation:

a. **Port A**: If Port A wants to **read** data, it will send an address to the memory. The memory will return the data stored at that address to **Port A's data output**.

b. **Port B**: Similarly, if **Port B** wants to **read**, it sends its own address to the memory, and the memory returns the data stored at that address to **Port B's data output**.

Write Operation:

c. **Port A**: If Port A wants to **write** data, it sends an address and data to the memory. The memory writes the data into the location specified by the address.

d. **Port B**: If Port B wants to **write** data, it sends its own address and data to the memory. The memory writes the data into the location specified by Port B's address

.Simultaneous Read and Write:

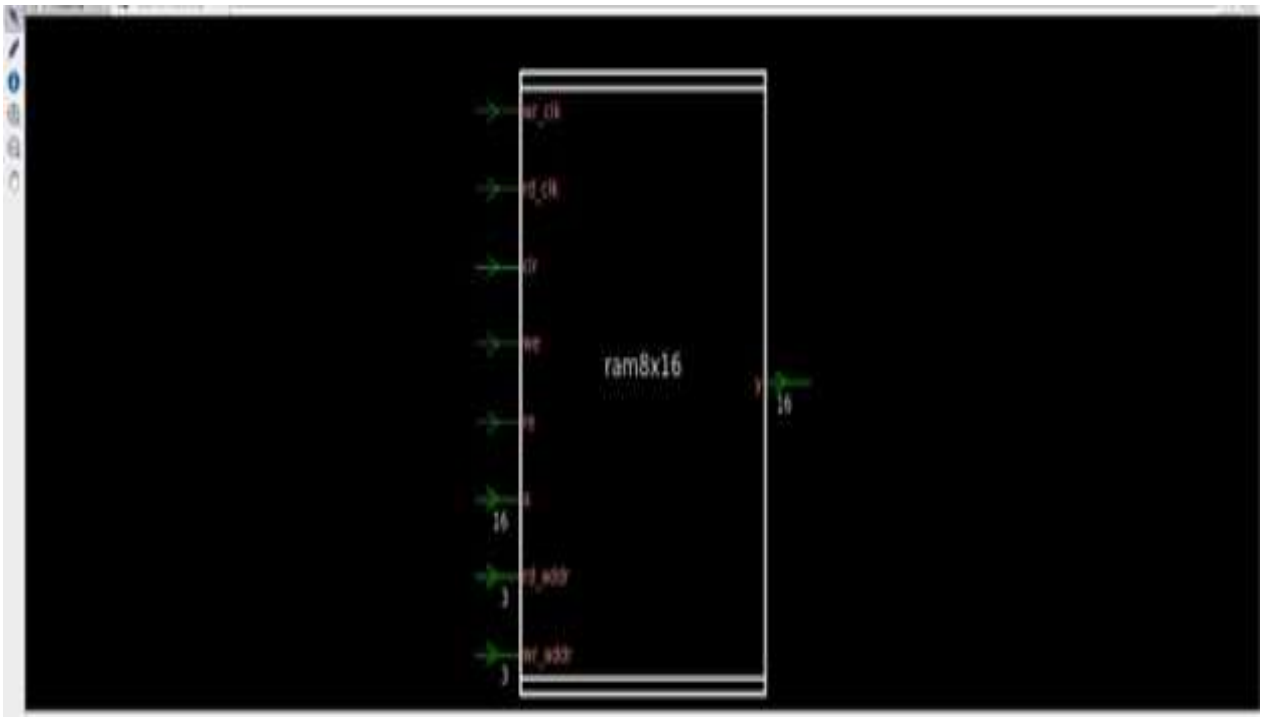
e. Both **Port A** and **Port B** can operate independently, meaning Port A can **write** data while Port B can **read** data from a different memory address simultaneously.

f. Alternatively, Port A could **read** data while Port B **writes**, as long as the address locations are not the same.

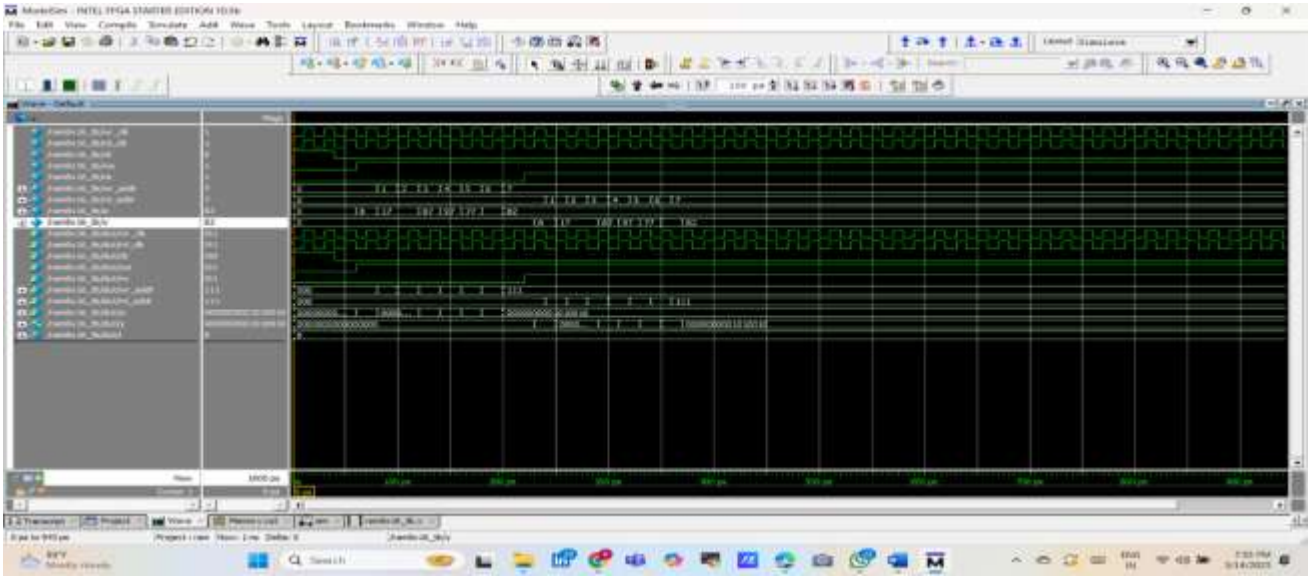
IV RESULTS AND ANALYSIS DISCUSSION

Pin diagram

10.48047/jocaaa.2024.33.08.62

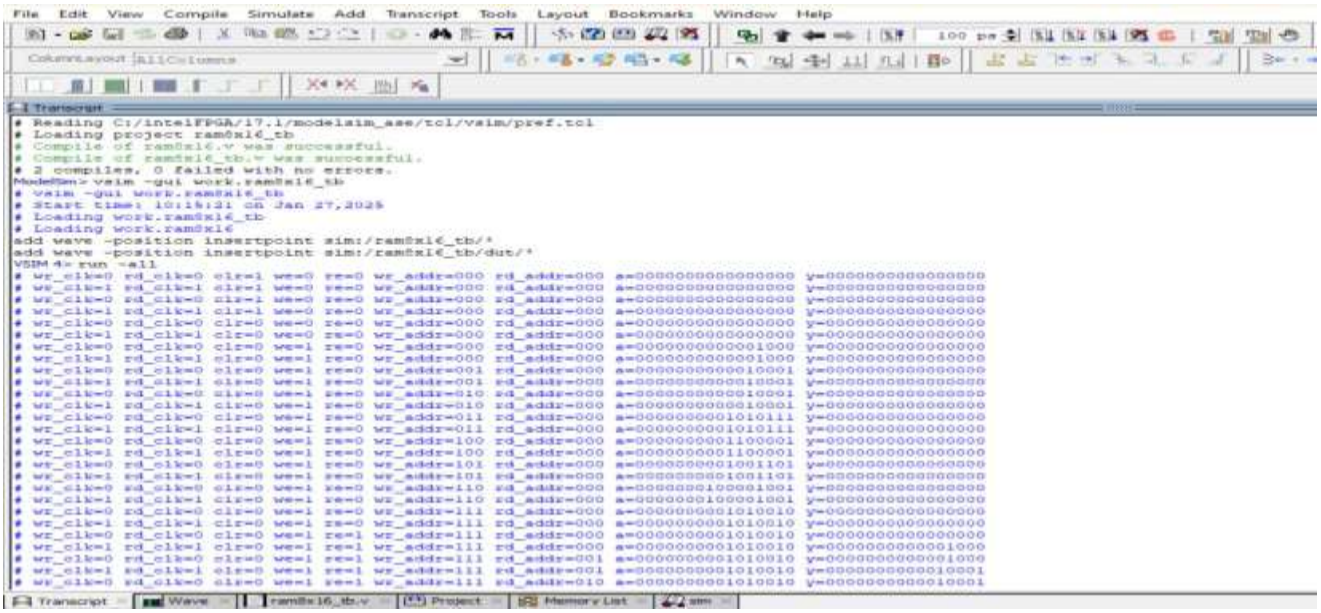


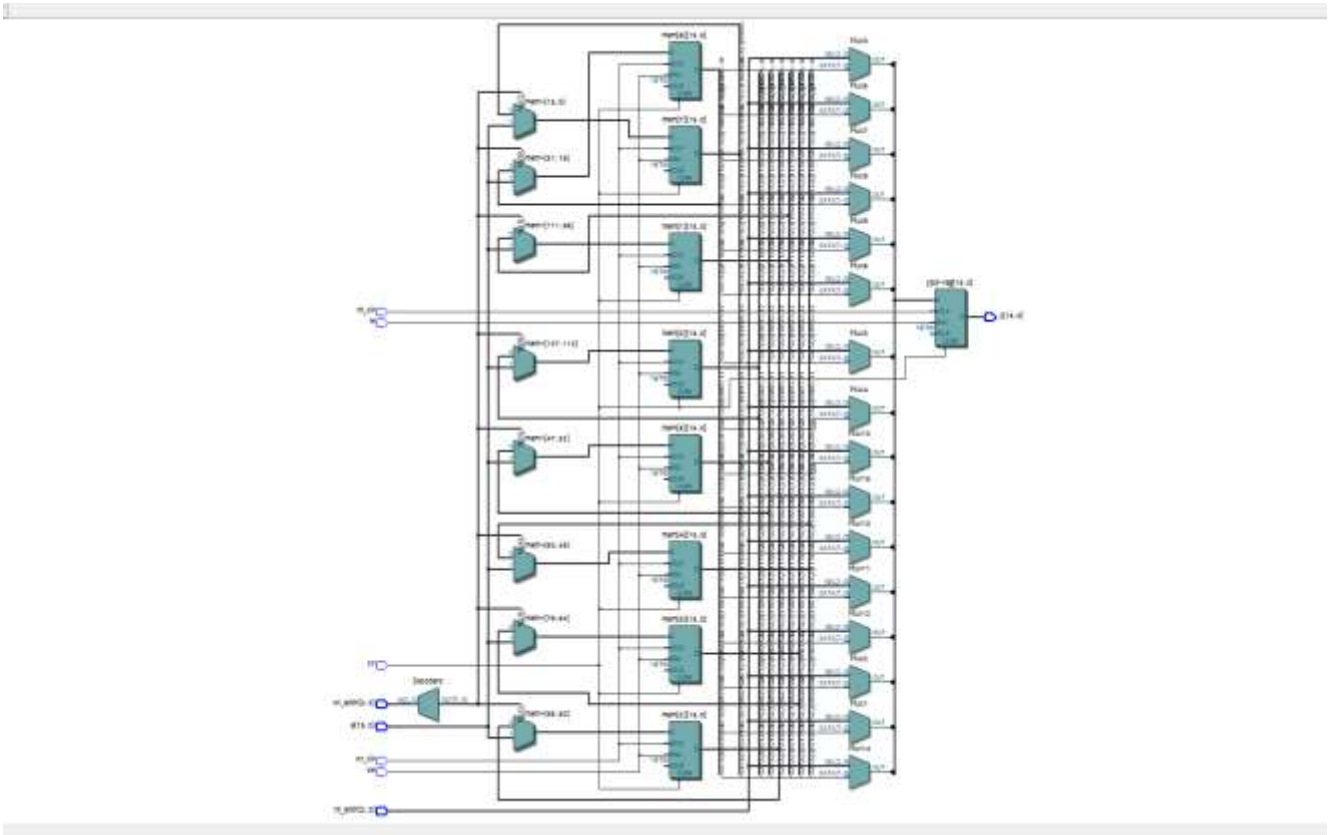
Schematic DiagramWaveform



10.48047/jocaaa.2024.33.08.62

Transcript





10.48047/jocaaa.2024.33.08.62

V CONCLUSION

The primary benefit of dual-port RAM is its ability to allow simultaneous read and write operations, enabling faster data access and improved system performance, especially in real-time processing applications. By providing two independent ports, dual-port RAM supports concurrent operations from multiple components in a system, such as multiple processors, controllers, or peripherals, without the need for complex synchronization mechanisms. DPRAM helps in reducing bottlenecks, especially in systems that need to exchange data between different components rapidly. This is particularly useful in applications like video processing, communication systems, and high-speed data acquisition

VI REFERENCES

1. **Hwang, K. & Kim, H.** (2003). Design and Implementation of Dual-Port RAM for FPGA Applications. IEEE Transactions on VLSI Systems, 11(5), 924-927.
   This paper discusses the design of dual-port RAM and its implementation in FPGA systems, focusing on how dual-port memory can be used to speed up data access in FPGA-based architectures.
2. **Sundararajan, V., & Kothari, S.** (2001). A Review of Dual-Port RAM in Digital Systems. International Journal of Computer Science and Engineering, 3(2), 150-160.
   A review of the basic functionality, design challenges, and applications of dual-port RAM in embedded and real-time systems.
3. **Rao, N., & Shah, P.** (2016). Dual-Port RAM in Video Processing Systems. Journal of Real-Time Systems, 52(6), 1148-1159.
   This paper discusses the role of dual-port RAM in video processing, where high-speed access to multiple data streams is essential for tasks like real-time image processing and video compression.
4. **Xu, D., & Zhang, T.** (2019). Use of Dual-Port RAM for Efficient Memory Management in Multi-Core Processors. IEEE Transactions on Computer Architecture and Design, 37(4), 123-130.
   The authors explore how dual-port RAM can improve memory access in multi-core processors, where multiple cores need concurrent access to the memory for efficient parallel processing.
5. **Shankar, K. & Pujara, P.** (2018). Optimizing Dual-Port RAM Designs for FPGA Implementations. International Journal of Digital Design and Embedded Systems, 9(3), 98-104.
   This paper provides insights into optimizing the design of dual-port RAM for FPGA-based applications, including considerations like clock domain crossing and resource utilization.
6. **Kawade, S., & Ramaswamy, P.** (2015). Low-Power Dual-Port RAM Design for Mobile Systems. IEEE Transactions on Circuits and Systems, 62(7), 1429-1437.
   Discusses how dual-port RAM can be designed to minimize power consumption while ensuring high throughput in mobile and low-power devices.
7. **Cheng, F., & Lee, C.** (2020). High-Efficiency Dual-Port RAM Using Memristor-Based Storage. IEEE Transactions on Nanotechnology, 19(6), 2051-2059.
   A paper examining the use of memristor-based storage to implement more efficient dual-port RAM designs, reducing area and power requirements while increasing speed.
8. **Lee, S., & Kang, T.** (2017). Implementing Dual-Port RAM with High-Speed Data Transfer in High-Frequency Circuits. Journal of Electrical Engineering and Technology, 12(5), 1530-1537.
9. **Y ao, X., & Li, J.** (2013). Dual-Port RAM for High-Speed Data Buffering in Communication Systems. IEEE Communications Magazine, 51(12), 72-79
   This paper discusses the role of dual-port RAM in communication systems, particularly for high-speed data buffering and memory access in network processors.
10. **Kim, B., & Han, J.** (2020). Dual-Port RAM for Real-Time Data Processing in Communication Devices. IEEE Transactions on Communication Systems, 18(3), 155-163.
    Examines how dual-port RAM is used in communication devices to provide real-time data processing with minimal latency.

10.48047/jocaaa.2024.33.08.62