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FULL CUSTOM DESIGN AND IMPLEMENTATION OF HIGH PERFORMANCE ADDER

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Abstract:

In this paper we present the design of a 10 transistor (10T) full adder optimized for low power and low area, suitable for portable and energy efficient VLSI applications. The design utilizes two XOR gates and one multiplexer, to minimize transistor count while achieving correct logical functionality for SUM and Carry outputs. Adders, are commonly found in the critical path of many ALUs, processors, and digital signal processing chips. As a result, each of these blocks should execute efficiently and precisely on their own, enhancing the overall performance of the system. Optimizing an adder may lead to overall system optimization. A desirable adder meets all the criteria, such as high speed, low-power dissipation, low leakage power, and small area. However, because there is a trade-off between the area, power and, speed. Obtaining the finest adder in terms of speed, power dissipation, leakage power, and area consumed would assist the designer in selecting an adder for the given application. The architecture is validated with schematic analysis, layout which tells us about the silicon area and performance comparison with conventional full adder designs.

Keywords:10 transistor adder, full custom, optimization.

INTRODUCTION:

(i) XOR gate

The fundamental functions for many circuits like adders, comparators, subtractors, parity checkers, multipliers, full adders, etc. are exclusive-OR (XOR) and exclusive-NOR (XNOR). There are two types of MOS i.e. the p-channel Metal Oxide Semiconductor (PMOS) and the n-channel Metal Oxide Semiconductor (NMOS). It is known that NMOS transistor is able to transmit the "LOW" signal (or “0") completely and it shows poor performance when the "HIGH" signal (or "1") has to be transmitted. If a switch device has to be implemented using a NMOS transistor, a control signal should be added to the terminal of gate and sets one of its end at "HIGH", whereas other end will fall to threshold voltage of NMOS, VNth. The PMOS transistor can easily transmit a "HIGH" signal completely but it can barely handle a "LOW" signal. In a switch device, if a signal goes "LOW" at the source of PMOS transistor, the other end will not sink to "LOW" signal, as it could not fall below threshold voltage of PMOS, VPth. MOSFET scaling has many advantages like higher speeds, lower power dissipation and higher packaging density. The concept behind MOSFETs scaling is the various parameters of the

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MOSFETs structure for better functioning of the device.

Dissipation in power can be determined by using some methods like node capacitances where node capacitance is made of gate, diffusion and wire capacitances, switching activity and size of control circuit.

There are three main components of power dissipation in (CMOS) circuits:

Switching Power: Power that is consumed by circuit node capacitance when transistor switching is done;

Short Circuit Power: Power that is consumed due to the current flow from power supply to ground when the transistor switching process in ON;

Static Power: Power dissipation because of leakage in circuits and static currents.

The above mentioned first two components are said to be **dynamic power**. Dynamic power comprises the major part of the power dissipation in VLSI circuits. Dynamic power is the power dissipated at the time of charging and discharging the load capacitance in given circuit. Average power dissipated in a general digital CMOS circuit is given by:

Here,

$$P_{total} = P_{dynamic}\,(P_d) + P_{static} + P_{short\text{-}circuit}$$
$$= V_{DD} \cdot f_{clk} \cdot \sum (V_{iswing} \cdot C_{iload} \cdot \alpha_i) + V_{DD} \cdot \sum I_{isc} + V_{DD} \cdot I_l$$

f_{clk} = system clock frequency, V_{iswing} = voltage swing at node i,
C_{iload} = load capacitance at node I, α_i = activity factor at node i.

I_{isc} = short circuit current and I_l = leakage current.

Today the main concern issues for designing any CMOS circuit are power, delay and silicon area of the chip. Transmission gate is also used in designing of XOR/XNOR circuit because transmission gate has high switching speed, requires less power and gives less delay.

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Functions of XOR and XNOR gate

(ii)Multiplexer

The multiplexer is an essential element in the networking of communications. A combination circuit is a multiplexer which transforms serial data to parallel data. Multiplexer's major role is to integrate numerous users (or channels) into a single data transmission line to enhance this channel's efficiency. The 2:1 MUX has an output, two inputs and a line. The specific input is picked and sent to the output according to the binary value of the selected line.

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Multiplexer is a universal combination circuit for all logical gates. The multiplexer is a 2nd input, n' select and single output line digital switchover. The output is created by connecting to the selected data entry line in accordance with the binary combination of the selected lines. 2:1 MUX features two input data lines, one selected line and one output line. If the select line's binary value is logical '0,' the input D0 is transferred to the output line. The data line D1 is then linked and sent to the output line when the binary value for the select line is logic '1.' Block diagram 2:1 MUX and Boolean expression is as follows: Figure 1 shows Boolean expression and block diagram 2:1 MUX [15].

$$Y = D0S^{-} + D1S$$

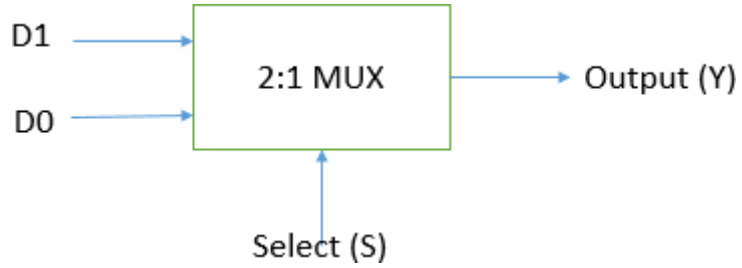

Fig 1: Basic 2:1 Multiplexer

Figure 2 provides the following logic circuit of 2:1 MUX with the fundamental logic gates i.e. AND, OR and NOT gates:

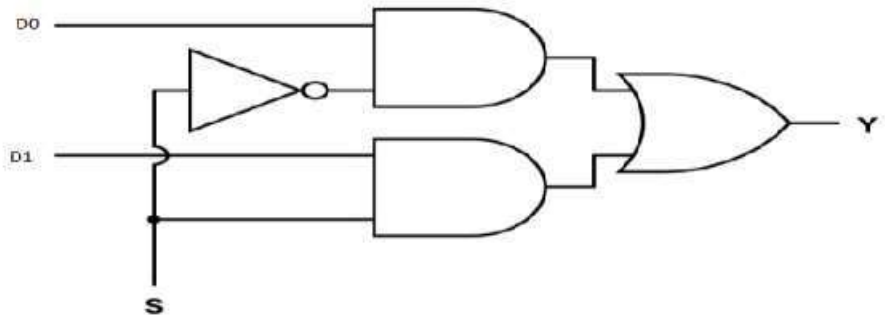

Fig 2: Logic Circuit of 2:1 MUX.

The truth table as given in Table 2 shows all conceivable combinations of the selected line and the data supplied. From the table it can be easily deduced that if the selected line is of low logic, output is the same as data entering D0 regardless of the values of other data entry. Likewise, whatever the value of the D1 data line may be, the resulting output will then show the same value as the D1 data input if the selected line is in high logic [16].

S	D0	D1	Y
0	0	0	0
0	0	1	0
0	1	0	1

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0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 2: Truth Table of 2:1 MUX.

(iii)ADDER

1-bit full adder cell is a basic element used in circuits like multipliers, comparators, differentiators, integrators, subtractors, etc. It is used to design microprocessors, digital signal processors, etc. to achieve arithmetic operations. The performance of these processors is highly dependent on the 1-bit full adder cells [6–9]. In recent years, research communities are showing their keen interest to propose several kinds of different logic styles for implementing 1-bit full adder cell [10]. The objective of this work is to achieve output levels as close to voltage rails as possible. At the same, it also aims to achieve ultralow power consumption and area.

This paper is organized as follows. Section 1 briefly discusses about existing full adder circuits. In Section 2 full adder architecture is explained. In section 3 the proposed full adder circuit is presented. Simulation environment is shown in Section 4. Simulation results are presented in Section 5. Finally, conclusions and comparison are drawn in Section 6.

Related works:

The single-bit full adder cell is essential for performing different arithmetic operations. As a result, improving the effectiveness of the full adder cell could be critical in improving the general functioning of the system. In the field of research, several complete adder designs employing various logic styles and technological advances have been described. Numerous designs have been constrained to a solitary logic style, but others incorporate multiple logic styles [12]. While the essential function of all full adder designs constitutes the same, every design has unique benefits and drawbacks depending on performance parameters such as the number of transistors, delay, and power usage.

The dominant technology is the static CMOS 1-bit full architecture, as described in [17]. The design comprises 28 transistors that are similar to a typical CMOS arrangement. The flexibility of this design to respond effectively to changes in supply voltage scalability and transistor scaling is its primary benefit. It also has complete swing logic necessary for creating complex combinations. The high input capacitance of this design necessitates the employment of larger PMOS transistors, leading to a more significant physical dimension. The mirrored adder has evolved into a sophisticated structure with power consumption and several transistors comparable to a static CMOS complete adder design. Nonetheless, it outperforms CMOS regarding carry propagation delay [18]. The CPL adder, which is also extensively used, employs 32 transistors [9,19]. Pass transistor logic, as opposed to CMOS, combines the connection of the pass transistor's supply to different input signals, as opposed to the inclusion of supply lines, the growing transistor count, and the many intermediary switching nodes. Full adders based on transmission gate logic are presented as a possible solution to the voltage

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deterioration issue encountered in PTL circuits [20,21].

This section addresses the -1-bit adder architectures illustrated in Figs. 3–7 [23-26]. The designs depicted in Figs. 6–9 exhibit suboptimal performance in the deep subthreshold regime. Subsequently, more scholarly investigations on hybrid full adders were produced to minimize the dimensions, latency, and energy consumption [21–26]. Consequently, it is determined that the 6T full adder units are either entirely nonoperational or yield suboptimal output values. The output voltage levels of the designs depicted in Figs. 8 and 9 are characterized by full swing. Nevertheless, it is imperative to note that both devices require a substantial silicon area due to including 28 and 24 transistors, respectively.

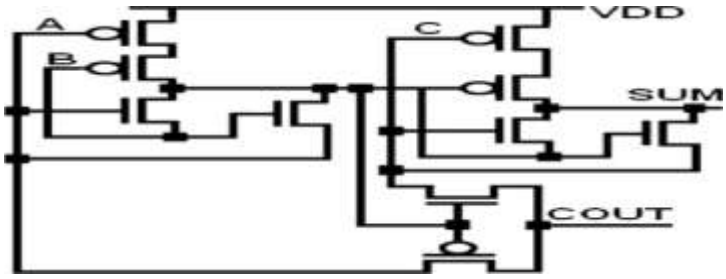

Fig. 3: 10T Adder-1 [24].

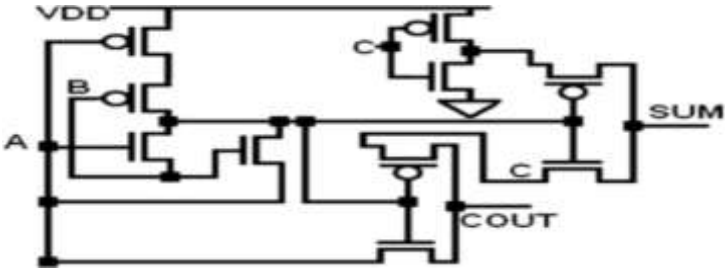

Fig. 4: 10T Adder-2 [25,26].

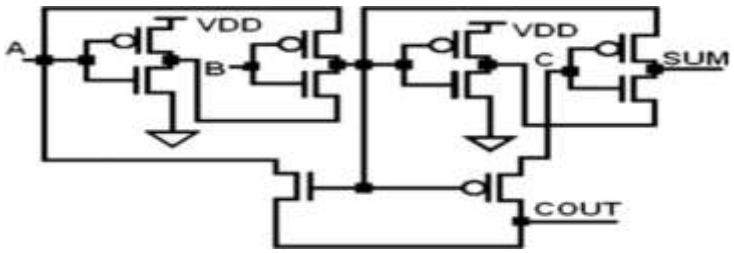

Fig. 5: 10T Adder-3 [25,26].

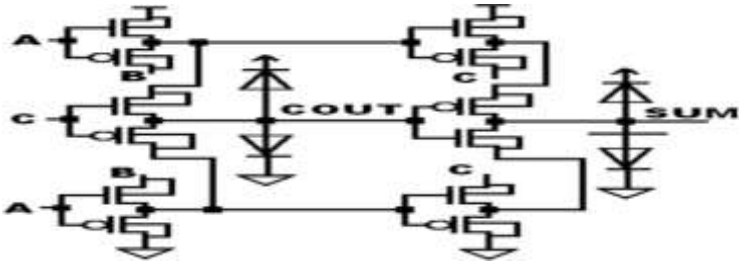

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Fig. 6: 20T Adder [22].

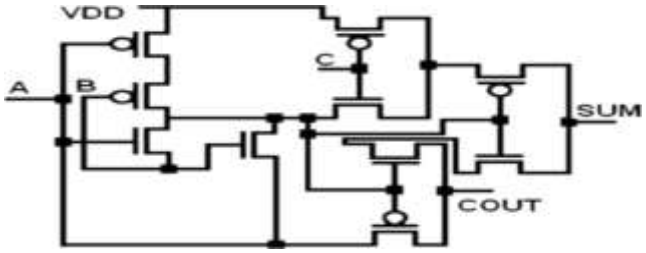

Fig. 7: 10T Adder [22].

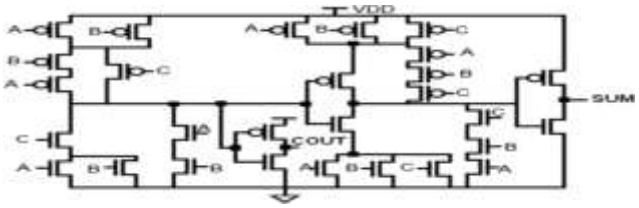

Fig. 8: 28 T full adder [23].

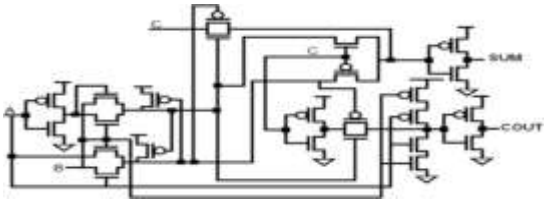

Fig.9: 24 transistors full adder [23]

FULL ADDER ARCHITECTURE:

Power can be minimized at either system level or architecture level or algorithm level or micro architecture level or gate level or circuit level. Here, we made an attempt to reduce the power at circuit level. Each design consists of number of micro architectures. Each micro architecture consists of number of gates. For CMOS implementation of the gate, the pull-up and pull- down of the circuit must be realized. A conventional full adder with XOR gates, AND gates and OR gates must be realized with corresponding pull-up networks, and pull-down networks. A conventional CMOS full adder consists of 28 transistors [3]. But, here we have designed a full adder only with 10 number of transistors, which occupies very less area and also consumes very less power. The adder is one of the most important components of a CPU. Multipliers, Arithmetic logic unit (ALU), floating-point unit and address generation like cache or memory access unit use it. In addition, full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors also it is useful.

Arithmetic functions such as addition, subtraction, multiplication and division are some examples, which use adder as a main building block [9]. As a result, design of a high-performance full-adder is very useful and important. On the other hand, increasing demand for portable equipment such as cellular phones, personal digital assistant (PDA), and notebook personal computer, shows the need of using area and power efficient VLSI circuits [1,11]. Low-power and high- speed adder cells are used in battery operation based

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devices. The full adder performs the computing function of the multipliers and ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs [2]. Figure10 Shows the logic level diagram of a full adder. The Boolean expressions for the SUM and CARRY bits are as shown below.

SUM=AB'Cin'+A'BCin'+A'B'Cin+ABCin-------- Eq1

CARRY=AB+ACin+BCin---------- Eq2

SUM bit is the EXOR function of all three inputs and CARRY bit is the AND function of the three inputs. The truth table of a full adder is shown in Table3. The truth table also indicates the status of the CARRY bit[5]. If carry bit has been generated or deleted or propagated, depending on the status of input bits A and B, the CARRY bit is either generated or deleted or propagated. If either one of A or B input is '1', then the previous carry is just propagated, as the sum of A and B is '1'[7].

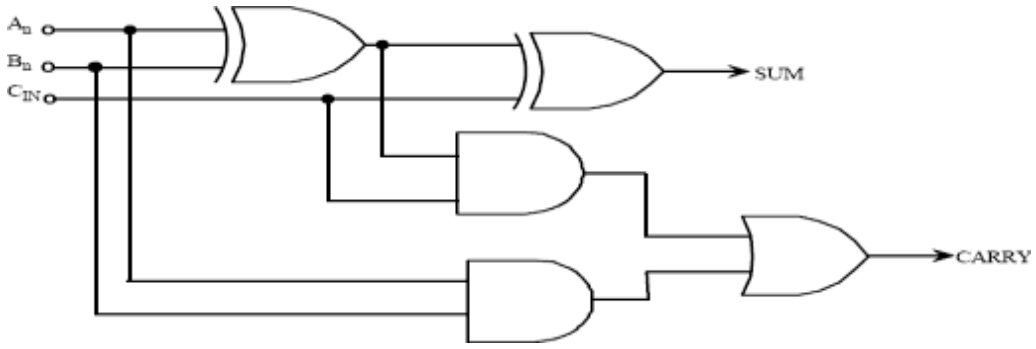

Fig10.: Logic level diagram of a full adder.

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 3: Truth table of full adder

Table 3 shows the carry status of full adder. If both A and B are '1's then carry is generated because summing A and B would make output SUM '0' and CARRY '1'. If both A and B are '0's then summing A and B would give us '0' and any previous carry is added to this SUM making CARRY bit '0'. This is in effect deleting the CARRY [8].

The conventional full adder which consists of 28 transistors is shown in figure11. Another

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full adder circuit which consists of 14 transistors using transmission gates is also shown in figure12. In Multipliers and ALU full adder forms the core of the entire design.

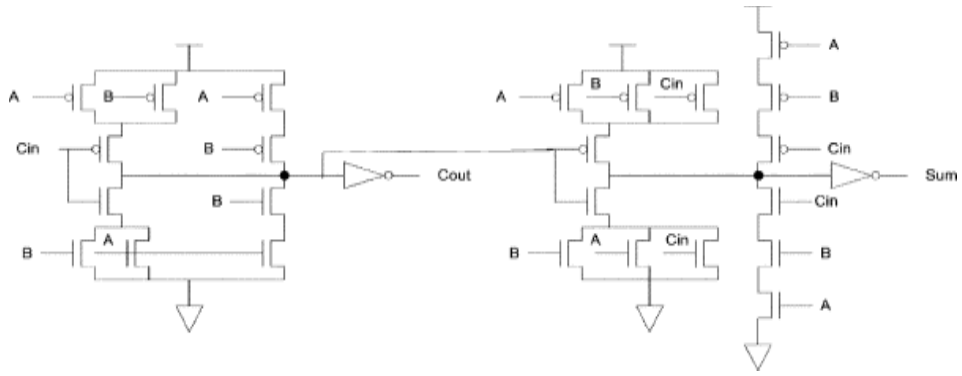

Fig11: Static complementary CMOS adders using 28 transistors

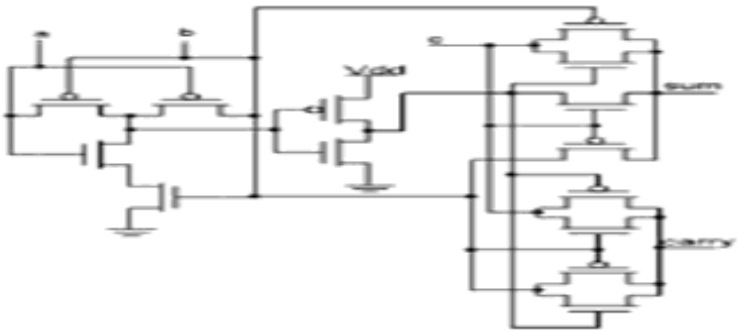

Fig12: Fourteen Transistor (14T) Full adder with Transmission Gates

Implementation: Proposed adder

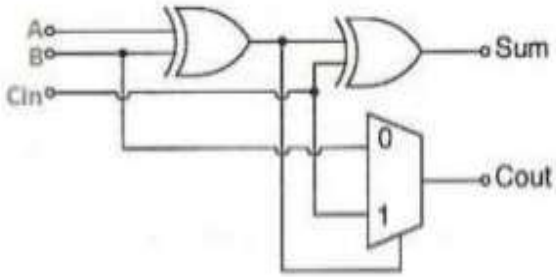

Fig.13: Proposed adder

Full adder is implemented using two xor gates and one 2:1 multiplexer [13,14]

Full adder is a combinational circuit that performs the addition operation of 3 input bits. It basically consists three inputs and two outputs. The input variables are expressed by A, B and Cin. The two output variables are expressed by sum (S) and carry (Cout) [4]. Fig. 1 shows the essential block diagram of full adder cell. The Boolean expression for full adder operation is defined below:

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A one-bit full adder is a fundamental digital circuit that perform the addition of three binary inputs: two significant bits (A and B) and an input carry (cin), producing a sum (sum) and carry output (cout).

A highly efficient implementation of the full adder can be achieved using two XOR gates and 2:1 multiplexer. The sum output is derived using the associative and commutative properties of the XOR operation. Initially the two inputs A and B are passed through the first XOR gate, producing an intermediate value of X=A XOR B. This value is XORed with Cin that is carry input using the second XOR gate to generate the final output of the Sum given by SUM=A xor B xor Cin.

The carry output cout, instead of being computed using the conventional majority logic expression (AB+BCin+ACin), is elegantly obtained using a 2:1 multiplexer. The select line of the multiplexer is driven by the same intermediate XOR output X=A XOR B when A and B are equal that is X=0, the carry output is determined by B, since both inputs are either 0 or 1, directly influencing the need for a carry. When A and B are different that is X=1, the carry out depends on the value of Cin. This logic is implemented by connecting input 0 of the multiplexer to B, input 1 to Cin, and selecting between them using the XOR output X as the control signal. Therefore, cout=(X1).A+Xcin, which is the standard 2:1 multiplexer function. This design is highly advantageous for VLSI implementations due to its reduced transistor count, lower power consumption, and smaller silicon area compared to conventional full adder designs. It is especially suitable for low power and high density arithmetic circuits in modern digital systems.

Multiplexer Schematic:

Multiplexer is designed with one PMOS and NMOS transistor. The schematic is as shown below. A0 and A1 are the two inputs and S is the select line and Y is the output**.**

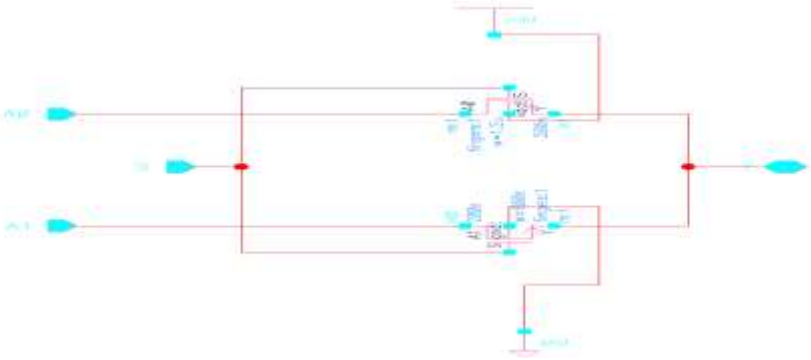

Fig.14: Schematic of multiplexer

Symbol

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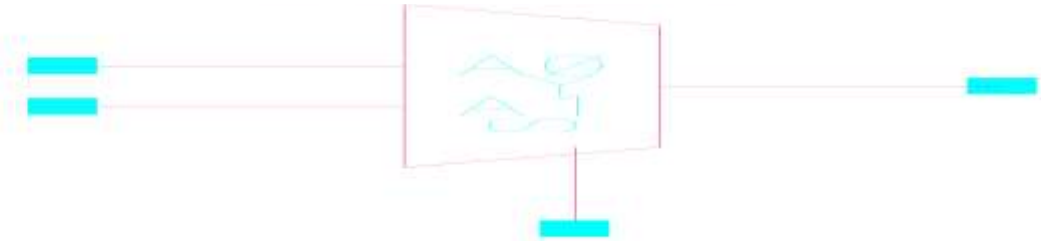

Fig.15: Symbol of multiplexer

Multiplexer Layout

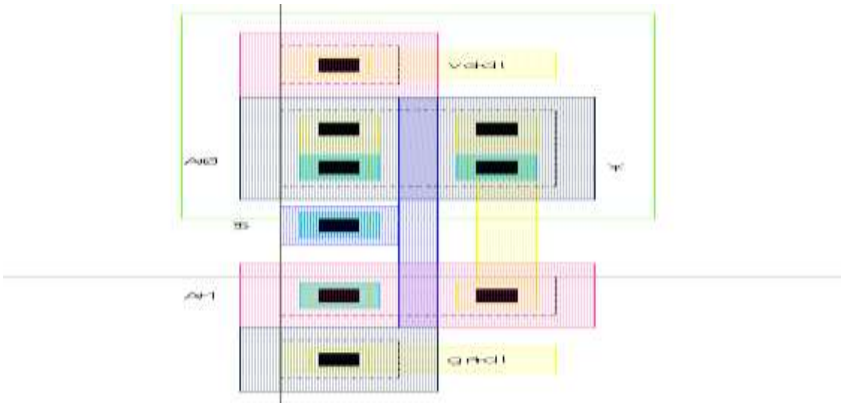

Fig.16: Layout of multiplexer

XOR Schematic

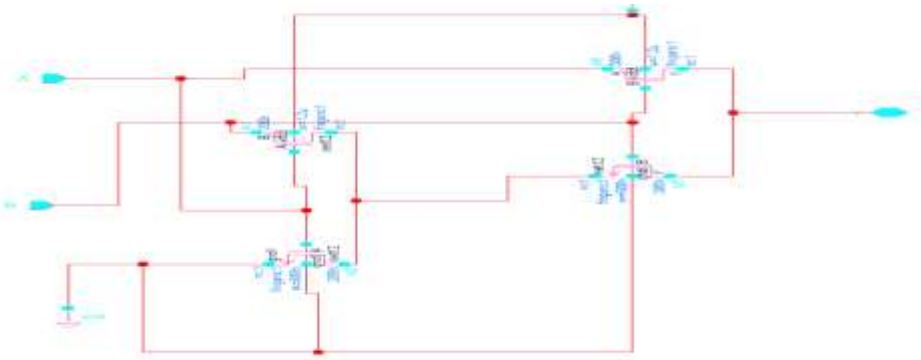

Fig.17: Schematic of XOR gate

XOR Layout

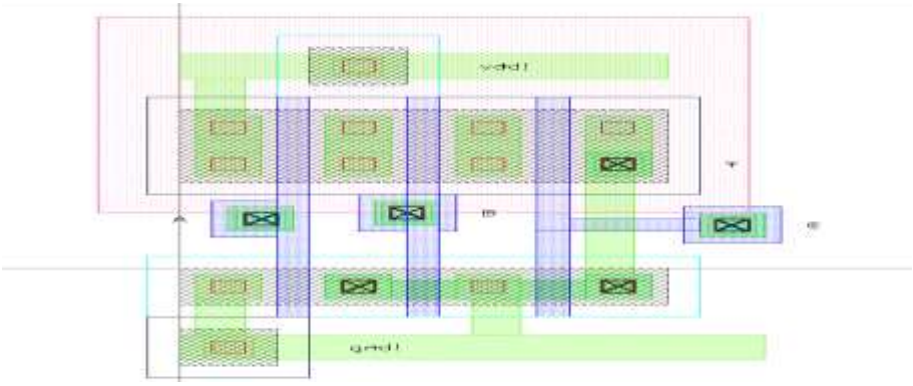

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Fig.18: Layout of XOR gate

10 transistor Adder

10 Transistor Full Adder Design(10TFA)

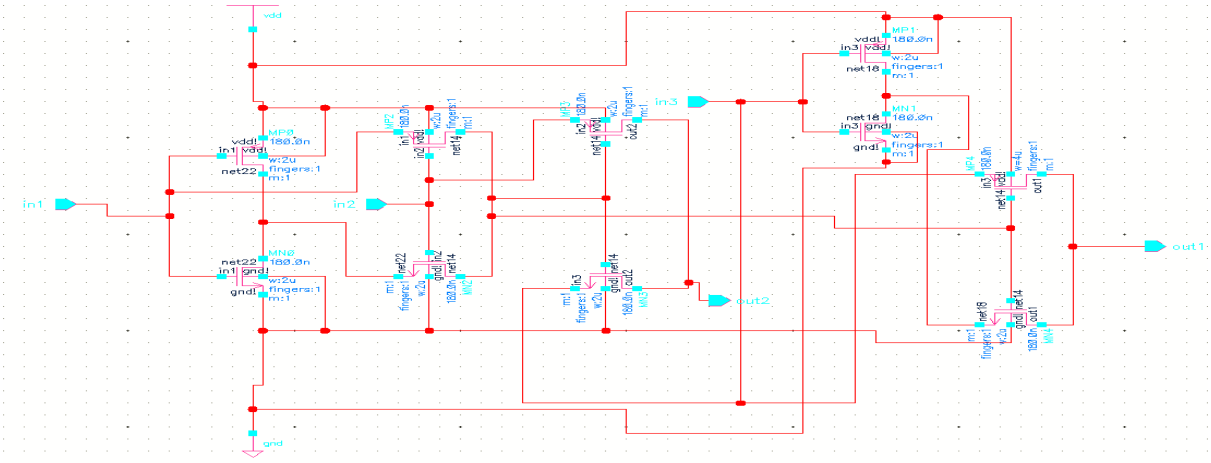

Fig.19: Schematic of Adder

symbol

Fig.20: Symbol of Adder

Layout

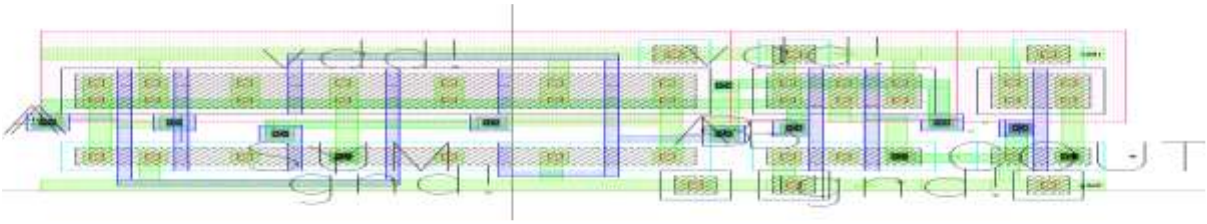

Fig.21: Layout of adder

Results:

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Simulation results of XOR Gate

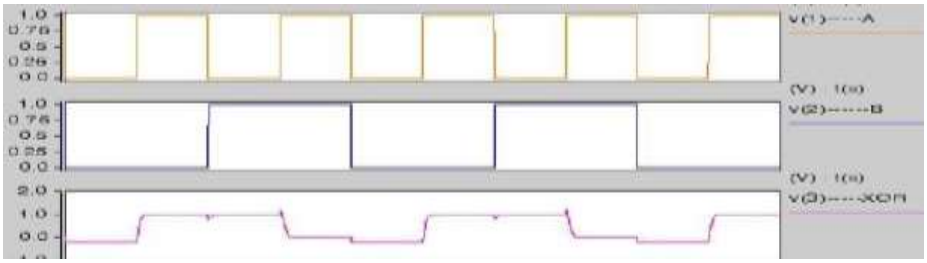

Fig.22: Simulation of xor gate

Simulation results of ADDER

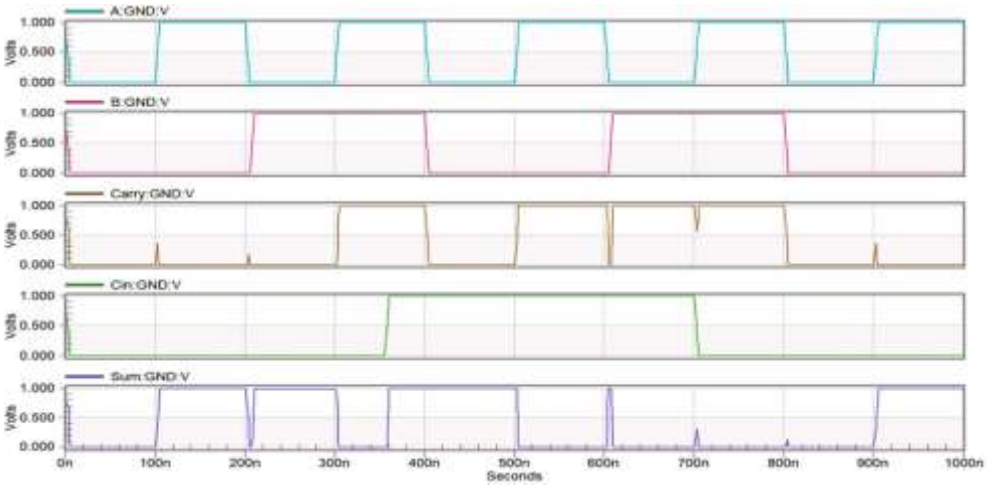

Fig.23: Simulation of one-bit adder

Conclusion:

The proposed 10TFA takes the three inputs A, B and C. The third input C represents carry input. The outputs are SUM and Cout. The adder circuit diagram of the new 1-bit full adder is shown in figure19. The designed adder implements equations 1 and 2 using XOR and MUX based design logic with 10 transistors. The full adder circuit uses 0.18µm CMOS process technology, which provides transistors with three characteristics, namely high-speed, low-voltage and low- leakage. As the main target of this design is to minimize Power, so the transistors are selected for it accordingly. The typical supply voltage for this process is 1.2V and 0.8 V. The 10- transistor 1-bit full adder is designed at transistor level, using 0.18µm CMOS process technology. Table 4 shows the comparison of proposed adder with respect to CMOS adder in terms of power consumption and performance. Table 5 shows the comparison of proposed adder with respect to the existing adders in terms of performance and average power operating at 1.2V and 0.8V.

Table 4: Performance comparison of proposed adder w.r.t. CMOS adder

	Power Consumption (W)	Delay(S)
CMOS adder	1.96e-007	27.3212n
Proposed Adder	4.211e-015	5.21n

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Table 5: Comparison of Proposed 1-bit Adder w.r.t existing adders.

Full adder	Delay (ns)		Average Power (W)	
	1.2V	0.8V	1.2V	0.8V
CPL	37.3	84.8	3.89µ	1.72µ
CCMOS	39.7	125.8	1.91µ	0.68µ
TG –Adder	58.3	139.7	1.41µ	0.64µ
TF-Adder	66.8	145.6	1.33µ	0.61µ
24T Adder	65.9	128.4	1.68µ	0.76µ
DPL Adder	45.6	91.9	2.11µ	0.87µ
Proposed Adder	5.216959	80.3	4.211899x e-015	3.244885e-016

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