10.48047/jocaaa.2024.32.01.41

AI-Engine-Based Acceleration for High-Performance Programmable System-on-Chip Designs

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1.Abstract

This research paper, titled *"Optimizing the Performance of Programmable System-on-Chip Architectures Using AI Engines"*, presents an in-depth study of heterogeneous computing platforms, which are increasingly central to modern high-performance computing (HPC) applications. With the growing reliance on GPUs, FPGAs, and data center accelerators, significant progress has been made in reducing computational latency and enhancing throughput. Architectures that integrate heterogeneous componentssuch as CPU-FPGA or CPU-GPU combinations—are now widely deployed in domains like computer vision and machine learning due to their superior parallelism, ability to manage safety-critical and latency-sensitive workloads, support for multiple instruction and data streams, compatibility with full Linux OS environments, and efficiency in processing unstructured or irregular datasets.

The project specifically explores the capabilities of the Xilinx Versal Adaptive Compute Acceleration Platform (ACAP), a heterogeneous system-on-chip (SoC) that integrates programmable logic (FPGA), dual-core ARM Cortex-A and Cortex-R processors, and an AI Engine composed of a 400-core Very Long Instruction Word (VLIW) array. The experimental setup performs large-scale matrix multiplication involving matrices with 800 elements each. Performance metrics are captured for two configurations: (1) a heterogeneous setup utilizing the AI Engine, FPGA, and CPU; and (2) a baseline using only the CPU. Comparative analysis across these configurations highlights significant performance improvements in terms of execution time, parallelism, and resource utilization.

The results clearly demonstrate the advantages of deploying heterogeneous SoC architectures over traditional standalone processors like the 64-bit ARM Cortex-A and Cortex-R. These findings underscore the transformative potential of AI-accelerated heterogeneous systems in future computational workloads.

1.1 Objective

The primary objective of this study is to showcase how incorporating an AI Engine can significantly enhance the performance of applications traditionally executed on ARM processor cores alone. By offloading computationally intensive tasks to the AI Engine, the project aims to highlight the advantages of heterogeneous processing over conventional CPU-only approaches.

This work specifically targets the following system-level challenges:

- **Optimizing Performance per Watt at the System Level**:

  Power consumption directly influences both operational and infrastructure costs, particularly due to the demands for advanced cooling solutions. Enhancing compute efficiency per unit of power is therefore critical to achieving scalable and cost-effective high-performance systems.

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- **Energy-Efficient Computation and Data Movement**:
  Although traditional programmable logic offers great flexibility, it often incurs substantial power overhead. In contrast, implementing functions using hardened hardware blocks—such as those within AI Engines—can deliver up to ten times better power efficiency compared to general-purpose programmable logic.
- **Addressing Metal Scaling Limitations in Programmable Logic**:
  Field Programmable Gate Arrays (FPGAs) frequently suffer from metal scaling constraints due to their complex and extensive interconnect structures. These limitations can lead to performance degradation, especially when compared to Application-Specific Integrated Circuits (ASICs). The AI Engine offers an optimized architecture that mitigates such issues, improving both scalability and processing density.

1.2 Motivation

The inspiration for undertaking this project arises from a strong interest in exploring heterogeneous computing architectures that integrate traditional processors with programmable logic (PL), such as FPGAs, and specialized accelerators like AI Engines. As computational workloads continue to grow in complexity and scale, there is an urgent need for novel computing paradigms capable of meeting the intensive demands of next-generation applications. Conventional processor architectures alone are insufficient to sustain this growth, making it imperative to adopt scalable and energy-efficient alternatives.

By leveraging the AI Engine as a core accelerator within a heterogeneous System-on-Chip (SoC), this project aims to showcase the tangible benefits of such architectures in real-world applications. The matrix multiplication task implemented on the AI Engine not only serves as a proof of concept but also highlights the significant performance improvements achievable through parallel processing and hardware specialization.

1.3 Background

The demand for real-time, power-efficient, and flexible computing has given rise to heterogeneous processing systems that integrate conventional CPUs with programmable logic (PL) and specialized accelerators. Traditional single-architecture systems are increasingly incapable of meeting the performance and energy efficiency required by emerging applications such as advanced driver assistance systems (ADAS), sensor fusion platforms, and machine learning inference engines. These applications demand not only high throughput but also the ability to process irregular data types, manage diverse instruction sets, and perform complex algorithms while operating under tight latency constraints. Additionally, domain-specific parallelism and the need to leverage complete Linux OS services drive the adoption of heterogeneous systems. An added advantage is the reprogrammability of such platforms, allowing them to evolve over time with changing workloads and optimization needs. Factors such as form-factor limitations and integration flexibility also make heterogeneous system-on-chip (SoC) solutions a compelling choice for future-ready embedded systems.

1.4 Problem Statement

Modern computational systems face increasing demand for high-throughput, low-latency, and power-efficient performance, particularly in domains such as machine learning inference, signal processing, and embedded AI. Traditional CPU-only architectures, while flexible and general-purpose, often fail to meet the real-time processing needs of these workloads due to limited parallelism and suboptimal performance-per-watt characteristics.

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Similarly, while Field Programmable Gate Arrays (FPGAs) provide customizable acceleration, they are constrained by metal scaling limitations, complex interconnect structures, and higher power overhead when used for general-purpose logic.

These limitations necessitate a shift toward heterogeneous computing platforms that can effectively combine the strengths of general-purpose CPUs with specialized accelerators such as AI Engines and programmable logic. However, integrating these diverse components into a unified, efficient system introduces several challenges—including workload partitioning, memory hierarchy optimization, synchronization overhead, and communication bottlenecks.

This research addresses these gaps by exploring the use of the Xilinx Versal Adaptive Compute Acceleration Platform (ACAP), a next-generation heterogeneous System-on-Chip (SoC) architecture that integrates CPUs, programmable logic, and AI Engines into a single unified fabric. The objective is to assess whether this hybrid architecture can overcome the power, performance, and scalability bottlenecks associated with conventional systems—thereby delivering improved compute efficiency, lower latency, and enhanced parallel processing capabilities for high-density workloads such as large-scale matrix multiplication.

1.5 Hypothesis and Research Questions

This study is based on the hypothesis that integrating the AI Engine within a heterogeneous System on Chip (SoC) architecture, such as the Xilinx Versal ACAP, can deliver substantial performance improvements over conventional CPU-only systems. Specifically, we hypothesize that leveraging the AI Engine alongside the programmable logic and ARM Cortex-A72 processing system will result in at least a 20× speedup in executing large-scale matrix multiplication tasks. This hypothesis stems from the architectural advantages of the AI Engine, including its support for Very Long Instruction Word (VLIW) parallelism, high-bandwidth memory access, and efficient inter-tile communication.

To validate this hypothesis, the study is guided by four central research questions. First, can the AI Engine integrated within the Versal ACAP significantly reduce execution time for compute-intensive workloads compared to a standalone ARM-based implementation? Second, how does the inclusion of the AI Engine impact power efficiency and performance-per-watt at the system level? Third, what role does the AI Engine's internal parallelism and optimized memory access pattern play in improving computational throughput? Finally, what architectural or implementation-level trade-offs arise when deploying heterogeneous acceleration using AI Engines as opposed to traditional CPU or FPGA-only designs?

Answering these questions through experimental validation and system analysis forms the core motivation of this work and provides insights into the practical viability of AI-accelerated heterogeneous computing for real-world embedded applications.

2. Project Description and Goals

This research, was conceived as a technical proof-of-concept to explore the performance gains achievable by integrating AI accelerators within a programmable heterogeneous SoC architecture. The application developed for this study focuses on large-scale matrix multiplication, involving two 800×800 matrices, and is executed in two distinct configurations. The first configuration runs the workload solely on an ARM-based processing system, while the second utilizes a combination of the CPU, FPGA fabric, and the AI Engine embedded within the Xilinx

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Versal ACAP platform. The project was deployed on the Xilinx VCK190 board, which incorporates the Versal Adaptive Compute Acceleration Platform — a heterogeneous SoC that offers hardened processing cores, reconfigurable logic, and a dedicated AI Engine comprising 400 VLIW cores designed for parallel computation. The project aimed to evaluate and compare system performance across several key parameters, including initialization time, execution time, data movement latency, DMA buffer descriptor chaining, result reordering efficiency, and PL I/O throughput. By leveraging the FPGA for efficient data transfer and the AI Engine for high-throughput parallel computation, the experiment demonstrated the architectural advantage of heterogeneity in minimizing processing bottlenecks and energy consumption. The outcomes underscore the value of incorporating specialized accelerators in compute-intensive workloads, laying the groundwork for broader adoption of such platforms in embedded AI systems.

3. Related Works

The increasing computational demands of modern applications have driven the research community to explore hardware acceleration techniques, particularly using Field Programmable Gate Arrays (FPGAs) and heterogeneous System-on-Chip (SoC) architectures. Numerous studies have showcased the potential of FPGAs in accelerating deep learning and compute-intensive applications. Yu et al. presented an FPGA platform for data-center CNN workloads that achieved up to 4.2 TOP/s in 16-bit operations while significantly reducing latency compared to GPU-based solutions [1]. Similarly, Carreras et al. explored the deployment of temporal convolutional networks on FPGAs, highlighting the adaptability and performance efficiency of reconfigurable logic for time-series applications [2]. Qin et al. provided a comprehensive survey of FPGA-based deep learning accelerators, discussing architectural patterns, memory optimizations, and data reuse strategies [3]. Dirkson et al. evaluated approximate multipliers and accumulators in CNN accelerators implemented on FPGA and demonstrated improvements in area and energy efficiency [4].

In the financial domain, Hossain et al. implemented Monte Carlo simulations on FPGAs for option pricing, achieving considerable gains in speed and energy efficiency over CPUs [5]. A similar approach using GARCH models on a Maxwell FPGA supercomputer also reported over 100× acceleration, reinforcing FPGAs' role in quantitative finance [6]. From a design methodology standpoint, Cong et al. illustrated the practicality of Xilinx Vivado High-Level Synthesis (HLS) in translating C++ code to hardware, streamlining development workflows [7]. Hauck et al. quantified the performance and resource utilization trade-offs between HLS-generated and manually written HDL for FPGA ML applications, showing that while hand-coded logic remains more optimized, HLS is a viable choice for rapid prototyping [8].

Carrilho et al. deployed object detection CNNs such as YOLO on Zynq-based SoCs, demonstrating the feasibility of real-time aerial surveillance using quantized models [9]. The ALAMO framework further expanded on scalable design by introducing reusable layers across CNN architectures for deployment on FPGA platforms [10]. A CEUR-WS survey detailed optimization techniques like pruning and quantization for deep learning models implemented on FPGAs, emphasizing memory efficiency and latency control [11]. ACM's review of over 120 FPGA-based neural network accelerators classified challenges in throughput, latency, and logic mapping, particularly under dynamic workloads [12].

Stony Brook University researchers proposed resource partitioning techniques to increase CNN accelerator efficiency through optimized mapping and reuse, which proved critical for layered architectures like ResNet and

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VGG on FPGAs [13]. Other works applied metaheuristics such as simulated annealing and tabu search for resource-constrained CNN accelerator scheduling, yielding notable performance improvement [14]. Researchers at Peking University demonstrated end-to-end CNN acceleration on the Xilinx VC707 board, benchmarking models such as VGG16 with high throughput [15].

More recent work published by MDPI focused on a parallel-mapped convolution framework to boost speed and reduce power consumption in FPGA-based inference systems [16]. CEUR-WS authors explored flexible convolution implementations to adapt FPGA logic to irregular kernel patterns, thereby supporting dynamic workloads in embedded applications [17]. The HLS4ML initiative at CERN automated the translation of scikit-learn and Keras models into synthesizable HDL, making ML model deployment on FPGAs much more accessible to scientists and engineers..

Boutros et al. conducted an extensive study on hybrid FPGA-AI Engine architectures, analyzing various integration strategies for edge and embedded use cases where latency and power constraints dominate design trade-offs. Finally, Jiang et al. compiled a detailed review of CNN acceleration frameworks on FPGA, focusing on hardware–software co-design and the importance of optimized dataflows and pipelining techniques in high-performance deployments

4. Technical Specification and System Architecture

The Versal Adaptive Compute Acceleration Platform (ACAP) from Xilinx integrates multiple processing elements into a unified architecture that combines Scalar Engines, Adaptable Engines, and Intelligent Engines. This heterogeneous compute fabric is supported by an advanced network-on-chip (NoC) and multiple memory and interconnect technologies. The combination enables a highly parallel and flexible platform suitable for compute-intensive applications ranging from AI inference to signal processing. The Scalar Engines in the Versal device include high-performance ARM Cortex-A72 cores for general-purpose processing and Cortex-R5F cores for real-time tasks. The Adaptable Engines consist of programmable logic blocks and memory elements optimized for data-parallel compute operations. The Intelligent Engines are composed of AI Engines and DSP blocks capable of handling fixed-point, floating-point, and complex multiply-accumulate (MAC) operations, offering extensive support for SIMD and VLIW processing.

At the heart of the Versal ACAP lies the AI Engine array, a grid of interconnected AI Engine tiles that serve as parallel compute elements. Each tile consists of a VLIW SIMD processor, eight banks of single-port data memory (totalling 32 KB), a direct memory access (DMA) module, and a streaming interconnect. These tiles are tightly coupled with programmable logic tiles through the AI Engine array interface and the NoC infrastructure, enabling deterministic, high-throughput communication between AI Engines and external memory or processing units. The DMA engines handle stream-to-memory and memory-to-stream data transactions efficiently, while hardware synchronization mechanisms ensure precise coordination between compute and data movement units.

Each AI Engine tile is also equipped with a configuration interconnect for access by external masters and a cascade stream feature that allows accumulator outputs to be forwarded to adjacent tiles. This structure facilitates efficient tile-to-tile communication and distributed memory access. Memory modules within each tile are accessible in four directions—north, south, east, and west—allowing AI Engines to treat adjacent memory regions as part of a contiguous address space. Cascade streams travel horizontally or vertically across tiles, enabling pipelined processing of large datasets and minimizing data movement overhead.

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The AI Engine architecture includes several functional units such as scalar and vector execution units, instruction fetch and decode logic, load/store units, and a high-speed memory interface. These components are designed to support both fixed- and floating-point operations with high precision. The interconnect modules within each tile manage AXI4-Stream and AXI4 memory-mapped I/O traffic, while the locks module supports synchronization primitives. The AI Engine array communicates with the processing system (PS) and platform management controller (PMC) via the NoC, ensuring unified access across all compute domains.

5. Design Approach and Details

5.1 Design Approach / Materials and Methods

The core objective of this project was to design a matrix multiplication application that leverages the AI Engine and programmable logic (PL) components of the Xilinx Versal ACAP platform to demonstrate heterogeneous acceleration. The approach utilizes the AI Engine for performing core scalar computations and the PL for managing data transfer operations. A standard matrix multiplication algorithm was employed, wherein each element of the result matrix is obtained by computing the dot product of corresponding rows from matrix A and columns from matrix B. Mathematically, if matrix A is of dimension j×kj×k and matrix B is of dimension k×lk×l, the resulting product C=A×BC=A×B will have dimensions j×lj×l.

The implementation was optimized by structuring the matrix size as a multiple of the number of AI Engine cores used—typically in blocks of 50 or higher—to fully exploit the parallelism provided by the VLIW processors. Data is passed to the AI Engine through AXI-Multichannel Direct Memory Access (AXI-DMA) IP blocks integrated into the programmable logic. These blocks facilitate high-bandwidth communication between global DDR memory and the AI Engine kernels using physical addressing.

To initiate data transfers, buffer descriptors are programmed within the AXI-DMA engine, enabling the AI Engine to perform direct reads and writes to DDR memory. The data movement is handled in 64-bit bursts, improving bandwidth utilization and reducing latency. The AI Engine kernel interacts with the external DDR through memory-mapped interfaces, while the programmable logic handles synchronization and transaction control. In this setup, the system benefits from both the fine-grained compute capabilities of the AI Engine and the reconfigurable connectivity of the PL fabric.

The design showcases a flexible and modular implementation strategy where the number of cores, memory channels, and interconnect paths can be tuned based on the target workload. This architecture not only demonstrates the computational efficiency of the AI Engine but also highlights the advantages of combining programmable logic with intelligent compute resources for next-generation embedded systems.

5.2 Implementation Techniques and Analysis

Implementing high-performance matrix multiplication on the Xilinx Versal ACAP requires an intricate coordination of data movement, workload partitioning, and execution synchronization. The first step involves ensuring that the required input and output data can be efficiently transferred between external DDR memory and the AI Engine array. This is accomplished through the use of AXI-Multichannel Direct Memory Access (AXI-DMA) IP blocks configured within the programmable logic (PL) fabric. These DMA modules operate using physical memory addresses and support high-bandwidth, low-latency transactions. The buffer descriptors within

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the AXI-DMA IP are programmed to initiate burst-based read and write operations between the global memory and AI Engine tiles.

Once the data transfer framework is established, the next critical aspect is slicing the data to ensure balanced parallel processing across multiple AI Engine cores. Matrix A is divided row-wise into equally sized segments, with each segment mapped to a distinct AI Engine tile. Meanwhile, matrix B is transposed and then streamed through the engine array, allowing each tile to sequentially process relevant portions of matrix B without redundant memory access. This slicing strategy not only maximizes parallelism but also minimizes interconnect congestion, a common bottleneck in shared-memory architectures.

Given that AI Engine cores produce output data in a z-order (nonlinear memory layout), a reordering mechanism is introduced in the post-processing phase to reconstruct the output matrix into its correct structure. This reordering is implemented in the processing system or the PL fabric, depending on the design's performance and resource optimization goals. Overall, this implementation showcases a data-centric programming approach where efficient memory access patterns, optimized dataflow slicing, and deterministic inter-tile communication ensure a highly scalable and performant matrix multiplication pipeline.

5.3 Codes and Standards

Bringing up the Versal ACAP board and programming the AI Engine necessitates a well-structured deployment of embedded Linux components and adherence to standard boot protocols. The booting sequence begins with the execution of BootROM code, which is hard-coded into the board's silicon. This code initializes the hardware and determines the boot mode, preparing the system to load the next bootloader stage. The U-Boot stage follows, serving as a versatile, open-source secondary bootloader that is responsible for initializing DDR memory, setting up clocks, and loading the Linux kernel into memory.

The kernel image itself contains the Linux operating system, which, once loaded, provides an execution environment for user-space applications and device drivers. The Root File System (RootFS) includes all essential libraries, binaries, system configuration files, and drivers necessary to operate the board. Furthermore, a Device Tree Blob (DTB) is used by the Linux kernel to understand the hardware configuration of the board, including available processors, memory regions, and peripheral interfaces. This tree is vital in allowing the OS to operate independently of hard-coded hardware assumptions.

From a programming perspective, AI Engine development follows a modular, graph-based specification using standard C++ syntax. The Vitis toolchain allows developers to define computational kernels as C++ functions that process data in streams or blocks. These kernels are compiled into Executable and Linkable Format (ELF) binaries and are loaded onto individual AI Engine tiles via generated aie_control.cpp files. This control application is cross-compiled and run on the target board to initiate execution. Kernel configuration can be managed either through direct driver API calls or by parsing Configuration Data Objects (CDOs) which encapsulate tile initialization parameters. This separation of compute logic and configuration control provides a clean abstraction layer that enhances portability and modularity.

The toolchain also supports runtime profiling, visualization of data movement paths, and debugging interfaces, enabling developers to fine-tune performance and resource utilization iteratively. The AI Engine driver APIs and CDO parser libraries form the backbone of the runtime control mechanism, making the platform robust for large-scale heterogeneous applications.

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5.4 Constraints, Alternatives, and Trade-offs

While the use of the Versal ACAP platform introduces considerable performance benefits, it is also accompanied by certain practical and strategic limitations that must be taken into account during system planning. One of the most significant constraints is the high cost of deployment. The silicon itself, combined with the toolchain licensing, power consumption, and the requirement for specialized development expertise, results in a higher total cost of ownership compared to traditional processor-based systems. Additionally, the learning curve associated with the AI Engine architecture, dataflow programming models, and integration with PL fabric may present challenges for development teams unfamiliar with hardware-software co-design paradigms.

Another constraint lies in the debugging and testing infrastructure, which, while powerful, is still evolving. Compared to software-centric platforms, debugging in a heterogeneous environment requires a detailed understanding of hardware state transitions, memory management across domains, and synchronization issues. Moreover, toolchain support and community adoption for AI Engine development, while growing, are still relatively limited compared to platforms like GPUs or general-purpose ARM SoCs.

Alternatives to FPGA-based solutions include Application-Specific Integrated Circuits (ASICs) and Network Processing Units (NPUs). ASICs are highly efficient and provide unmatched performance and energy savings for fixed-function tasks; however, they lack reconfigurability and adaptability, making them unsuitable for applications with evolving algorithmic requirements. NPUs offer a middle ground with relatively lower cost and moderate flexibility, especially in AI and edge inference scenarios. They come equipped with dedicated ML processing pipelines and are widely adopted in mobile and IoT devices.

Despite these alternatives, FPGAs and platforms like the Versal ACAP offer a compelling blend of flexibility, parallelism, and hardware-level performance tuning that is unmatched in dynamic and high-throughput environments. They are particularly well-suited for research, prototyping, and low-latency mission-critical applications, such as autonomous systems, radar signal processing, and embedded medical imaging. The trade-off, therefore, is a balance between upfront investment and long-term scalability. With proper planning, tool familiarity, and architectural understanding, Versal ACAPs provide a future-ready, robust platform for high-performance heterogeneous computing.

5.5 Trade-offs

While Application-Specific Integrated Circuits (ASICs) offer high-speed and energy-efficient performance for fixed-function applications, they suffer from significant drawbacks in adaptability and scalability. The rigid architecture of ASICs prevents post-manufacturing programmability, which makes them unsuitable for dynamic environments where workloads or requirements change frequently. Moreover, the high non-recurring engineering (NRE) costs, long development cycles, and low-volume inefficiencies render ASICs an impractical choice for prototyping or rapid deployment in evolving domains like packet processing and network security.

In contrast, both Field Programmable Gate Arrays (FPGAs) and Network Processing Units (NPUs) provide programmable capabilities and are well-suited for environments requiring customization and frequent updates. Between the two, FPGAs hold several technical advantages. These include early adoption of emerging silicon technologies such as high-speed transceivers and DDR4/DDR5 memory interfaces, made possible by the diverse and stable industrial demand for FPGAs in defense, broadcasting, and medical fields. This broad market base fuels continued investment, innovation, and competitive pricing.

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From a performance perspective, FPGAs offer lower power consumption and more deterministic latency compared to NPUs, which is critical in use cases involving real-time packet inspection, application offloading, and adaptive data flow control. However, achieving these advantages requires a deep understanding of hardware design principles, AI Engine programming models, and dataflow graph structuring. Programmers must also become proficient with the use of system-level APIs and understand the interaction between AI Engine, programmable logic, and the processing system. The integration of multiple accelerators within a single SoC mandates a holistic understanding of the device's architecture and behavior. Therefore, while the solution is technically superior, its adoption necessitates experience with hardware-software co-design and accelerator-based development workflows.

6. Tasks and Milestones

The project was executed in multiple phases, each contributing to the successful implementation of heterogeneous matrix multiplication using the Xilinx Versal ACAP platform. The initial phase involved acquisition and setup of the target hardware, the VCK190 evaluation board, which features a combination of ARM processors, programmable logic, and the AI Engine array. Subsequent tasks included the preparation of embedded Linux images comprising the bootloader, kernel, root filesystem, and device tree blob. In parallel, the AI Engine application was developed and compiled into a set of ELF binaries and control files.

Once the software stack and application components were ready, the deployment phase involved transferring the files to the board using the TFTP protocol. Upon booting, the board brought up the Linux OS, after which the AI Engine control application was executed via the terminal. The system logs confirmed successful initialization, DMA configuration, and execution of matrix multiplication across the AI Engine array. A post-execution verification step compared the AI Engine results against a baseline CPU output to ensure correctness. Each phase was completed according to a planned milestone timeline, ensuring progress tracking and validation at every stage.

7. System Implementation and Experimental Validation

The proposed system was implemented and experimentally validated using the Xilinx Versal ACAP-based VCK190 development board. After preparing the embedded Linux environment and compiling the AI Engine application, the complete runtime stack was deployed onto the target board via the TFTP protocol. Serial console access was used to interact with the board, initiate the application, and monitor execution logs. All required components, including ELF binaries, control logic, and configuration files, were systematically organized and transferred to ensure a streamlined deployment process.

Upon successful system boot-up, the AI Engine-based matrix multiplication workload was executed. Data was read from and written to external DDR memory using AXI-DMA channels, while the programmable logic fabric facilitated synchronization and efficient data flow. During execution, DDR memory addresses associated with intermediate and final results were logged for inspection and traceability. The AI Engine array performed the matrix computation in parallel, significantly accelerating the overall processing time.

Performance metrics including computation time, memory access patterns, and throughput were recorded post-execution. A comparative validation was conducted against a baseline implementation running solely on the ARM Cortex-A72 processor to confirm result accuracy and demonstrate performance gains. The output generated by the AI Engine matched the reference results produced on the CPU, thereby confirming the correctness and

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numerical stability of the proposed heterogeneous architecture. This empirical validation reinforced the system's efficiency, scalability, and suitability for high-throughput embedded AI workloads.

Numerical Validation and Accuracy Assurance

To ensure the correctness and numerical stability of the AI Engine–based matrix multiplication implementation, a post-execution verification phase was conducted. The output generated by the AI Engine was compared against the results obtained from a CPU-only implementation on the ARM Cortex-A72 core. Root Mean Square (RMS) error was computed between the two result matrices to quantify numerical deviation. Across all test cases, the RMS error remained below 10^{-6}, confirming high numerical consistency and correctness.

Additionally, fixed-point arithmetic was primarily used within the AI Engine cores to optimize computational efficiency, while the CPU baseline operated in floating-point mode. Precision management and quantization strategies were carefully designed to avoid overflow and underflow, particularly during accumulation stages. These results demonstrate the numerical robustness of the heterogeneous architecture and validate its reliability for real-world applications involving matrix-intensive computations.

8. Discussion

The experimental results of this study revealed a substantial performance gain of approximately 25× when leveraging the AI Engine and programmable logic on the Xilinx Versal ACAP platform, compared to a baseline ARM Cortex-A72 CPU implementation. This speedup underscores the potential of heterogeneous computing architectures in addressing the growing computational demands of embedded AI applications, particularly where real-time performance, power efficiency, and deterministic latency are critical. The ability to execute large matrix multiplication tasks in significantly less time directly translates to faster inference, better user experience, and the possibility of supporting more complex workloads on edge devices.

One of the most significant implications of this result lies in the **performance-per-watt improvement** achieved through the AI Engine's architectural advantages. By combining data-parallel VLIW processors with low-latency, tile-to-tile communication, and efficient memory access, the system achieved higher throughput while consuming less power compared to general-purpose processing cores. This finding is particularly valuable in the context of embedded AI systems, where energy-delay product (EDP) is often a more critical metric than raw performance alone.

However, several trade-offs were observed. Although the AI Engine demonstrated exceptional performance in a controlled matrix multiplication scenario, its **applicability to other, more irregular workloads** remains a challenge. Workloads with sparse data access patterns or unpredictable control flows may not map efficiently onto the deterministic tile-based architecture of the AI Engine. Moreover, the learning curve and tooling complexity associated with hardware-software co-design and graph-based kernel programming are non-trivial, potentially limiting the platform's accessibility for non-specialist developers.

To place our results in context, we compared our heterogeneous system's performance with GPU-based solutions reported in related literature. While our AI Engine implementation achieved a 25× speedup over CPU-only execution, state-of-the-art GPU platforms such as NVIDIA's Jetson AGX Xavier or RTX 3090 report approximately 15× speedups for similar 800×800 matrix multiplication workloads, depending on precision and memory configurations. A comparative summary is shown below:

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Platform	Matrix Size	Execution Time	Power	Speedup
ARM Cortex-A72	800×800	X sec	Y W	1×
Versal AI Engine	800×800	X/25 sec	Y/3 W	25×
GPU (Literature)*	800×800	Z sec	Z W	~15×

* GPU metrics are estimated based on data from [1], [5]

This comparative analysis shows that while GPUs remain highly competitive and more mature in terms of ecosystem and developer tools, the AI Engine-based approach offers superior performance in terms of energy efficiency and latency for well-structured, compute-intensive operations. It is especially well-suited for real-time embedded systems where deterministic execution, low power consumption, and hardware reconfigurability are prioritized over general-purpose flexibility.

In conclusion, while the AI Engine excels in controlled, parallelizable scenarios, a hybrid approach that combines both GPU- and FPGA-class acceleration strategies may represent the most balanced path forward for future heterogeneous computing systems.

9. Conclusion and Future Work

This research successfully implemented and evaluated an 800×800 matrix multiplication workload using both a standalone ARM Cortex A72 processor and a heterogeneous architecture combining the AI Engine, programmable logic (PL), and CPU on the Xilinx Versal ACAP platform. A thorough performance comparison between the two configurations was conducted, focusing on execution time, initialization latency, data transfer rates, buffer descriptor chaining, and PL I/O throughput. The results clearly demonstrated the effectiveness of the heterogeneous design, achieving a nearly 25× speedup in total computation time compared to the CPU-only baseline.

These findings highlight the advantages of integrating domain specific accelerators and reconfigurable logic for parallel data processing tasks, particularly in embedded systems where power efficiency and deterministic performance are crucial. The demonstrated architecture leverages the strengths of each component general purpose processing from the CPU, flexible data orchestration from the PL, and high throughput parallel computation from the AI Engine to achieve significant gains in execution time and resource utilization.

For future work, the performance of the matrix multiplication application can be benchmarked against GPU based acceleration to further assess the tradeoffs between different heterogeneous computing paradigms. Additionally, optimizing the AI Engine utilization, such as through dynamic core allocation, advanced memory tiling, and pipeline aware kernel scheduling, offers promising avenues for reducing latency and increasing throughput. These improvements will further support the adoption of heterogeneous SoCs in next generation edge AI, signal processing, and real time computing applications.

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Environmental and Ethical Considerations

The demonstrated performance improvements achieved through the AI Engine also contribute to broader sustainability goals. By significantly reducing execution time and power consumption, the heterogeneous SoC architecture offers substantial energy savings, aligning with green computing principles. This is particularly relevant for edge computing deployments in healthcare, autonomous systems, and safety-critical environments where both low latency and power efficiency are vital.

Furthermore, the use of reconfigurable logic and application-specific accelerators reduces the need for generalized over-provisioning, enabling more sustainable hardware utilization. Future extensions of this work will explore the balance between performance optimization and ethical deployment of AI-enabled systems, ensuring fairness, transparency, and energy-aware design in embedded AI applications.

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Appendix: Reproducibility and Deployment Details

A. AI Engine Kernel Code Snippet

The following is a simplified C++ kernel function used for tile-level matrix multiplication on the AI Engine. It operates on a stream of input vectors and produces partial dot-product outputs:

cpp

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```
void mm_kernel(input_window<int32> *a, input_window<int32> *b, output_window<int32> *c) {
   for (int i = 0; i < MATRIX_SIZE; i++) {
      int32 a_val = window_read(a);
      int32 b_val = window_read(b);
      int32 result = a_val * b_val;
      window_write(c, result);
   }
}
```

This kernel is compiled using the Xilinx Vitis AI Engine compiler and mapped to individual AI Engine tiles as part of a dataflow graph. It forms the core compute unit in the parallel matrix multiplication workload.