

A LOW POWER BASED 8×8SRAM ARRAY USING MULTI THRESHOLD -CMOS TECHNIQUE AND VARIABLE THRESHOLD -CMOS TECHNIQUE

¹ RADHIKA. R, RESEARCH SCHOLAR IN DEPARTMENT OF ECE IN JNTUH, HYDERABAD, TELANGANA. rykradhika@gmail.com.

² B.K. MADHAVI, PROFESSOR IN DEPARTMENT OF ECE IN SIDDHARTHA INSTITUTE OF TECHNOLOGY, HYDERABAD, TELANGANA. bkmadhavi2009@gmail.com.

ABSTRACT: All modern high speed VLSI circuits need some kind of data storage. Static random access memory (SRAM) is a commonly utilised memory in consumer electronics that serves to store and retrieve huge amounts of data quickly. Therefore, a very power-efficient design is required. Low power approaches are necessary to obtain low power SRAM cells. The first step in designing an 8×8 SRAM array is to create an 8T SRAM cell and test its read and write operations. The circuits needed for this design include a 3 to 8 Decoder, a precharge circuit, a write driver, and a sense amplifier. After this, begin integrating low power strategies into the SRAM cell. In this case, the design of the SRAM cell makes advantage of two low power strategies. Low power approaches include MTCMOS and VTCMOS, which stand for variable threshold CMOS. The best low power strategy to decrease the 8T SRAM cell's dynamic power consumption is shown by the simulation results and graphical graphs. Use TANNER Eda V16.0 for the design of an 8x8 SRAM array with minimal power consumption.

KEYWORDS: Low power, Static random-access memory, SRAM Array, Multi Threshold CMOS Technique (MTCMOS), Variable Threshold CMOS Technique (VTCMOS).

INTRODUCTION

With advancing technology, there is always an increase in demand for larger data storage capacity. This has driven the fabrication technology and memory development towards more compact design rules and towards higher data storage densities. A variety of memories are available to store and access the information stored. According to ones need one may select a read only memory which is generally used in microcontrollers or a read write memory that is generally used in microprocessors. In comparison to DRAM though SRAM requires more space, it is easily fabricated and is much faster. Dynamic RAM unlike the Static RAM needs to be refreshed after equal intervals of time. Hence for SRAMs the standby power is very low despite of high density

of transistors. SRAM cells have high noise immune due to larger noise margins, and have ability. The most important application of SRAM is in CPU cache memories, small on chip memories, FIFOs or other buffers. Here, design of 8x8 SRAM array chip and analyses the area and delay of the entire chip.

LITERATURE REVIEW

The no of transistors used in the circuit is main concern for power optimizations. Even though four transistors is enough to design the SRAM circuit, it needs the resistive loads additionally which reduces the reliability of the circuit. The writing stability of the load less 4T SRAM cell is not good [1]. To improve the writing stability the 5T SRAM cell is designed [2]. This circuit possesses the large amount of leakage power due its feedback connection. To avoid the instability of the write operation, look ahead bias that controls the threshold voltage dynamically. This circuit uses the 7 transistors [3]. In order to reduce the leakage current, the self-controllable voltage circuit is employed. But, its data retention and transistor sizing is complicated [4]. The MTCMOS technique is more efficient than the self-controllable voltage circuit. MTCMOS is the Multi Threshold CMOS technique is used in 12T SRAM circuit [5]. In this paper, the circuit complexity is high. To optimize the power the memristor is used. Being an analog element the memristor possesses an accountable leakage power. The overall area of the circuit is increased due to the presence of memristor [6].

Design of 8T SRAM Cell

The SRAM cell that we considered in this paper is “8T SRAM Cell” which consists of two crossly coupled inverters and access transistors to read and write the data and additional two symmetrical NMOS transistors (N5 and N6) placed opposite to the access transistor. Instead of 6T SRAM Cell the 8T SRAM Cell is used. Because this cell has low leakage power compared to the conventional 6T SRAM Cell. But the addition of those two NMOS transistors (N5 and N6) the power consumption of this cell increased. The supply voltage of this cell is 800.0mv. For write operation drive the input value and its compliment to the bitline (BL) and bitline_bar (BLB) then raise the word line (WL). Pre charging of bit line (BL) and bitline_bar (BLB) is set to high and let them float. The QA and QB are the outputs of these two cross coupled By observing the transient response of 8T SRAM cell it indicates working nature of the cross coupled inverters the word line

is maintained at 1V constantly, QA is compliment to bitline (BL) and QB is compliment to bitline_bar (BLB) as shown in the Fig.

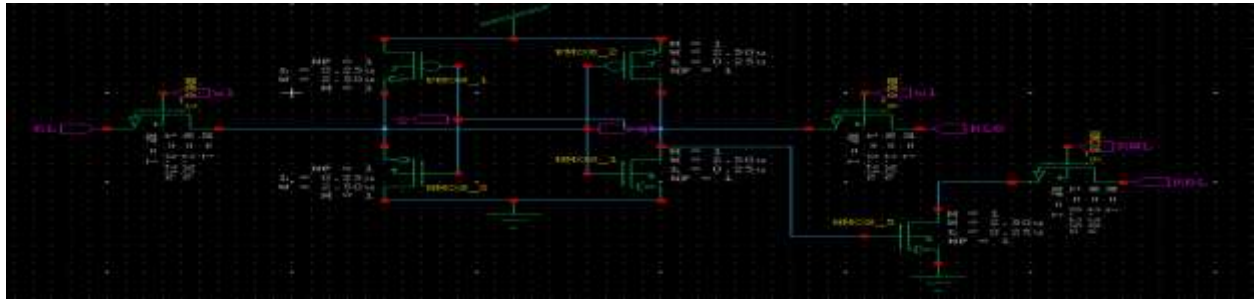


Fig: Schematic of 8T SRAM Cell

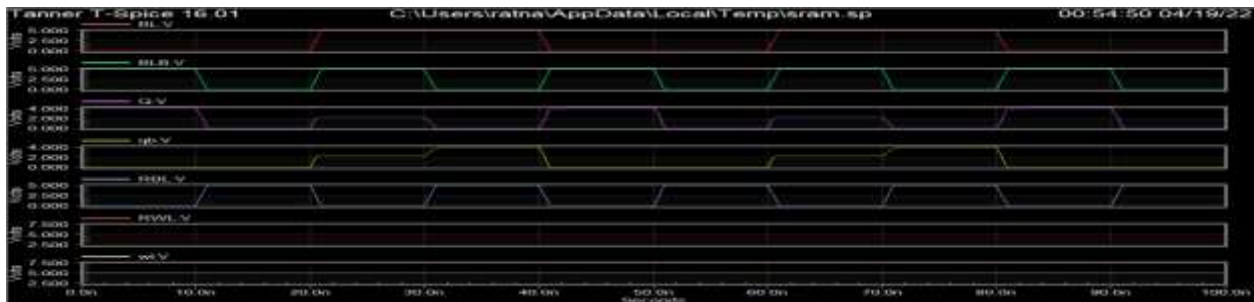


Fig: Transient response of 8T SRAM Cell

BLOCK DIAGRAM OF GENERIC SRAM ARRAY

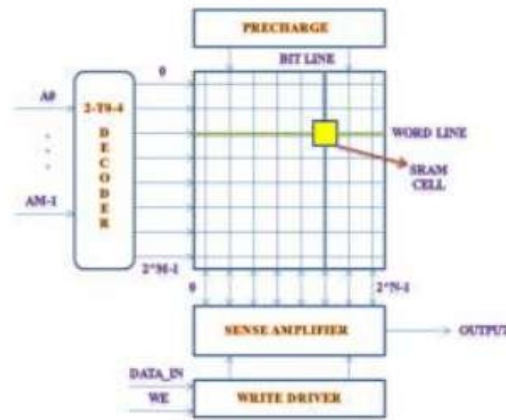


Fig: block diagram generic SRAM Array

To Design SRAM Array, Firstly design sub circuits of SRAM Array are essential circuits and plays crucial role in designing of SRAM Array. They are 3 to 8 Decoder, Pre-charge circuit, Write Driver, Sense amplifier, SRAM cell.

DESIGN OF 3 TO 8 DECODER

The decoder is a logic circuit that accepts the set of inputs that represent a binary number and activates that output which corresponding to the input binary number. A decoder has „n“ inputs and 2^n output lines. The 3-to-8 decoder operates according to the Truth table as shown in Table 1.

- The 3-bit input is A_0, A_1, A_2 and the Eight outputs are $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$.
- If the input is the binary number i , and then output D_i is uniquely true.
- For example, if the input $A_0, A_1, A_2=01$, then output D_0 is true, and $D_1, D_2, D_3, D_4, D_5, D_6, D_7$ are all false.
- This circuit “decodes” a binary number into a “one-of-eight” code.

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table 1. Truth Table of 3 to 8 Decoder

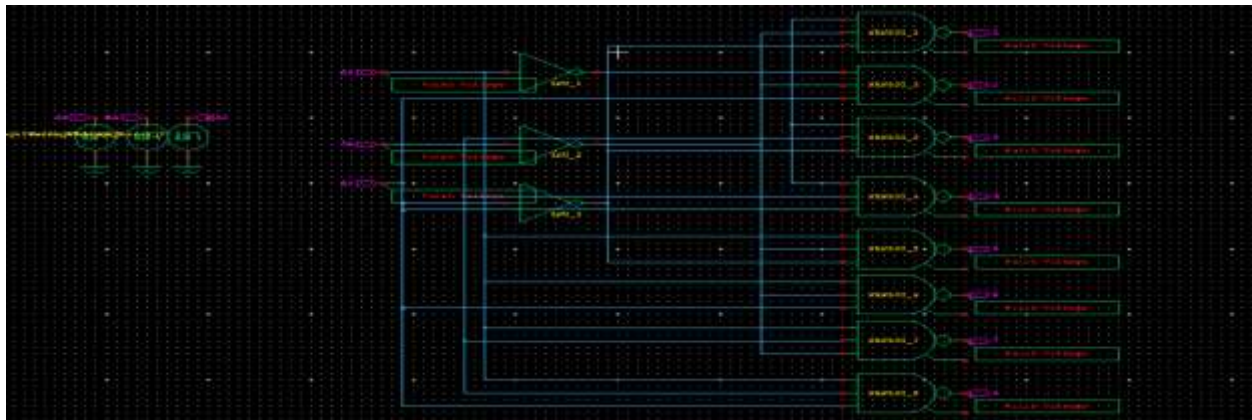


Fig : Schematic of 3 to 8 Decoder

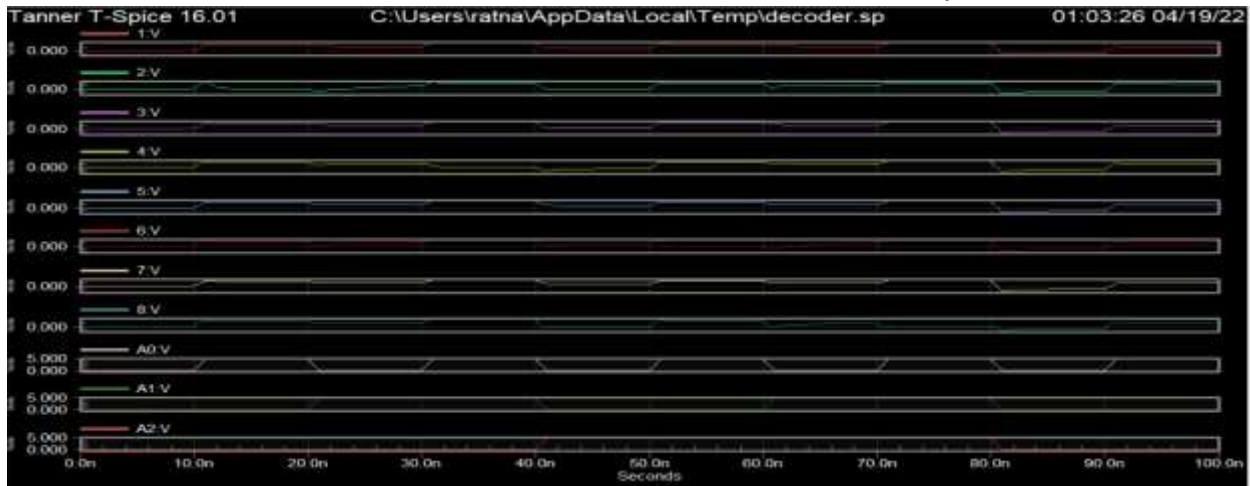


Fig: Transient response of 3 to8 Decoder

DESIGN PRE-CHARGE CIRCUIT

The pre-charge circuit is one of the vital component that is persistently employed within SRAM cell. The work of the pre charge is to charge the bit and bitline-bar to the power supply $V_{dd}=1.8v$. The pre charge circuits authorize the bit lines to be charged high at all times aside from throughout read and write operation.

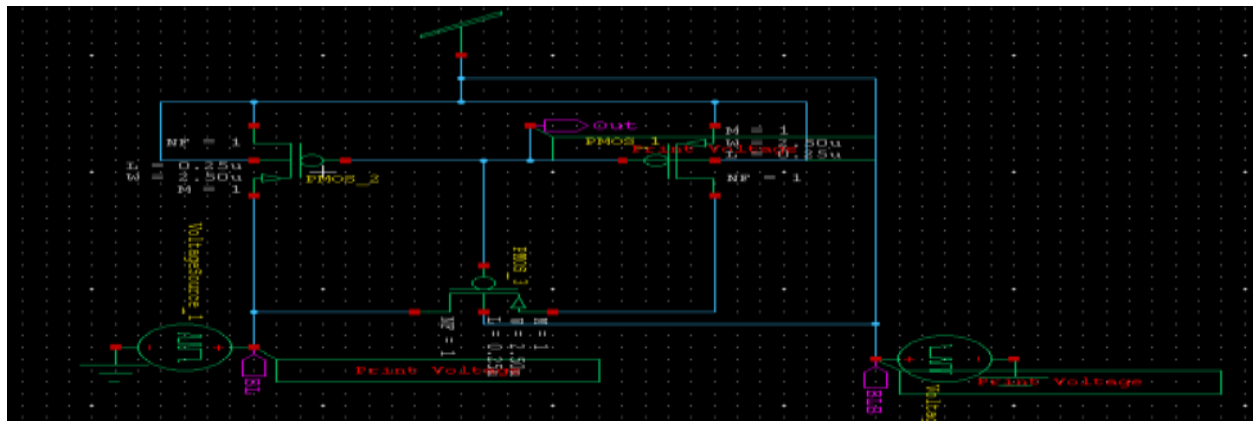


Fig: Schematic of Pre-charge circuit

Pre-charge of the power line voltages in a high voltage DC application is a preliminary mode which limits the inrush current during the power up procedure. The pre-charge that holds bit lines at positive voltage makes it possible to amplify that differential signals to a useful logic level.

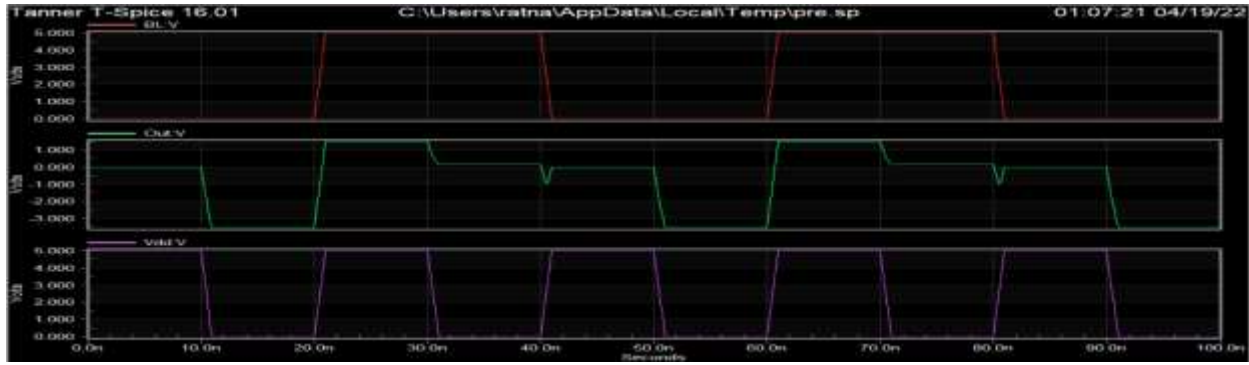


Fig : Transient response of Precharge circuit

DESIGN OF WRITE DRIVER CIRCUIT

The write driver circuit is one of the vital component in the SRAM array design. The job of the write driver is to keep the bit line and bitline-bar to ground potential for the further next level of its work. Before this the bit line and bitline-bar are being charged maximum supply voltage of Vdd. By the usage pre-charge circuit it will get charged and after that it gets discharged. The two logics are given to the two points of the junction of the NMOS. i.e0 and 1.The bit line which is nearer to the 0 logic it gets discharged first after that its logic gets inverted. In this way the bit line and bitline-bar gets discharged to the ground. With this kind of operation the bit line and bit line bar gets discharged. So that the voltage difference between bit line and ground, bit line bar and ground is zero. So that another data can be easily retrieved by the memory cell.

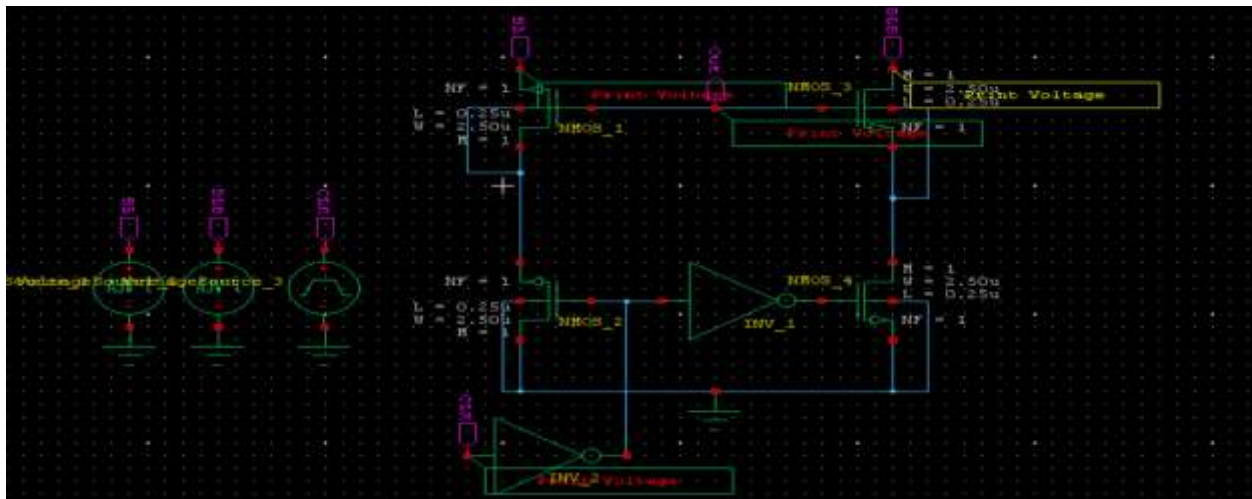


Fig: Schematic of Write driver

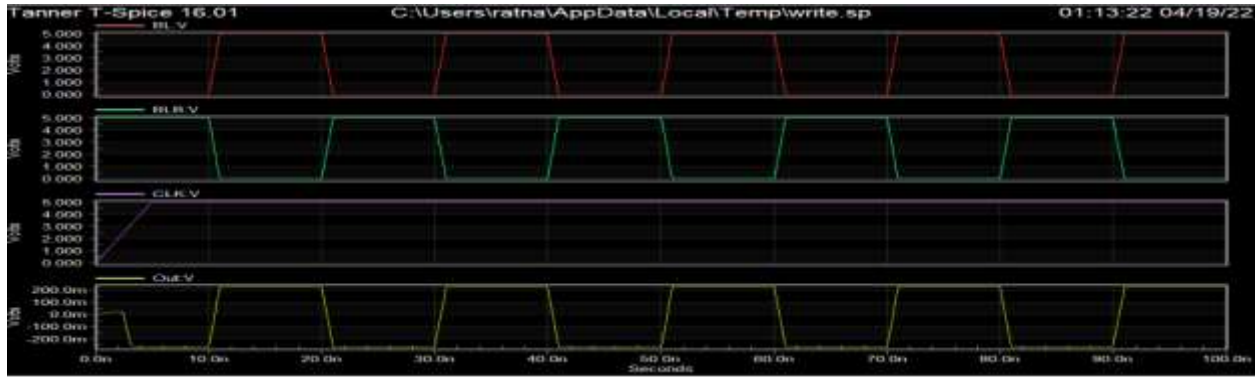


Fig: Transient response of Write Driver

DESIGN OF SENSE AMPLIFIER

The Sense amplifiers are the essential component in the SRAM memory design. The job of sense amplifier is to sense the bit line and bitline-bar for proper observing action. It improves the read and write speed of the SRAM memory cell. Another job is to achieve the low power consumption operation in memory design. The sense amplifiers primary utilized to amplification of the voltage difference is being produced on the bit line and bit line bar at the time of operation. As we know that in SRAM operation we didn't do refresh of the memory for the further process, as the each segment has one sense amplifier for the single output. So, it can get proper use of the sense amplifier in the designing circuit. These is the various parameters of a sense amplifier are

$$\text{Gain } A = V_{out}/V_{in}$$

Sensitivity S is $V_{in \text{ min-}} - \text{least noticeable signal}$. Rise time t_{rise} , fall time t_{fall} -10% to 90%.

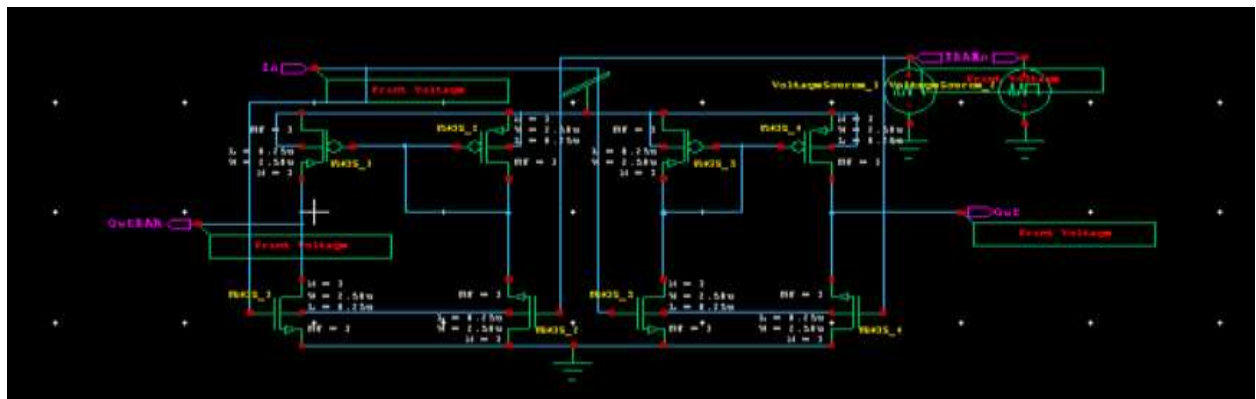


Fig: Schematic of Sense Amplifier

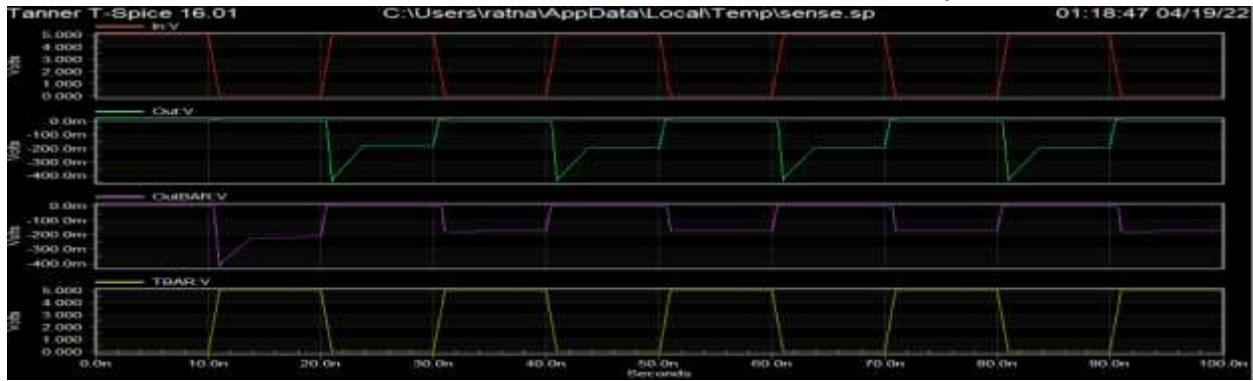


Fig: Transient response of sense amplifier

DESIGN OF 8×8 SRAM ARRAY

The Transient response for the write 0 and write 1 operation is shown in Fig. 20. In the read operation, also here the WL7 and WL0 are activated in order to perform the required operations. The WL7 when it is high at a point the WL0 is low, resulting in write 1 operation at QA0 and write 0 operation at QB0. Therefore, the write 0 and write 1 operations are verified.

The transient response as shown in the above results, in read operation when both the inputs get low at that time data is being kept at the constant value. When WL7 goes from high to low and WL0 goes from low to high with sense enable gets on it get confirmed for the read Operation of the memory cell.

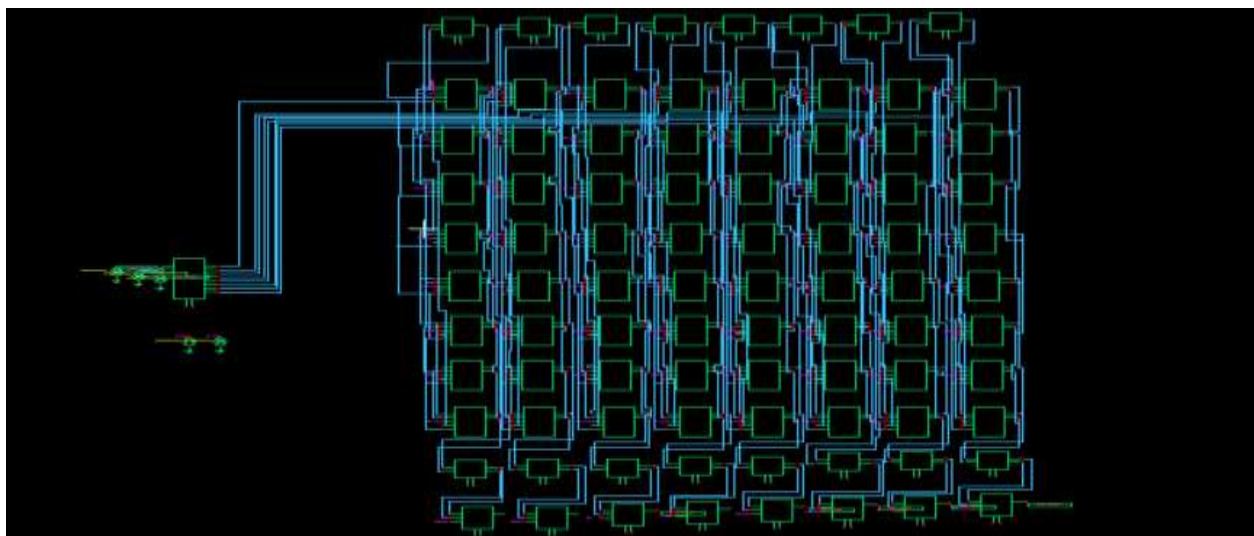


Fig: Schematic of 8×8 SRAM Array

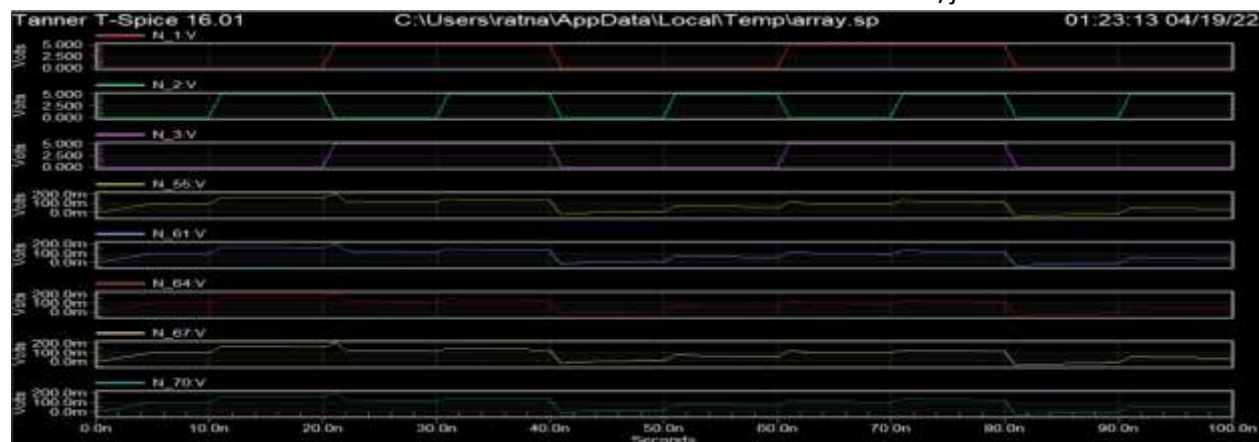


Fig: Transient response of 8*8 sram cell

CONCLUSION

A Low power 8X8 SRAM array is designed for storing 64 bits. Peripheral components such as 3 to 8 decoder, Pre charge circuit, write driver circuit, sense amplifier including and has been designed and assembled to form SRAM array. Differential type sense amplifier is used for noise reduction. Pulse input signal with a peak to peak voltage of 800.0mV (rail rail) and Supply voltage of 800.0mV for SRAM cells and for 8×8 SRAM array the supply voltage is 1.8V is considered. Transient responses for read and write operations for both logic-1 and logic-0 have been analyzed. Investigated the low power techniques among two techniques better results got in MTCMOS Technique. In this Technique reducing the power consumption to 57% as compared to conventional 8T symmetrical SRAM cell. SRAM array and SRAM cells and peripheral components are designed in Tanner eda.

REFERENCES

- [1] Robert Giterman, MaozVicentowski, Itamar Levi, YoavWeizman, OsnatKeren and Alexander Fish., “Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell,” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS”, no.5, May. 2018.
- [2] R. Bisht, P. Aggarwal, P. Karki and P. Pande. 2016. Low power and noise resistant 16×16 SRAM array design using CMOS logic and differential sense amplifier. 2016 International Conference on Computing, Communication and Automation (ICCCA), Noida. pp. 1474-1478.
- [3] Benton H. Calhaun, Anantha P. Chandrakasan “Static Noise MarginVariation for Sub-threshold SRAM in 65 nm CMOS”, IEEE Journalof SolidState Circuits,, pp.1673-1679. vol.41,July 2006.
- [4] Chotaro Masuda, Tetsuya Hirose, Kei Matsumoto, Yuji Osaki, Nobutaka Kuroki, and Masahiro Numa, “High Current Efficiency Sense Amplifier Using Body-Bias Control for Ultra-Low-Voltage SRAM”, in Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium,2011.
- [5] S. Tavva et al. “Variation Tolerant 9T SRAM Cell Design”GLSVLSI“10,pp.55- 60,may 16, 2010.
- [6] Arandilla,C.D.C et al.“Static Noise Margin of 6T SRAM Cell in 90-nm CMOS” IEEE 13th International Conference on computer modeling and Simulation, pp.534- 539,March 30,2011.
- [7] K. S. Yeo, W. L. Goh, Z. H. Kong, Q. X. Zhang, andW. G Yeo, “Highperformance low-power currentsense amplifier using a cross-coupled currentmirrorconfiguration,” IEE Proc. G Circuits, Devices, andSystems, Vol. 149, No. 56, pp. 308-314, Oct. 2002.
- [8] Singh S K, Singh S V, Kausik B K, Chauhan C and Tripathi T 2014 Characteriztion& improvement of SNM in deep submicron SRAM design International Conference on Signal Processing and Integrated Networkspp 538-542.
- [9] Christiensen D.C. Arandilla, Anastacia B. Alvarez and Christian Raymund K. Roque 2011 Static noise margin of 6T SRAM cell in 90-nm CMOS International Conference on Modelling and Simulationpp 534-539.

10.48047/jocaaa.2024.33.08.237

[10] VanamaKundan, GunnuthulaRithwik and Prasad Govind 2014 Design of low power stable SRAM cell International Conference on Circuit, Power and Computing Technologies pp 1263-1267.