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Image Acquisition and Processing System based on ZYNQ

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Abstract

With the advancement of manufacturing processes, imaging sensors have become more and more sophisticated, the amount of image data generated is increasing, and application scenarios and functional algorithms have become more and more complex. The traditional serial processing method can no longer meet the real-time requirements of image processing. The use of hardware to accelerate image algorithms has become a basic trend in image acquisition and processing systems. Xilinx's Zynq7000 series chip integrates a dual-core A9 series ARM processor (PS) and an A7 series FPGA (PL). The industry standard AXI interface (advanced extensible interface) is used for information between ARM and FPGA. Interactive. This paper designs an image acquisition and processing system based on Zynq, which collects images through OV5640, uses Zynq as the main control chip to analyze and process the image data, and uses RGB LCD for image display. This article develops the OV5640 video capture IP, LCD driver IP, and image edge detection IP, and calls these key IPs in the ZYNQ system to establish an image capture and processing system that integrates image data collection, transmission, storage, image display, and edge extraction. The overall effect of the system is good, and it can effectively detect the edge information of the target. At the same time, the image collection and display can reach the design target of 60 frames per second, which has strong applicability.

Keywords

ZYNQ; Hardware Acceleration; SCCB; Image Acquisition; Edge Detection Processing Algorithm.

1. Introduction

People mainly rely on the sense of touch, hearing, vision and taste the world to get information and knowledge, and more than 80% visual information , but only rely on the eyes to collect image information is completely not enough, because the human eye can't in the high strength work, at the same time many times require observation environment is very bad, It is also possible that the observed object is invisible to human eyes, so people use machines to assist human eyes to collect and process images, which is why machine vision was born. In recent years, with continuous breakthroughs in the performance of processing chips, machine vision has been widely applied in various life fields, such as intelligent driving, medical treatment and so on .

Traditional image acquisition and processing technology is based on computer platform software[1], but because of computer instructions are carried out according to the order of the serial, in the image processing efficiency is very low, the processing of high-resolution image will consume a large amount of time seeks new just now far cannot satisfy the real-time requirement of production and living. Later, some multi-core embedded processors are also used in the application of image acquisition and processing. Because the system has multiple cores, the system can carry out multiple image processing tasks at the same time, which improves the real-time processing efficiency compared with the computer system. However, the command processing method of the embedded processor is still serial execution, which is

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difficult to meet the computing requirements of daily life for a large amount of image data in high-resolution images.

Xilinx designs a fully programmable All Processor SOC (APSOC) zynQ-7000, which integrates a central Processor CPU(PS side) core and FPGA (PL side) to solve the above problems.

Aiming at the main problems of image acquisition system based on computer and serial execution embedded processor, this paper designs an image acquisition and processing system based on ZYNQ[2], which can design appropriate acquisition and display driver modules according to the specific image input source and display format. At the same time, the platform can realize the acceleration of various image processing algorithms, and further expand the application field of the platform. Compared with the traditional image acquisition system, the parallel processing characteristic of FPGA can realize the driving timing more conveniently, and also can accelerate the image processing. At the same time, THE ARM+FPGA architecture greatly improves the resource utilization rate of hardware, and improves the flexibility and versatility of the system. The hardware and software cooperation technology and IP reuse design ideas used in this design have a certain enlightenment significance to the design and development of image processing, instrument control and other fields.

2. Video Capture Technology based on ZYNQ

2.1. Software and Hardware Co-design Technology

The traditional embedded system design is developed and designed from top to bottom. The software and hardware design are independent of each other. Once the system has problems, the layout and wiring need to be rearranged on the printed version, which is not only low efficiency but also high cost.

Hardware and software collaborative design is characterized by developers to use the tools of unification of the hardware and software of system design, design of hardware circuit at the same time can be to design of software, and hardware and software specification, unified communication mechanism between the two, when both are completed through design platform for simulation functions.

The Vivado design Suite combines the concept of hardware and software co-design, which provides a highly unified design environment based on industry standards and supports the combination of programmable technologies. The suite includes not only Vivado IDE, a hardware design synthesis and timing constraint tool, but also Xilinx SDK, an embedded software development tool. Design tools based on IDE and SDK .

(1) Firstly, according to the requirements of actual production and life, the functional analysis is carried out, and parameters and indicators of relevant technologies are formulated to provide standards for subsequent design.

(2) Overall design of the system according to the actual function division and technical indicators. The hardware and software are divided according to the hardware processing characteristics of PL and PS terminals. Generally, the parallel tasks inclined to massive data calculation and timing control are designed on the PL side, and the control tasks and sequentially executed tasks are implemented on the PS side.

(3) Design the hardware circuit of the system through hardware description language according to the actual demand. Through the Vivado IDE development tool, you can design a custom IP according to the requirements of the project, and the tool includes integration, layout and wiring, function simulation, and other functions, which is very user-friendly.

(4) Software development according to hardware circuit. The hardware configuration file is imported into Xilinx SDK to design the system software by using C language or C++ language.

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(5) After step (3) and Step (4) have been designed, software debugging can be carried out through The Debug in Vivado SDK and logic analyzer in Vivado IDE for timing and data analysis. If the software and hardware tests meet the design requirements, then the software and hardware can be integrated and the system can be tested. On the contrary, if the design requirements are not met, the design needs to be redesigned according to the previous steps after analysis.

2.2. IP Reuse Technology

IP core is essentially a circuit module customized according to specific functions, generally divided into IP soft core and IP hard core. IP soft cores can be changed by users while IP hard cores cannot be redeveloped.

The hardware circuit of Zynq7000 series is integrated into one IP, all hardware resources can be added and extracted by configuring IP core (can be set as AXI interface), so the IP designed according to the function is connected to Zynq IP, and the same IP can be connected to different modules to achieve different hardware functions. Figure 1 shows the IP-centric design approach of Vivado IDE[3].

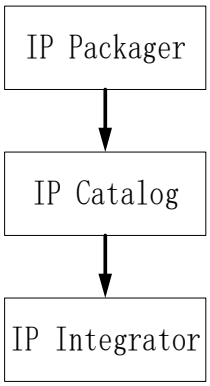

Figure 1. Vivado's IPcentric design approach

(1)IP Catalog. This is a proven IP library that includes Xilinx official or third-party IP libraries, as well as its own designed IP.

(2)IP Packager is an IP encapsulation tool that encapsulates hardware documents designed by developers, such as source files (RTL, etc.), test sets, simulation models, etc., into an IP. Also, IP Packager allows IP interfaces to be set directly to the AXI bus standard, which makes packaged IP more compatible.

(3)IP Integrator is a component of a graphical interface of all kinds of IP, from the IP Catalog call required IP resources for the component of its own system, through the IP Integrator run Connection Automation can achieve automatic connection to the AXI interface. You can also use valid Design to check whether there is a problem with the connection between IP addresses.

2.3. AXI Bus

AXI protocol is a part of AMBA, a microcontroller bus specification launched by ARM company. Zynq700 series uses AXI4 bus protocol, which enables efficient data interaction between PL and PS parts. The protocol and communication mechanism of AXI4 are described below.

The AXI4 feature is that the data channel and control instructions between the master and slave are implemented through two channels. As long as the host sends the first address of the received data to the slave machine, the slave machine can send batch data to the host.

For each channel, the master sends out a request signal before communicating with the slave machine, and returns a reply signal after receiving the signal from the slave machine. This

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process is called "handshake". Figure 2 shows the handshake process of each signal interaction channel of master-slave machine.

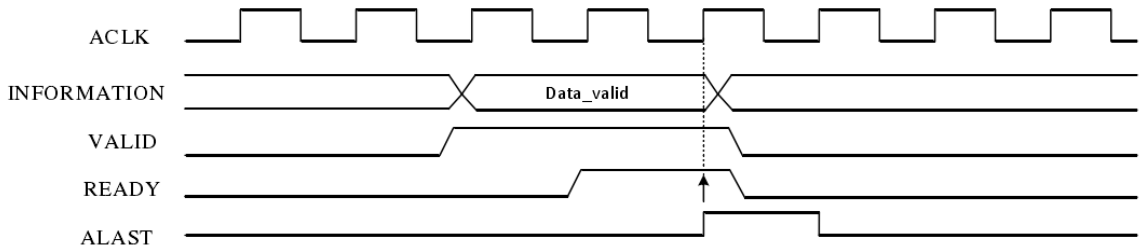

Figure 2. The handshake process for AXI4 channel signals

When the host VLAID signal is high, it indicates that the host signal or data to be transmitted is ready. When the READY signal of the slave machine is at high power, it indicates that the slave machine can receive signals or data from the host. When both signals are at high levels, the master slave machine starts to interact[4]. Both read and write channels produce a LAST signal when the transmission ends.

3. Overall System Design

The acquisition end of the image acquisition system collects image data in real time by OV5640 camera, and then processes the image through edge detection algorithm, and then displays it through a 7-inch LCD screen. The functions and design ideas of the system are as follows:

1) Collect images. Optical imaging sensor OV5640 is used to collect images, and an image data acquisition IP is designed at the PL end to convert OV5640 output data into video stream format. SCCB bus protocol is implemented in PL terminal to configure the internal register of OV5640 and control its working state.

2) Perform edge detection algorithm on image data. The mathematical model of edge detection algorithm is converted into hardware circuit by hardware description language and encapsulated into IP for system construction.

3) Cache and display image data. Considering the difference between OV5640's working clock and LCD's pixel clock, as well as the size of image data, VDMA IP calls DDR's storage resources outside the PS end for frame caching of image data. The PS terminal and PL terminal use AXI bus mechanism to exchange information. Thus controlling DDR to read and write image data[5].

4. Test Analysis

Figure 3, Figure 4, Figure 5 and Figure 6 are obtained by simulating the LCD display driver.

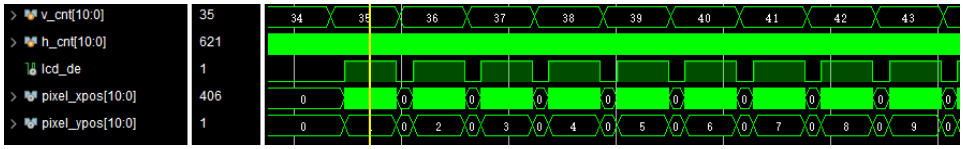

Figure 3. Simulation diagram of a frame image

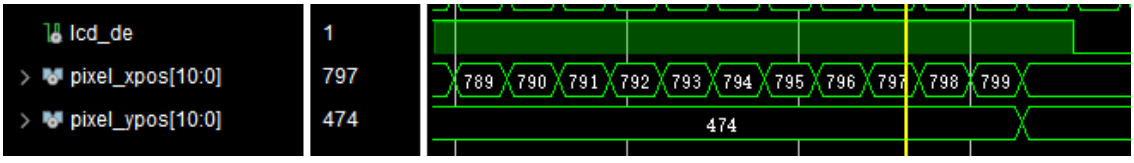

Figure 4. Simulation diagram of a frame image

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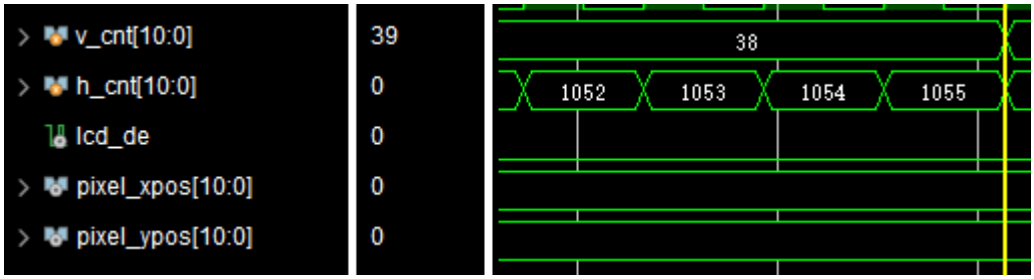

Figure 5. Simulation diagram of a frame image

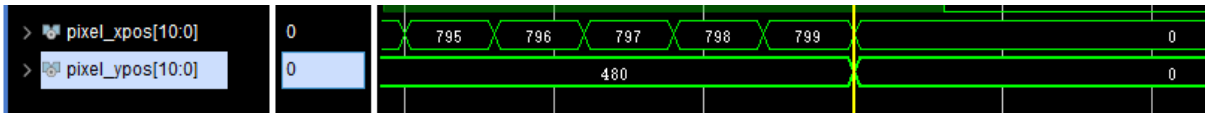

Figure 6. Simulation diagram of a frame image

V_cnt, H_CNT, LCD_DE, pixel_xpos and pixel_Ypos are column count, row count, pixel data enabled, pixel display abscise (effective area) and pixel display ordinate (effective area) respectively. It can be seen from FIG. 3 and FIG. 4 that the effective enable of pixel data is displayed from the point (0, y) of the effective area, that is, the position at the beginning of each line. The effective enable of pixel data is not lowered until the end of each line. Figure 5 shows that the width of h_CNT is always wider than that of pixel_ypos due to the fact that the screen is divided into valid and invalid areas. As you can see from Figure 6, pixel_ypos stops counting when it reaches 480, indicating the end of a frame display.

5. Conclusion

This paper designs a high-speed image acquisition and processing system based on Zynq processor. The main contents of this paper include:

(1) For Zynq image acquisition, relevant technologies such as software and hardware cooperation technology AXI bus protocol have been prepared, and the basic architecture of video acquisition system including VDMA, data protocol conversion IP and timing logic controller has been established in Zynq system.

(2) Designed and developed the video acquisition software and hardware system, designed and developed the OV5610 video data read and write protocol, and correctly obtained the image data output by OV5640. Developed LCD driver IP, including timing control logic, data transmission, display control and so on.

(3) The Sobel edge detection image algorithm was designed and developed, and the design method of area for speed was adopted in FPGA to achieve the purpose of hardware acceleration and video edge detection.

(4) System simulation test. Since the PL-side part of the system involves many modules, it is difficult to start the system if the system is verified directly at the end. Therefore, timing simulation analysis is carried out on the driver IP of pl-side timing control (such as LCD display driver).

After a long time of design and debugging verification, the system achieved a good overall effect, can realize effective detection of the target edge information, and image acquisition and display can reach the design goal of 60 frames/SEC. However, in the verification process, it was found that there were many noise points in the final edge detection results. In the follow-up study, the image should be filtered after the end of image collection and then the edge detection. If the corrosion expansion treatment can be carried out after the edge detection, the effect will be better.

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