Device Performance of Junctionless Transistors- A Review

Imran Ullah Khan[1], Sai Sharma[2] & Shashi Kant Gupta[3]
pdf.imranuk@lincoln.edu.my, saisharma@lincoln.edu.my & raj2008enator@gmail.com
[1]PDF Scholar Lincoln University, Malaysia

Abstract

In contrast to the classical p-n MOSFET, a Junctionless transistor features identical doping in the source, channel, and drain regions, resulting in a negligible concentration gradient. The Junctionless transistor switches off because of the distinction in the semiconductor's work function and the gate material. Transistors without junctions provide a substantial edge compared to conventional MOSFET devices. Their advantage lies without a p-n junction, leading to simplified fabrication process and improved SCEs. With fabrication of initial Junctionless transistors, many other transistors of this kind have been proposed and investigated. One of them being the core-shell structure. The core-shell design confers inherent benefits to Junctionless (JL) MOSFETs, overcoming the poor mobility, requirement of negative threshold voltage, and stochastic dopant variations, while preserving the merits of the Junctionless transistors. In this paper, the core-shell junction-less transistor is reviewed based on optimizations of core doping succeeded by variations in the length of the gate and the effect of different dielectrics. The study seeks to conduct a simple but comprehensive evaluation of the performance of core-shell junction less FET based on aforesaid parameters to better understand the device's operational capabilities. Figure of merits, especially the ratio of I_{on}/I_{off}, DIBL, as well as Sub-threshold slope, were investigated to emphasize the merits and demerits of different doping profiles and gate length variation. It is demonstrated that an oppositely doped core surrounded by a shell was found to achieve a lower leakage current with a 20 nm length of channel and dielectric constant of 15, performing better than an undoped shell structure. The ratio of on/off current was nearly 10^{12}. Additional benefits include 60.61mv/decade SS and DIBL of 8.5mV/V^{-1}.

Keywords: Junctionless, core-shell, Electrical characteristics, core doping, doping concentration, gate length, dielectrics.

I. Introduction

At present, IC's are prevalent in multiple aspects of life, from desktops to handheld gadgets. With economic and technological progress, demand rises for better efficiency and greater mobility in electronics.

As manufacturing technology progresses, planar MOSFETs shrink, reducing channel length. Consequently, SCE inevitably arises. Recent semiconductor advancements enable exploration of alternative transistor fabrication methods.The goal is to reduce size, increasing transistor density and enhancing performance [1]. Scaling primarily focuses on controlling short-channel effects that impact device efficiency. A multi-gate design significantly enhances electrostatic stability, providing better resistance to short-channel effects [2].

Among multi-gate designs, the CSG MOSFET excels due to superior characteristics, as the gate's full control over the silicon film effectively removes corner effects [3,4]. Although multi-gate MOSFETs improve gate control, optimizing the drain/source profile is crucial to limiting short-channel effects and reducing series resistance [5].This challenge is effectively tackled by adopting a Junctionless (JL) architecture, eliminating the need for p-n junctions. The device was first developed at Tyndall National Institute, Ireland. However, physicist Julius Edgar Lilienfeld initially patented the junctionless transistor principle in 1925. Unlike other transistors, the Lilienfeld design lacked junctions. While a junctionless transistor may seem unconventional, the term "transistor" itself does not inherently denote junctions.

Precisely, the Lilienfeld transistor is a gated trans-resistor, meaning it acts as a resistor controlled by gate that in turn controls carrier density as well as flow. Despite being the earliest patented design, technological constraints in Lilienfeld's time made practical fabrication impossible. On account of technological barrier, Colinge et al. took nearly 85 years to develop the first Junctionless nanowire transistor. These devices offer complete CMOS functionality, featuring an almost ideal subthreshold slope, extremely low leakage current, and minimal mobility degradation with gate voltage variations [6].

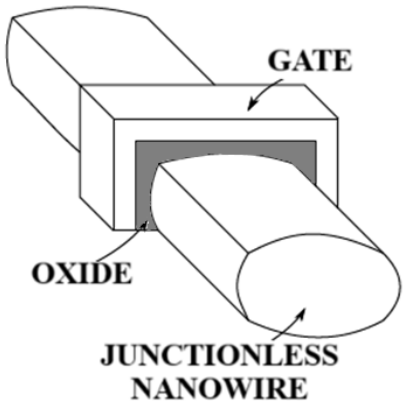

Fig. 1: Structure of Junctionless nanowire transistor [23]

The unparalleled simplicity of JL transistors is what makes them appealing. With a doping profile in the range of 1019 cm3, the device thickness typically needs to be around 5–10 nm. The negative repercussions of high doping include: typically operating in a normally-on state accompanied by a negative VTH, unavoidably diminished mobility of carrier, erratic doping variations, heightened impact ionization, and so on.

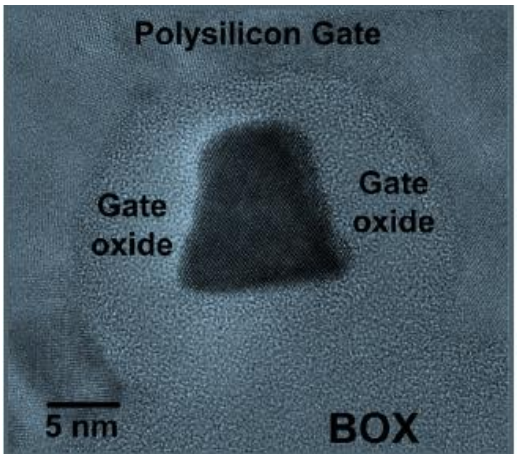

Fig. 2: TEM photograph of a JNT [22]

II. Threshold voltage in Junctionless transistors

Junctionless devices offer great adaptablity in attaining various VTH by adjusting their dimensions [18]. They even exhibit greater threshold voltage reliance on temperature compared to trigate devices [19, 20]. This work presents an analytical model for JNT threshold voltage, emphasizing $Cg_{(ox)}$ and temperature dependence. The prototype accounts for nanowire W, H, doping concentration, thickness, as well as temperature. In JNTs, Vth is determined by depletion region depth rather than accumulation or inversion layer formation. According to Jean-Pierre Colinge, a simple yet effective physical model incorporating bulk and accumulation currents in JLFETs is as follows [19].

VOLTAGE	DRAIN CURRENT
FOR- $V_{GS}>V_{po}$ $V_{GS}<V_{FB}$ $V_{DS}<V_{DSAT1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}(V_{GS}-V_{po})^{n+1} + S_{min}V_{DS}\right)$
$V_{GS}>V_{po}$ $V_{GS}<V_{FB}$ $V_{DS}<V_{DSAT1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}\left((V_{GS}-V_{po})^{n+1} - (V_{GS}-V_{DS}-V_{po})^{n+1}\right) + S_{min}V_{DS}\right)$
$V_{GS}>V_{FB}$ $V_{DS}<V_{DSAT1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}S_{max}C_{ox} + \frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}\left(V_{DS}(V_{GS}-V_{FB}) - \frac{1}{2}V_{DS}^2\right)$
$V_{GS}>V_{FB}$ $V_{DS}<V_{DSAT1}$ $V_{DS}>V_{DSAT2}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}S_{max}C_{ox} + \frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}\left(V_{DS}(V_{GS}-V_{FB}) - \frac{1}{2}V_{DS}^2\right)$
$V_{GS}>V_{FB}$ $V_{DS}>V_{DSAT1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(S_{max}(V_{GS}-V_{FB}) + \frac{S_{max}+nS_{min}}{n+1}(V_{FB}-V_{po})\right) + \frac{1}{2}\frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}(V_{GS}-V_{FB})^2$

III. Capacitance at Gate oxide

IV.

The Cg/l is typically evaluated as :

Cox = (εox.P/tox),

neglecting corner capacitance. This approximation holds when thickness of oxide is much smaller than Width and/or H, such as Width = Height = 60 nm and tox = 2 nm (oxide thickness is 3% of Width and/or Height). However, in smaller devices like JNTs, the tox becomes analogous to Width and Height, e.g., Width = H = 10 nm and tox = 2 nm (tox is 20% of W and/or H). In this case, corner capacitance significantly impacts performance and cannot be ignored. To achieve more accurate oxide capacitance values

$$C_{\text{ox}} = \varepsilon_{\text{ox}}\left(\frac{P}{t_{\text{ox}}} + f\right)$$

Here, **f :** corner capacitance, which remains independent of device dimensions.

V. VARIANT OF JUNCTIONLESS TRANSISTOR

Recently introduced a core-shell variant of the Junctionless transistor, addresses the shortcomings of a traditional Junctionless transistor, for instance, inferior mobility, random dopant fluctuations, and negative threshold voltage, while preserving its distinctive characteristics of lacking junctions [7][8].

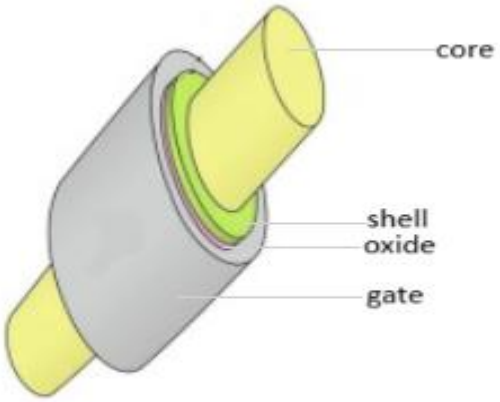

Fig. 2: Structure of core-shell junction-less transistor

Various studies have explored different core structures and the number of gates surrounding the core-shell configuration to date. The core-shell architecture consists of a shell without doping encompassing a highly concentrated doped core, resulting in a high charge, off-state operation, outstanding mobility, and current drive with very high values [7][8]. The addition of a core, doped with an opposite charge interposed between the shells, in the GAA junctionless field-effect transistor, further enhances its performance [8].

A projected improved Core-Shell Dual Gate Junctionless MOSET with heavily doped drain as well as source regions displays a small leakage current with an on-state current at a higher value [9][11]. The Core-Shell-Nanowire-Junctionless-Accumulation-Mode-Field-Effect Transistor demonstrates high transconductance, drain current, Subthreshold Slope, ratio off Ion/Ioff, cut-off frequency, and output conductance compared to the Nanowire-Junctionless-Accumulation-Mode-FET [10]. The study of the rectangular CSDG junctionless transistor in terms of the spacer dielectric and dielectric at the gate shows enhanced efficiency when the core thickness exceeds 3 nm with a dielectric with high k while the core doping is reduced. Additionally, the impact of incorporating spacers indicates optimal device performance with a core thickness of 4 nm along a gate dielectric with lower k. [13].

Core-shell dual-gate (CSDG) junctionless transistors have been investigated for their potential applications in neuromorphic hardware and synaptic devices. These transistors utilize floating body effects, charge trapping, and optimal device design for long-standing depression operations [9][14]. The CSDG nanowire transistor has shown promising results in system-level simulations, achieving high recognition accuracy in pattern recognition tasks [15]. Additionally, the CSDG nanowire transistor is well-suited to CMOS technology, rendering it a compelling contender for neuromorphic hardware implementation [11].

When comparing the performance of misaligned gate classical DGJLFET with rectangular core-shell (RCS) based JL FETs, it's evident that the projected RCS-based structure demonstrates enhanced performance in the condition of a perfectly aligned gate. Furthermore, it exhibits reduced sensitivity to the effects of misalignment of gates compared to classical JLFETs. Specifically, the rectangular CS double gate JLT demonstrates a tolerance boundary of fifty per cent misalignment of the gate, while the conventional structure lacks flexibility in handling gate misalignment.[16]. By ensuring that both the core and shell thicknesses are set to 3 nanometers each, according to the investigation, 20% of misalignment of the gate on both margins of the channel does not significantly affect the performance constraints. This finding alleviates the pressure to achieve perfect gate alignment [17]. The optimal parametric values, such as an OFF current of approximately 10^{-16}A, an ON current of around 10^{-5}A, an Subthreshold Swing of approximately 66.2 mV/decade, an I_{ON}/I_{OFF} ratio of approximately 10^{10}, DIBL of about 42.1 mV/V, and a V_{th} of roughly 0.56 V under faultlessly aligned gate conditions, are achieved by maintaining both core and shell thicknesses at three nanometer each.

The characteristics (I_d vs V_{gs}) of both traditional Nanowire JLFETs and core-shell JLFETs, have been contrasted across various active deposit thicknesses. With a silicon layer of dimension 10 nanometers, the core-shell JLFET demonstrates a remarkable reduction in OFF current by 4 folds, resulting in a substantially high I_{ON}/I_{OFF} of 10^{10}. Additionally, it's observed that the I_{OFF} rises with the decrease in the doping level of the p+ core.

The suggested nanotube semi-JTFET, featuring Ge in the source and Gallium Arsenide as the drain, achieves a nearly 100-fold increase in on-state drive current contrasted with traditional nanowire TFETs. On analysing the sensitivity of the primary electrical variables, it is suggested that the doping concentrations of the source and channel and the metal gate work function prove to be crucial design constraints that significantly impact the efficiency of the device. A higher subthreshold swing in the NSJTFET compared to the conventional TFET, having, an SS of 25 mV/dec suggests that the NSJTFET may have a slightly less efficient switching performance [12].

On comparing the transfer characteristics of the Core-shell JLFET, having a shell thickness of 2 nm with the Nanowire JLFET with diameters of 10 nanometres and 20 nanometres, it is observed that CSJLFET with 20 nm diameter have comparable characteristics with nanowire of diameter 10 nm. Whereas, NW Junctionless FET with a diameter of 20 nm show a higher drain current for the same Vgs.

Increasing the doping concentration of the Polysilicon gate in DG JL MOSFET can also reduce leakage current, but it results in low I_{on}.

The cut-off frequency of the modified CS dual gate JLMOSFET increases as the length of the gate decreases, reaching up to 600-900 GHz, making it a promising candidate for the THz gap [9].

VI. Conclusion

The use of alternative materials like indium-gallium-arsenide, GaN, and germanium is limited due to charge trapping at the interface and interface defects. However, JLFETs can efficiently utilize these high-mobility materials since bulk carriers are less influenced by the interface.

Due to the volume conduction mechanism in junctionless transistors, the interaction between the dielectric interface and carrier flow is reduced. As a result, they demonstrate higher immunity to defects and interface traps compared to Ge MOSFETs [22-24]. Additionally, Ge JLFETs exhibit a band gap of 2.36 eV when the film thickness is 1 nm, which decreases to 0.86 eV at 3 nm thickness [25]. By surrounding a heavily doped core with an undoped shell, the transistor achieves off-state operation, outstanding mobility, and usually high current drive with high charge. The addition of the undoped shell eliminates the weaknesses of a traditional JLFET, like degraded mobility, opposite threshold voltage, and arbitrary dopant fluctuations, even though maintaining its attractive properties. In the projected rectangular CS-Dual Gate JLMOS, the presence of an opposite doping core results in a significant depletion effect, improving the device's performance. The doping profiles, dielectric constants, thickness of gate oxide and silicon, and core doping are all factors that can be varied to study the potential profile and transfer characteristics of the core-shell junctionless transistor.

Additionally, approximating SCEs in shell-doped DG JL MOSFETs highlights the usability of shell doping as well as core thickness in controlling SCEs and optimizing the core-shell JL architecture for low-power applications. The core-shell architecture in the CS GAA JLFET, with a differently doped core, interposed between the shells, contributes to performance improvements. CS GAA JLFET has the potential to elevate the efficiency of junctionless FET, offering better control over device operation and improved energy efficiency.

Nearly all Junctionless device topologies exhibit a higher **Ion/Ioff** ratio along with improved **DIBL** and **SS** values. Junctionless transistors present a promising alternative to traditional MOSFETs and have the potential to replace them in future technologies.

References:

[1] Shubo Zhang 2020 J. Phys.: Conf. *Ser.* 1617 012054 Review of Modern Field Effect Transistor Technologies for Scaling

[2] Ferain I, Colinge C A and Colinge J-P 2011 Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors Nature 479 310–6

[3] K.P. Pradhan, M.R. Kumar, S.K. Mohapatra, P.K. Sahu, Analytical modeling of threshold voltage for Cylindrical Gate All Around (CGAA) MOSFET using centre potential, Ain Shams Engineering Journal, Volume 6, Issue 4,2015 Pages 1171-1177, ISSN 2090-4479

[4] Y. Siddiqui, N. Mittal and I. U. Khan, "Performance Analysis and Characterization of Double Gate and Gate All Around MOSFET," 2021 10th International Conference on System Modeling & Advancement in Research Trends (SMART), India, 2021, pp. 614-617, doi: 10.1109/SMART52563.2021.9676257.

[5] Hisamoto D, Lee W-C, Kedzierski J, Takeuchi H, Asano K, Kuo C, Anderson E, King T-J, Bokor J and Hu C 2000 FinFET—a self-aligned double-gate MOSFET scalable 20 nm IEEE Trans. Electron. Devices 47 2320–5

[6] Colinge, JP., Lee, CW., Afzalian, A. et al. Nanowire transistors without junctions. Nature Nanotech **5**, 225–229 (2010). https://doi.org/10.1038/nnano.2010.15

[7] Sorin Cristoloveanu, Gérard Ghibaudo, The core-shell junctionless MOSFET, Solid-State Electronics, Volume 200,2023108567, ISSN 0038 1101, https://doi.org/10.1016/j.sse.2022.108567.

[8] Rewari, S. Core-Shell Nanowire Junctionless Accumulation Mode Field-Effect Transistor (CSN-JAM-FET) for High-Frequency Applications - Analytical Study. *Silicon* **13**, 4371–4379 (2021). https://doi.org/10.1007/s12633-020-00744-3

[9] Ajay Resistances and ESD Reliability Study of Core-Shell Channel Junctionless DG

[10] MOSFET. *Silicon* **13**, 1325–1329 (2021). https://doi.org/10.1007/s12633-020-00527-w

[11] Ahangari, Z. Performance optimization of a nanotube core–shell semi-junctionless p^+p^+n heterojunction tunnel field effect transistor. *Indian J Phys* **95**, 1091–1099 (2021). https://doi.org/10.1007/s12648-020-01776-6.

[12] Vishal Narula, Amit Saini & Mohit Agarwal (2023) Correlation of Core Thickness and Core Doping with Gate & Spacer Dielectric in Rectangular Core-Shell Double Gate Junctionless Transistor, IETE Journal of Research, 69:7, 4492-4503, DOI: 10.1080/03772063.2021.1946437

[13] Ansari, M.H.R.; Kannan, U.M.; Cho, S. Core-Shell Dual-Gate Nanowire Charge-Trap Memory for Synaptic Operations for Neuromorphic Applications. *Nanomaterials* **2021**, *11*, 1773. https://doi.org/10.3390/nano11071773

[14] M. H. Raza Ansari, D. Kim, S. Cho, J. -H. Lee and B. -G. Park, "Core-Shell Dual-Gate Nanowire Synaptic Transistor with Short/Long-Term Plasticity," *2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, Chengdu, China, 2021, pp. 1-3, doi: 10.1109/EDTM50988.2021.9420876.

[15] Vishal, Narula., Mohit, Agarwal. Effect of gate misalignment on the performance of rectangular core-shell based junctionless field effect transistor. (2020).;2265(1):030481-. doi: 10.1063/5.0016611

[16] Vishal Narula and Mohit Agarwal. Impact of core thickness and gate misalignment on rectangular core-shell based double gate junctionless field effect transistor, 2020 Semicond. Sci. Technol. 35 035010 DOI 10.1088/1361-6641/ab6bb2

[17] Kranti A, Yan R, Lee C-W, Ferain I, Yu R, Akhavan N D, Razavi P and Colinge J-P 2010 Junctionless nanowire transistor (JNT): Properties and design guidelines Proc.European Solid-State Dev. Research Conf. pp 357–60

[18] Lee C W, Borne A, Ferain I, Afzalian A, Yan R, Akhavan N D,Razavi P and Colinge J-P 2010 High-temperaturenperformance of silicon junctionless MOSFETs IEEE Trans. Electron Devices 57 620–5

[19] de Souza M, Pavanello M A, Trevisoli R D, Doria R T and Colinge J-P 2011 Cryogenic operation of Junctionless nanowire transistors IEEE Electron Device Lett. pp 1–3

[20] Sallese J-M, Chevillon N, Lallement C, I˜niguez B and Pr´egaldiny F 2011 Charge-based modeling of junctionless double-gate field-effect transistors IEEE Trans.Electron Devices 58 2628–37

[21] Reduced electric field in junctionless transistors Jean-Pierre Colinge,a Chi-Woo Lee, Isabelle Ferain, Nima Dehdashti Akhavan, Ran Yan, Pedram Razavi, Ran Yu, Alexei N. Nazarov,b and Rodrigo T. Doriac Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland

[22] Singh, D.K.; Kumar, P.K.; Akram, M. Investigation of Planar and Double-Gate Junctionless Transistors with Non-Uniform Doping. In Proceedings of the 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur, India, 2–4 November 2018; pp. 1–5.

[23] K. S. Im, J. H. Seo, Y. J. Yoon, Y. I. Jang, J. S. Kim, S. Cho, J. H. Lee, S. Cristoloveanu, J. H. Lee, and I. M. Kang, “GaN junctionless trigate field-effect transistor with deep submicron gate length: Characterization and modeling in RF regime, Jap. J. Appl.Phys., vol. 53, no. 11, 118001, Oct. 2014.

[24] Nupur Mittal, Imran Ullah Khan, Piyush Charan, Design and performance analysis of low power fully integrated tunable bandpass filter,Materials Today: Proceedings,2023 ISSN 2214-7853,https://doi.org/10.1016/j.matpr.2023.03.369.

[25] Singh, D.K.; Kumar, P.K.; Akram, M. Investigation of Planar and Double-Gate Junctionless Transistors with Non-Uniform Doping. In Proceedings of the 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur, India, 2–4 November 2018; pp. 1–5.

[26] Nowbahari, Arian & Roy, Avisek & Marchetti, Luca. (2020). Junctionless Transistors: State-of-the-Art. Electronics. 9. 1174. 10.3390/electronics9071174.

[27] Shubham Sahay; Mamidala Jagadesh Kumar, "Fundamentals of Junctionless Field-Effect Transistors," in Junctionless Field-Effect Transistors: Design, Modeling, and Simulation , IEEE, 2019, pp.67-123, doi: 10.1002/9781119523543.ch3.

[28] V. Djara, L. Czornomaz, V. Deshpande, N. Daix, E. Uccelli, D. Caimi, M. Sousa, and J.Fompeyrine, “Tri-gate InGaAs-OI junctionless FETs with PE-ALD Al2O3 gate dielectricand H2/Ar anneal,” Solid-State Electron., vol. 115, pp. 103–108, Jan. 2016.

[29] S. Yi, Z. Chen, R. Dowdy, K. Chabak, P. K. Mohseni, W. Choi, and X. Li, “III–V Junctionless gate-all-around nanowire MOSFETs for high linearity low power applications,” IEEE Electron Device Lett, vol. 35, no. 3, pp. 324, 2014.

[30] K. H. Goh, S. Yadav, K. I. Low, G. Liang, X. Gong, and Y. C. Yeo, “Gate-all-around In0.53Ga0.47As junctionless nanowire FET with tapered source/drain structure,” IEEE Trans. Electron Devices, vol. 63, no. 3, pp. 1027–1033, Mar. 2016.

[31] J. H. Seo, S. Cho, and I. M. Kang, “Simulation for silicon-compatible InGaAs-based junctionless field-effect transistor using InP buffer layer,” Semicond. Sci. Technol.,vol. 28, no. 10, 105007, Aug. 2013

[32] K. S. Im, C. H. Won, Y. W. Jo, J. H. Lee, M. Bawedin, S. Cristoloveanu, and J. H. Lee, “High-performance GaN-based nanochannel FinFETs with/without AlGaN/GaN heterostructure,” IEEE Trans. Electron Devices, vol. 60, no. 10, pp. 3012–3018, Oct. 2013.