

A COMPREHENSIVE REVIEW OF FINFETS: A PARADIGM SHIFT IN SEMICONDUCTOR DESIGN

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Abstract:

Fin Field-Effect Transistors (FinFETs) have become an essential technology in modern semiconductor devices, addressing the constraints of conventional planar MOSFETs. As device dimensions decrease to the nanoscale, Short-Channel Effects (SCEs) become increasingly significant, impairing device performance. FinFETs mitigate these issues by a three-dimensional fin-like architecture that boosts electrostatic control, diminishes leakage current, and augments drive current. This paper reviews the history, design factors, and performance advantages of FinFETs, emphasizing their influence on contemporary CMOS technology. Different FinFET architectures, such as Tri-Gate, Double-Gate, and Gate-All-Around (GAA) topologies, are examined, emphasizing their benefits compared to traditional MOSFETs. The review includes the influence of high-k dielectrics, strain engineering, and material breakthroughs on enhancing FinFET performance. A survey of emerging applications in high-performance computing, low-power electronics, and artificial intelligence highlights the importance of FinFETs in next-generation semiconductor technology. The move from FinFETs to nanosheet and GAA transistors is succinctly discussed, offering insights into prospective scaling trends. This thorough assessment seeks to provide an in-depth analysis of the progress and current advances in FinFET technology.

Keywords: FinFET; Leakage current; High k Dielectrics; Short Channel Effects; Nanoscale.

Introduction:

The invention of FinFET transistor technology can be traced back to Japan, specifically to the development of the Depleted Lean-channel Transistor, or DELTA, in 1989.

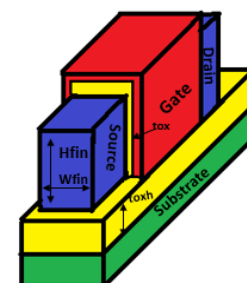
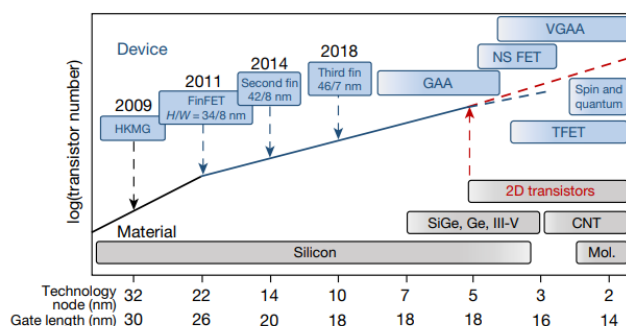


Fig.1 Technology node and gate length versus transistor scaling[1] **Fig.2** Schematic diagram of 3D FinFET.

The figure.2 shows 3D FinFET. FinFETs exhibit an improved Subthreshold Swing (SS) slope, superior stability in the I_{ON}/I_{OFF} ratio, and reduced intrinsic gate capacitance relative to bulk MOSFETs. Multigate variations of the FinFET transistor, such as double gate and tri-gate configurations, are employed to enhance the short channel characteristics. FinFET is a transistor characterized by its vertical channel architecture, which can be fabricated utilizing advanced three-dimensional technology. The system necessitates a reduced power supply, exhibits diminished short channel effects, and functions at a significantly higher speed relative to traditional bulk silicon CMOS technology. The current 3D structures are integral components of the modern semiconductor industry, primarily due to their efficiency in power consumption, enhanced speed, compact size, and reliability, which have garnered significant focus within the realms of microelectronics, chip design, computing, and data processing. By manipulating various physical parameters such as fin height, fin width, gate oxide thickness, and gate length, it is possible to enhance FinFET nodes [2]. The fabrication of FinFET is shown in figure.3. Triple gates and GAAFET represent a selection of devices that have been explored to manage short-channel effects, thereby facilitating the continuation of Moore's law while maintaining consistent device performance. The discourse surrounding the replacement of FinFETs frequently centers on gate-all-around field-effect transistors that utilize vertically stacked horizontal nanosheets. The GAAFET technology was initially conceived in 1988 by the Toshiba ULSI Research Center. In contrast to FinFET, which features a three-sided channel with the gate, GAAFET possesses a gate that surrounds the channel entirely, thus the designation gated-all-around. The present generation of GAAFETs exhibits superior performance across various parameters when contrasted with the existing FinFETs.

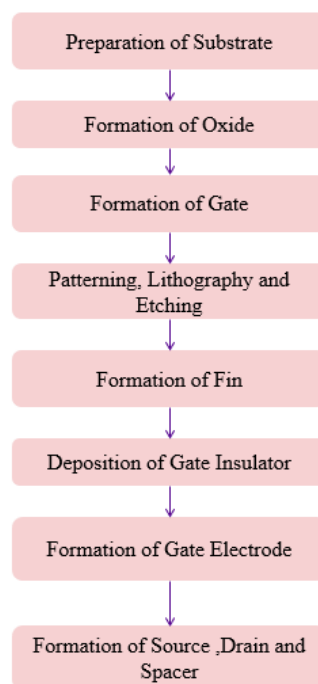
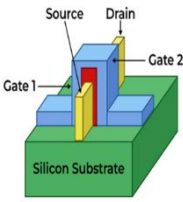
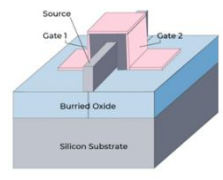
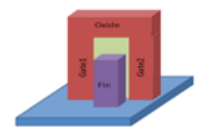
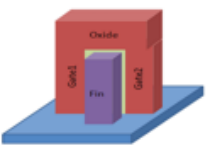
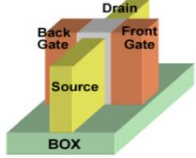
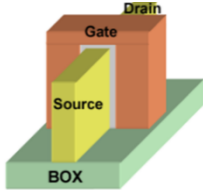
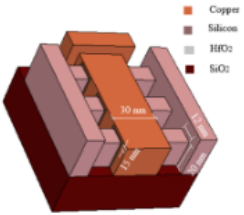


Fig.3 Fabrication of FinFET.

Various FinFET architectures:

To overcome the short channel effects of planar MOSFETs, there was a need for double vertical gate(FinFET), Triple gate(Trigate), Omega-shaped gate(Ω -gate), T-channel FET and GAA nanowires. The following are various FinFET architectures .

Types of FinFET	Description	Structure of FinFET
Bulk FinFET[3]	<ol style="list-style-type: none"> 1. Bulk FinFET is built on a silicon wafer with an insulating layer (usually silicon dioxide) between the fin and the substrate. 2. The fin is isolated from the bulk substrate by this insulating layer. 3. Lower leakage currents because the insulating layer reduces parasitic effects. 	 <p>The diagram shows a 3D perspective of a Bulk FinFET. A central vertical fin is shown in blue. It is flanked by two gates, Gate 1 (left) and Gate 2 (right), shown in red. The top of the fin is labeled as the Source and Drain. The entire structure is built on a Silicon Substrate, which is shown in green.</p>
SOI FinFET[4]	<ol style="list-style-type: none"> 1. SOI FinFET is built on a silicon wafer with an insulating layer (usually silicon dioxide) between the fin and the substrate. 2. The fin is isolated from the bulk substrate by this insulating layer. 3. Lower leakage currents because the insulating layer reduces parasitic effects. 	 <p>The diagram shows a 3D perspective of an SOI FinFET. A central vertical fin is shown in pink. It is flanked by two gates, Gate 1 (left) and Gate 2 (right), shown in blue. The top of the fin is labeled as the Source. The fin is built on a Buried Oxide layer, which is shown in light blue, and this is on top of a Silicon Substrate, shown in grey.</p>
Double Gate FinFET[5]	<ol style="list-style-type: none"> 1. In Dual Gate FinFET the channel is controlled by two gates—one on each side of the fin (front and back). 2. Offers improved control over the channel compared to planar transistors but is less effective than tri-gate designs. 	 <p>The diagram shows a 3D perspective of a Double Gate FinFET. A central vertical fin is shown in purple. It is flanked by two gates, Gate 1 (left) and Gate 2 (right), shown in red. The top of the fin is labeled as the Oxide. The entire structure is built on a blue substrate.</p>
Trigate FinFET[5]	<ol style="list-style-type: none"> 1. In Trigate FinFET the channel is surrounded by three gates—one on the top and one on each side of the fin. 2. Provides superior control over the channel, significantly reducing short-channel effects and leakage currents. 	 <p>The diagram shows a 3D perspective of a Trigate FinFET. A central vertical fin is shown in purple. It is flanked by two gates, Gate 1 (left) and Gate 2 (right), shown in red. The top of the fin is labeled as the Oxide. The entire structure is built on a blue substrate.</p>

<p>Independent Gate FinFET[6]</p>	<p>1.The front and back gates are controlled independently</p> <p>2.More complex design and layout.</p>	
<p>Shot Gate FinFET[6]</p>	<p>1.The front and back gates are electrically connected and controlled as a single gate.</p> <p>2.Design complexity is reduced when compared to IG FinFETs.</p>	
<p>Multifin FinFET[7]</p>	<p>1.Significantly improves the mobility of charge carriers.</p> <p>2.For numerous applications, a tall fin of fin field-effect transistor (FinFET) serves as an effective model, and the multi-fin configuration of the FinFET yields similarly promising results regarding power gain.</p>	

Self heating effects in FinFET technology:

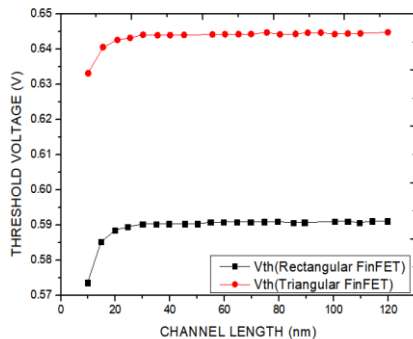
In FinFET technique, self-heating effects arise due to the interplay of its structural characteristics, scaling considerations, and the influence of electrical charges. In the realm of contemporary technologies, one can identify the self-heating effect (SHE) in electronic devices as a significant contributor to thermal stress factors. The results of the self-heating experiments indicate that self-heating is more pronounced in all varieties of 3D-gate FETs when compared to planar devices [8]. The planar devices dissipate thermal energy directly via the bulk material and the contact interfaces. In FinFETs, thermal energy accumulates at the apex of the fins, gradually dispersing through the fins towards the base and subsequently transferring to the substrate and contacts. As the quantity of fins within a FinFET architecture escalates, there is a corresponding rise in the drain current, which results in an augmentation of conduction channels.

Advancements in FinFET materials:

High-k dielectrics, exemplified by HfO₂ (hafnium dioxide), are being studied for their superior physical thickness and elevated barrier height compared to SiO₂. Currently, HfO₂ is extensively utilized due to its ability to significantly diminish leakage current, attributed to its high dielectric constant, which surpasses that of SiO₂. Among SiO₂, HfO₂, and TiO₂ gate materials, TiO₂ exhibits a significantly elevated drain current characteristic. Gallium nitride (GaN) is emerging as a lead material in FinFETs. Gallium Nitride, a binary III/V group direct bandgap compound semiconductor, offers high charge carrier mobility and an exceptionally high breakdown voltage. Furthermore, ferroelectric materials are integrated in the interest of achieving ultra-low power consumption in FinFETs[9].

Various FinFET applications:

FinFETs are engineered to exhibit reduced power consumption while maintaining elevated operational frequencies. This has facilitated the advancement of FinFETs through optimized



RF and analog applications. The primary domain in which FinFETs are utilized is in biomedical applications, specifically in the development of biosensors. Field-effect transistors (FETs) are utilized in oxygen sensors for divers to measure the partial pressure of oxygen in the breathing gas mixture. A junction-less accumulation-mode gate stack gate-all-around (JAM-GS-GAA) FinFET is introduced to enhance the fin aspect ratio. This study demonstrates that a reduced aspect ratio markedly improves linearity, minimizes harmonic distortion, and enhances RF/analog

performance [10].

Comparison of Rectangular FinFET and Triangular FinFET:

Fig.3 Comparison of rectangular and triangular FinFET for threshold voltage by varying the channel length.

The suppression of SCE is significantly more effective in the triangular fin configuration when contrasted with the rectangular fin layout. The reduction of SCE immunity correlates with an increase in H_{fin} in FinFET structures. In the case of rectangular FinFETs, the fin width remains uniform across the entire dimension of W_{fin} . In triangular FinFETs, the fin width exhibits a non-uniform characteristic, with distinct measurements for the top $W_{fin,top}$ and bottom $W_{fin,bottom}$ segments of the fin [11]. As illustrated in fig.3, the threshold voltage exhibits an increase when transitioning from wider to narrower fin widths, specifically from Rectangular FinFET to Triangular FinFET. The elevation in threshold voltage is significantly more evident for HfO_2 . At a channel length of 15 nm, the variation in threshold voltage between Rectangular FinFET and Triangular FinFET is approximately 18% when utilizing SiO_2 as the dielectric material.

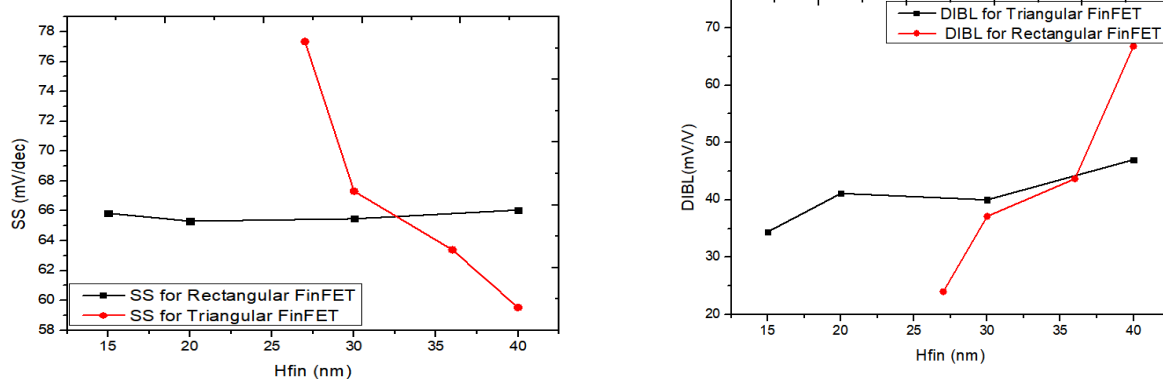


Fig.4 Subthreshold slope and DIBL for Triangular and Rectangular FinFET for varying fin heights.

In Fig.4 Triangular FinFET shows better values of SS and DIBL as compared to the Rectangular FinFET, because of increased fin height and enhanced doping concentration. In particular, in the configuration of Triangular FinFET, SS is found to be 68.56 mV/decade while DIBL measures 31.81 mV/V[12].

When the parameters are noted for conventional FinFET, I_{on} , I_{off} and SS are found to be 101 μ A, 0.508 nA and 65.33 mV/dec respectively[13]. Also for triangular FinFET, I_{on} is found to be 100 μ A, I_{off} is 0.065 nA and SS is 56 mV/dec[14].

Conclusion

This study reviews several performance indicators of FinFETs across different architectures and materials. SCEs are much diminished in FinFETs compared to planar MOSFETs. The development of various FinFET architectures is examined. This review article meticulously addresses the ongoing discourse surrounding 'FinFET' technologies by providing a comprehensive overview of advancements in modified architectures, prevailing trends, and their limitations. It elucidates the increasing significance of alternative semiconductor materials beyond Silicon and critically examines the evolving FinFET technology, highlighting its notable deficiencies and fabrication challenges in a detailed manner. The forthcoming advancements in transistor design, specifically GAA nanosheets and stacked nanosheet FETs, are already in the conceptual phase. The foundational principles established by FinFET technology will persist, supporting future innovations and sustaining Moore's Law, thereby facilitating the progression of new and enhanced electronic systems.

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