PERORMANCE EVALUATION OF CARBON NANO TUBE FIELD EFFECT TRANSISTORS BASED CONTENT ADDRESSABLE MEMORIES

[1] Imran Ullah Khan, [2] Shashi Kant Gupta
Postdoctoral Fellow Lincoln University, Malaysia
[1]pdf.imranuk@lincoln.edu.my

Abstract: To cater to the power utilization problem, cached routing data is exploited. The routing data is permanently cached either be it Content-Addressable Memory (CAM) or Static Random Access Memory (SRAM). CAM is the expansion of SRAM which compares the stored information with searched information. Pertinent to quick parallel search operations can be used in numerous connectivity-based circuits and network routers. The areas of application of the proposed CAM are network routers, controllers of cache and look up tables (LUTs). For comparative operation CAM having extra circuitry, is identical to RAM. The key challenge is to design advanced circuits that consume less power without negotiating efficiency. Nanoscale Complementary Metal Oxide Semiconductor (CMOS) circuits face some limitations, like short-channel effects, leakage currents, and source-to-drain tunneling. Carbon Nanotube Field Effect Transistors (CNTFETs) are a capable alternative to conventional CMOS technology, due to their high electron mobility, near-ballistic transport behaviour, strong drive current capability, and reduced device dimensions. Strategies concerning energy recoveries are also gaining significant attention, indicating enhanced efficiency over existing techniques. The integration of CNTFETs with energy recovery methods in circuit design has shown good results. An optimised set of CNTFET parameters—such as the number of nanotubes, chirality vector, pitch, dielectric constant, and dielectric material—has been employed in the design of Content-Addressable Memory (CAM) cells. Owing to adiabatic logic, an optimised CNTFET-based Binary CAM (BCAM) is projected. This design outclasses recent implementations reported in the literature, especially in terms of average power consumption and search delay. In addition to CAM cells, supporting circuits such as decoders and priority encoders that are required for constructing a CAM array are also designed. The proposed CNTFET-based BCAM array shows superior performance compared to its CMOS-based counterpart.

Keywords: SRAM; DRAM; CNTFET; CMOS; Look up table

Introduction

For effective performance of LUT, CAM is the hardware solution. Content-Addressable Memory (CAM) is one of the co-processors often used in Network Processing Units (NPUs) to take over tasks related to lookup tables, helping lighten the load on the main processor. Apart from

networking, CAMs have also been useful in a variety of areas, like virtual memory systems [1–2], cache-related memory operations [3–4], database acceleration [5], data compression [6], and even image processing [7]. In recent years, they've also been increasingly used for pattern matching [8–9]. Networking continues to be the main field where CAMs remain prominent, especially in critical tasks like packet classification and packet forwarding. CAM cell structures are typically built using conventional SRAM cells along with additional comparison circuitry. These cells support both **READ** and **WRITE** operations, in addition to the **SEARCH** function. One of the features of CAM is that the entire search operation is completed within a single clock cycle. Unlike classical memory, where the user provides an address and the memory returns the corresponding data, CAM works in reverse: the user inputs the data, and the CAM returns the address where a match is found. If no match exists, a "no match" indication is returned. When multiple matches occur, a **priority encoder (PE)** is used to determine the highest-priority match. Ability to perform searches in parallel across all cells, makes the CAM efficient and the search operation extremely fast

Content Addressable Memory (CAM)

In networking, CAMs mainly use READ and WRITE functions when the system needs to update or test the tables. But most of the power a CAM chip uses goes into SEARCH operations, since these happen very often and across many cells at once. CAM-based search engines are great for speeding up how quickly network devices can find data, but they also use a lot of power because everything is searched at the same time. For example, an 18Mb TCAM running at 250 million searches per second can use around 15 watts of power [4].

This power use is expected to go up even more for two reasons:
(1) Moving from IPv4 to IPv6 : means longer internet addresses, which need bigger CAMs—these are slower and need more energy.
(2) Internet speeds are getting faster (like OC-768), which means the CAM needs to search even quicker. But making it faster also makes it use more power.

The amount of power that an integrated circuit (IC) can handle is limited by how well it can get rid of heat. If it gets too hot, it needs special (and often expensive) cooling systems to manage the extra power. CAMs, because of their high power use, increase both the cost of packaging and the temperature inside the chip. This can lead to other problems like lower efficiency and reduced reliability.

So, to make CAMs more cost-effective and efficient, it's important to reduce their power consumption. This is especially important for portable devices, where saving energy means longer battery life.

The total power used by a CAM comes from two parts:
(i) **Static power** – the power used when the circuit is idle (usually very small), and
(ii) **Dynamic power** – the power used when the circuit is active and switching.

Most of the power is dynamic, and it's calculated using a specific equation [21].

$$P_D = \alpha\, C\, V_{SW}\, V_{DD}\, f \qquad (1)$$

Where α denotes average switching activity, C denotes the total node capacitance, V_{SW} denotes average voltage swing, V_{DD} represents the voltage supply, and f denotes the frequency of operation.

CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNTFETS)

Carbon Nanotubes (CNTs) are tiny, tube-shaped structures that can be either Single-Walled (SWCNT) or Multi-Walled (MWCNT). As shown in Fig. 1, a SWCNT is formed by rolling up a sheet of graphene (a single layer of graphite) using a wrapping vector defined as: $Ch = n_1a + n_2b$,

where n_1 and n_2 are positive integers that determine the chirality (or twist) of the tube, and a and b are unit vectors of the hexagonal carbon structure.

Values of n1 and n2 decide whether a SWCNT behaves like a metal or a semiconductor. If (n_1 - n_2) is a multiple of 3, the nanotube is metallic. Otherwise, it behaves as a semiconductor [87].

Based on the relationship between n_1 and n_2, SWCNTs are often described as armchair, zigzag, or chiral. Armchair CNTs, where $n_1 = n_2$, are always metallic. In zigzag CNTs, either n_1 or n_2 is zero. Chiral CNTs have both n_1 and n_2 non-zero and unequal. Both zigzag and chiral CNTs can act as conductors if the difference (n_1 - n_2) is a multiple of 3. If not, they become ideal for use in CNTFETs (Carbon Nanotube Field Effect Transistors) [88].

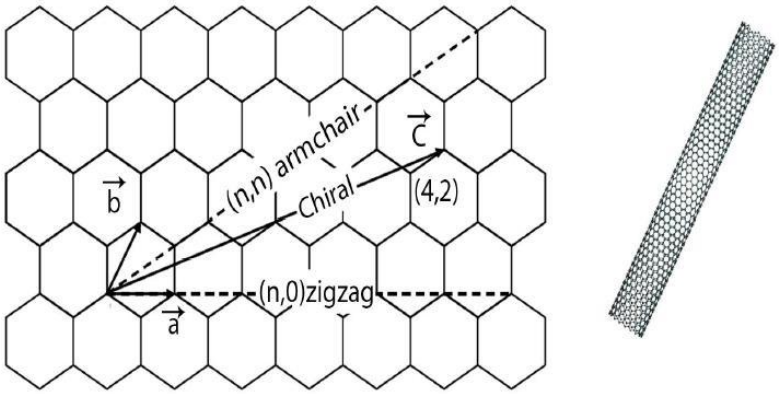

Fig 1: Unrolled sheet of graphite and the rolled lattice structure of CNT

Structure of CNTFET

There are three main types of Carbon Nanotube Field Effect Transistors (CNTFETs), commonly referred to as Schottky Barrier CNTFETs (SB-CNTFETs), MOSFET-like CNTFETs (M-CNTFETs), and Band-to-Band Tunneling CNTFETs (B-CNTFETs or TCNTFETs).

The SB-CNTFET operates based on the principle of quantum tunnelling through a Schottky barrier formed at the junction between the source and the carbon nanotube channel. This tunnelling mechanism is responsible for current injection, differentiating it from the thermionic emission process used in standard MOSFETs.

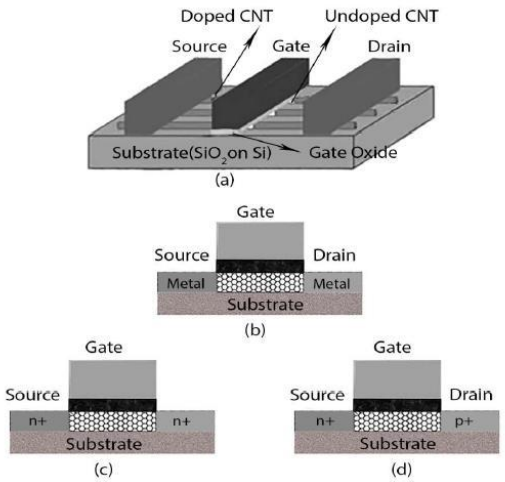

Fig 2: Carbon nanotube field effect transistor (CNTFET) (a) Schematic view of a CNTFET device, (b) SB-CNTFET, (c) M-CNTFET, (d) T-CNTFET

This type of CNTFET, shown in Fig. 2, is built by forming a direct contact between a metal and a semiconducting carbon nanotube. However, the presence of a Schottky barrier (SB) at the metal-CNT junction limits the transconductance of the device in the ON state. As a result, the current-driving capability is reduced, which makes SB-CNTFETs less suitable for high-speed applications. Another drawback of SB-CNTFETs is their strong ambipolar behaviour, meaning they conduct both electrons and holes, which can be undesirable, especially in complementary logic circuits where distinct switching behaviour is required.

To overcome these limitations, a new design known as the MOSFET-like CNTFET (M-CNTFET) was introduced, which helps eliminate the drawbacks associated with Schottky barrier contacts.

Related work

In [11], a novel CAM architecture was introduced, which demonstrated improved performance over existing designs reported in the literature. The proposed CAM cell exhibited significant enhancements in search delay, Power-Delay Product (PDP), and Energy-Delay Product (EDP). Notably, the design demonstrated a substantial reduction in power consumption, particularly under mismatch conditions, making it a more energy-efficient solution.

This research work, in addition, also introduces an efficient Match-Line (ML) sensing method. In [12], the authors proposed Zi-CAM, a power-efficient Binary CAM (BCAM) architecture. The architecture is composed of two main components, namely, the RAM Block (RB) and the Lookup Tables Block (LB). The RB is activated when the input search word contains a sequence of repeating zeroes; else, the LB is triggered. The proposed Zi-CAM architecture has demonstrated

improved power efficiency and reduced resource utilisation compared to other CAM architectures reported in the literature.

In [13], the researchers came up with a new type of analog CAM circuit that uses memristors to store data. Instead of using traditional digital storage, the data is held through adjustable conductance values in the memristors. Uniqueness of the design is that it can handle both analog and digital inputs, giving it more flexibility. The results were remarkable—power consumption was reduced by 37 times compared to regular digital CAMs. As well as, the analog version takes up less space on the chip, making it more compact. Because of these features, this analog CAM is a great fit for areas like probabilistic computing and decision tree applications.

In [14], based on P-MTJ (Perpendicular Magnetic Tunnel Junction) technology, the authors presented a Binary CAM (BCAM) design, using a 1T–1R configuration, where "1T" stands for one transistor and "1R" stands for one resistor. This design was developed to create a high-density, non-volatile CAM.

The CAM cell works by comparing the resistance difference between stored data and the input data during a search operation. This approach permits the creation of a compact and efficient non-volatile CAM cell. One of the key benefits of this structure is that it prominently reduces the switching activity of CAM cells, resulting in lower energy consumption for every search operation.

In [15], the authors proposed a CMOS-based CAM cell that incorporates elements of an STG DICE memory array along with an XOR logic gate. Placed over 4 μm apart on the chip, the transistors in this design are split into two identical groups. The layout was developed to enhance matching performance in microprocessor-based applications.

In [16], the first packet classification method using Binary CAM (BCAM) was introduced by the authors. The process was divided into two main steps: first, the multidimensional lookup was converted into a one-dimensional format; further, BCAM was used to perform a perfect match check. Additionally to improve speed, they introduced optimisation techniques. The proposed design was tested with 17 different packet types and outperformed traditional CAM cells in terms of the number of bits required. However, a throughput limitation was encountered, which affected its overall data handling speed.

Method, Experiments and Results

A BCAM cell circuit employing three CNTFET devices has been developed, focusing on the execution of the search operation. The proposed designs are based on three enhanced adiabatic logic families: Improved Efficient Charge Recovery Logic (IECRL), Improved Positive Feedback Adiabatic Logic (IPFAL), and Improved Pass Transistor Adiabatic Logic (IPTAL). The detailed circuit implementations corresponding to each design are shown in Figures 1,2 & 3.

These architectures aim to improve performance and reduce energy consumption by integrating CNTFETs with adiabatic logic, which is known for its ability to recycle charge during transitions. This approach significantly lowers dynamic power dissipation compared to conventional logic

styles. In the implemented circuits, the Precharge Control (PC) signal acts as the Word Line (WL), and is modeled as a sinusoidal waveform. This waveform shape is a key characteristic of adiabatic circuits, enabling smoother charging and discharging processes and contributing to reduced energy loss during operation.

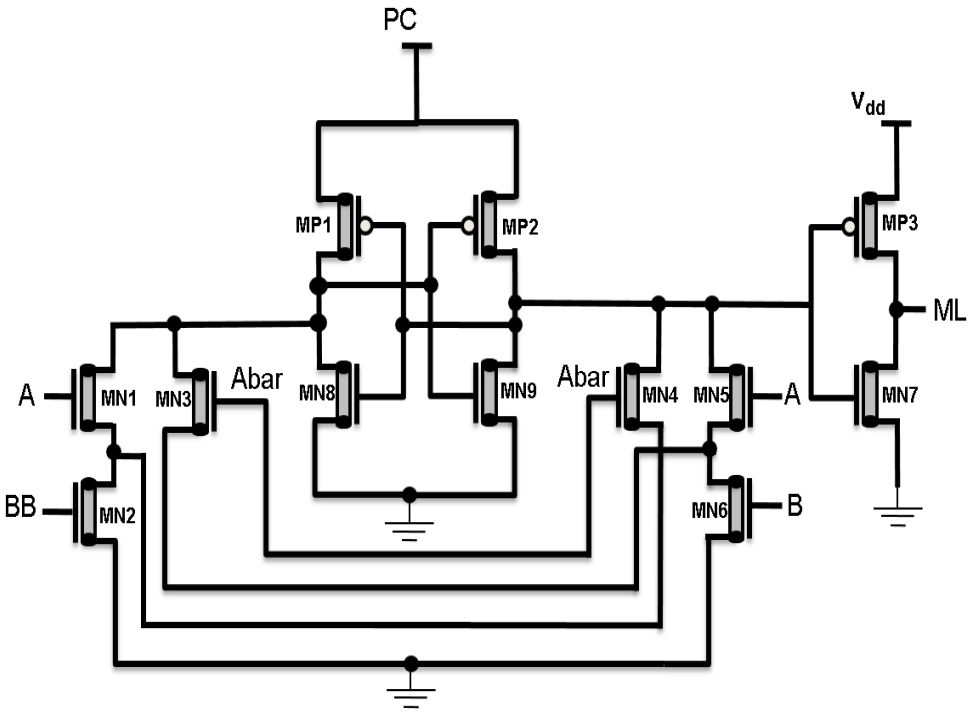

Fig 1. IECRL CAM cell based on CNTFET

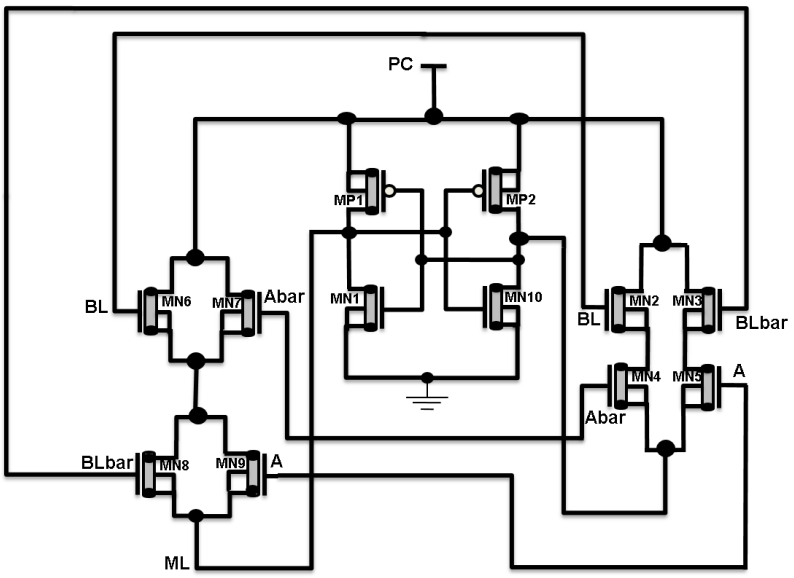

Fig 2. IPFAL CAM cell based on CNTFET

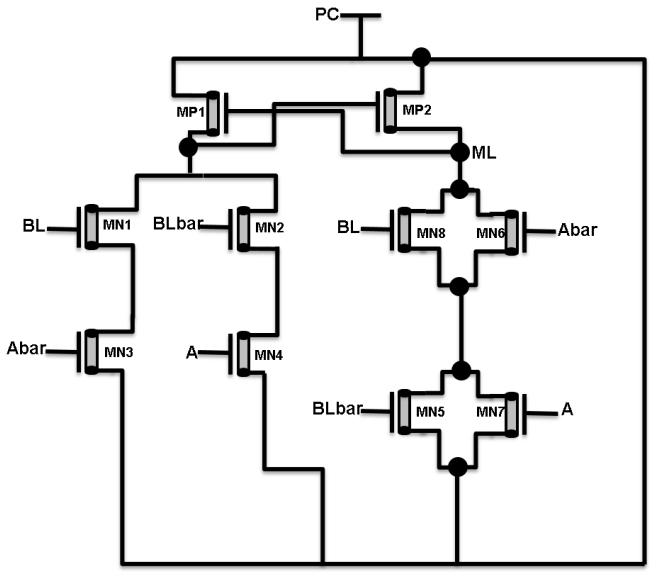

Fig 3. IPAL CAM cell based on CNTFET

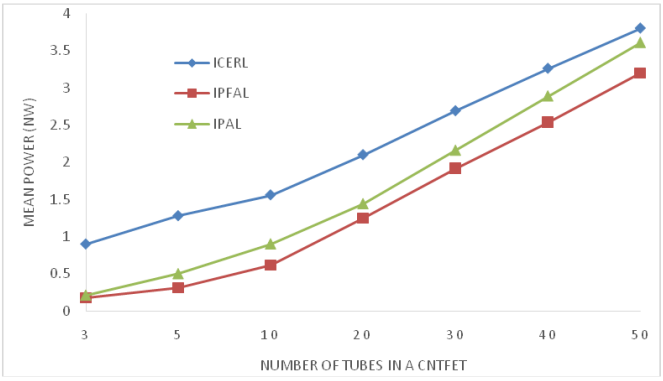

Fig 4 Power vs count of tube

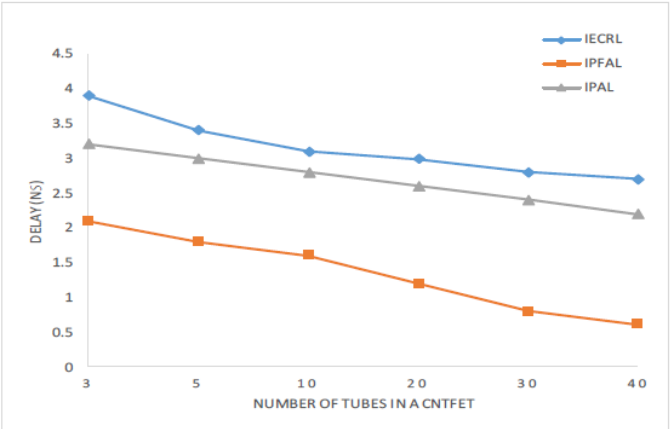

Fig 5. Delay vs. tube count of tube

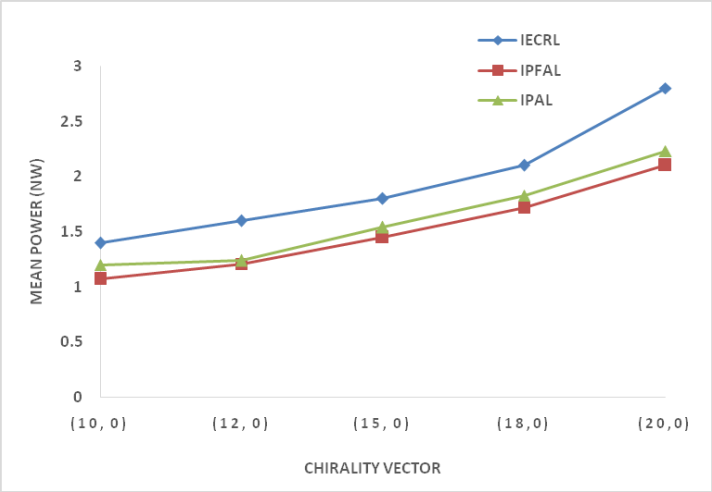

Fig 6. Power versus chirality vector

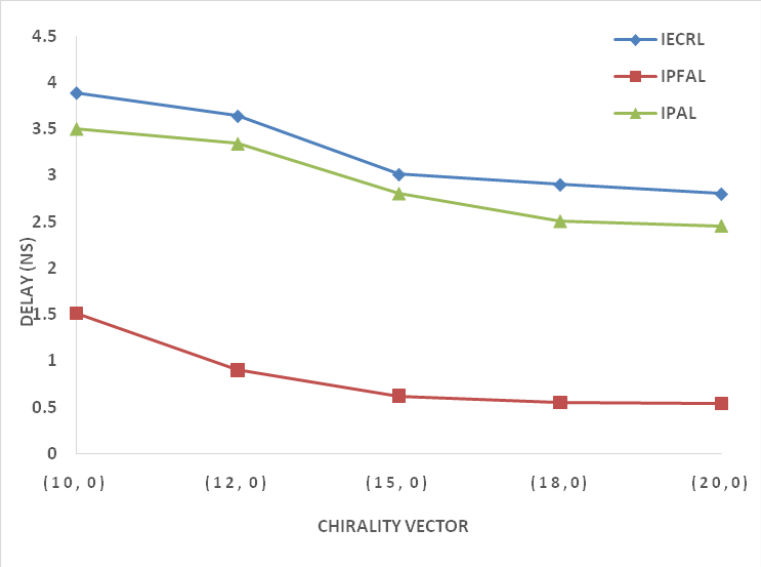

Fig 7. Delay versus Chirality Vector

Conclusions

The study establishes a set of optimized parameters for CNTFET-based BCAM cells. The circuits were implemented using 32nm technology nodes, with transistor modeling carried out using the Predictive Technology Model (PTM). Circuit simulations were conducted using HSPICE to evaluate performance metrics. A comparative analysis was performed between conventional CMOS-based BCAM cells and the proposed CNTFET-based designs.

The results validate significant developments in both delay and average power consumption for the projected cells. Notably, the mean power dissipation of the CNTFET-based BCAM cells is observed in the nanowatt range, in contrast to the microwatt range for their CMOS counterparts. Quantitatively, the proposed CNTFET implementation achieves a 90.8% reduction in mean power

consumption and a 56.4% improvement in delay compared to traditional CMOS-based BCAM cells.

FUTURE SCOPE OF THE WORK

In the future, we propose to explore the design of CAM cells exploiting advanced logic families aimed at achieving low power consumption and high-speed performance, employing both CNTFET and Graphene Nano Ribbon Field Effect Transistors (GNRFETs). These emerging technologies hold strong potential for improving circuit efficiency beyond the capabilities of conventional devices.

An equally critical component of CAM architecture is the Match Line Sensing Amplifier (MLSA). Future work will also focus on the design and optimisation of MLSAs using GNRFETs and CNTFETs, to improve key performance metrics such as speed, power efficiency, and Static Noise Margin (SNM).

Additionally, recent advancements in modern nano-interconnects have shown remarkable improvements in VLSI circuits with reference to signal stability, driving capability, power efficiency, speed, and noise immunity. Building upon these developments, we plan to extend our research to incorporate nano-interconnect technologies into CAM architectures to enhance their overall performance.

References

[1] Algamili, A. S., Khir, M. H. M., Dennis, J. O., Ahmed, A. Y., Alabsi, S. S., Hashwan, S. S. B., & Junaid, M. (2021). A review of actuation and sensing mechanisms in MEMS-based sensor devices. Nanoscale research letters, 16(1), 1-21. DOI: 10.1186/s11671-021-03481-7

[2] Abdelaziz, B., Fouad, K., & Kemouche, S. (2024). The effect of temperature and doping level on the characteristics of piezoresistive pressure sensor. Journal of Sensor Technology, 4(2), 59. DOI: 10.4236/jst.2024.42007.

[3] Aurich, J. C., Kirsch, B., Setti, D., Axinte, D., Beaucamp, A., Butler-Smith, P., & Yamaguchi, H. (2019). Abrasive processes for micro parts and structures. CIRP Annals, 68(2), 653-676. DOI: 10.1016/j.cirp.2019.05.006.

[4] A.L. Herrer-May, B.S. Soto-Cruz, F. Lopez-Huerta and L.A. Aguilera Cortes, “Electromechanical analysis of a piezoresistive pressure microsensor for low pressure biomedical applications”, Revista Mexicana de Física (Mexican Journal of physics), vol. 55, no. 1, pp. 14-24, Feb. 2009.

[5] A. Bernsa, U. Budera, E. Obermeiera, A. Wolterb and A. Lederb, “AeroMEMS sensor array for high-resolution wall pressure measurements”, Sensors and Actuators A: Physical, vol. 132, Issue 1, Pages 104–111, 8 Nov. 2006.

[6] Angel, S., & Daniel, R. J. (2017, January). Sensitivity enhancement by striped arrow embossed diaphragms in low pressure MEMS piezoresistive pressure sensors. In 2017 Trends in Industrial Measurement and Automation (TIMA) (pp. 1-5). IEEE.

[7] Arkwright, J. W., Underhill, I. D., Maunder, S. A., Jafari, A., Cartwright, N., & Lemckert, C. (2014). Fiber optic pressure sensing arrays for monitoring horizontal and vertical

pressures generated by traveling water waves. IEEE Sensors Journal, 14(8), 2739-2742. DOI: 10.1109/JSEN.2014.2311806.
[8] Aqel, A., Abou El-Nour, K. M., Ammar, R. A., & Al-Warthan, A. (2012). Carbon nanotubes, science and technology part (I) structure, synthesis and characterisation. Arabian Journal of Chemistry, 5(1), 1-23.
[9] Akiyama, M., Morofuji, Y., Kamohara, T., Nishikubo, K., Tsubai, M., Fukuda, O., & Ueno, N. (2006). Flexible piezoelectric pressure sensors using oriented aluminum nitride thin films prepared on polyethylene terephthalate films. Journal of applied physics, 100(11), 114318.
[10] Almassri, A. M., Wan Hasan, W. Z., Ahmad, S. A., Ishak, A. J., Ghazali, A. M., Talib, D. N., & Wada, C. (2015). Pressure sensor: state of the art, design, and application for robotic hand. Journal of Sensors, 2015.
[11] Ali, A., Khan, A., Ali, A., & Ahmad, M. (2017). Pressure-sensitive properties of carbon nanotubes/bismuth sulfide composite materials. Nanomaterials and Nanotechnology, 7, 1847980417707087.
[12] Abderahman, H. N., Dajani, H. R., Bolic, M., & Groza, V. Z. (2016, May). An integrated system to compensate for temperature drift and ageing in noninvasive blood pressure measurement. In 2016 IEEE International Symposium on Medical Measurements and Applications (MeMeA) (pp. 1-6). IEEE.
[13] Avouris, P. (2004). Supertubes [carbon nanotubes]. IEEE spectrum, 41(8), 40- 45.
[14] Al Mahruz, T., Matin, R., Wahid, F. B., & Dev, T. (2016). Material and performance analysis of MEMS piezoresistive pressure sensor. Int. J. Eng.Trends Technol.(IJETT), 31(1), 10-14.
[15] Ali, A., Khan, A., Karimov, K. S., Ali, A., & Daud Khan, A. (2018). Pressure sensitive sensors based on carbon nanotubes, graphene, and its composites. Journal of Nanomaterials, 2018.
[16] Alam, M. A., Hamdan, H. Y., Azeem, M., Hussain, P. B., bin Salit, M. S.,Khan, R., ... & Ansari, A. H. (2020). Modelling and optimization of hardness behavior of sintered Al/SiC composites using RSM and ANN: A comparative study. Journal of Materials Research and Technology, 9(6), 14036-14050.